SERDES Demonstration Kit User Manual

NSID: SERDES03-40USB

(DS99R103/104)

Rev 0.1

Table of Contents

Introduction:

National Semiconductor's SERDES evaluation kit contains one (1) DS99R103 Serializer (Tx) board, one (1) DS99R104 De-serializer (Rx) board, and one (1) two (2) meter high speed USB 2.0 cable.
Note: the demo boards are not for EMI testing. The demo boards were designed for easy accessibility to device pins with tap points for monitoring or applying signals, additional pads for termination, and multiple connector options.

The DS99R103/104 chipset supports a variety of display applications. The single FPD-LINKII (FPD-LinkII) interface is well-suited for any display system interface. Typical applications include: navigation displays, automated teller machines (ATMs), POS, video cameras, global positioning systems (GPS), portable equipment/instruments, factory automation, etc.

The DS99R103 and DS99R104 can be used as a 24-bit general purpose FPD-LinkII Serializer and De-serializer chipset designed to transmit data at clocks speeds ranging from 3 to 40 MHz.

The Serializer board accepts LVCMOS input signals. The FPD-LinkII Serializer converts the LVCMOS parallel lines into a single serialized FPD-LINKII data pair with an embedded FPD-LINKII clock. The serial data stream toggles at 28 times the base clock rate. With an input clock at 40 MHz, the transmission rate for FPD-LinkII line is 960Mbps.

The De-serializer board accepts the FPD-LinkII serialized data stream with embedded clock and converts the data back into parallel LVCMOS signals and clock. Note that NO reference clock is needed to prevent harmonic lock as with other devices currently on the market.

Suggested equipment to evaluate the chipset, an LVCMOS signal source such as a video generator or word generator or pulse generator and oscilloscope with a bandwidth of at least 40 MHz will be needed.

The user needs to provide the proper LVCMOS/RGB inputs and LVCMOS/clock to the Serializer and also provide a proper interface from the De-serializer output to an LCD panel or test equipment. The Serializer and De-serializer boards can also be used to evaluate device parameters. A cable conversion board or harness scramble may be necessary depending on type of cable/connector interface used on the input to the DS99R103 and to the output of the DS99R104.

Example of suggested display setup:
1) video generator with LVCMOS output
2) 6-bit LCD panel with a LVCMOS input interface.

Contents of the Evaluation Kit:

1) One Serializer board with the DS99R103
2) One De-serializer board with the DS99R104
3) One 2-meter high speed USB 2.0 cable (4-pin USB A to 5-pin mini USB)
4) Evaluation Kit Documentation (this manual)
5) DS99R103/104 Datasheet

SERDES Typical Application:

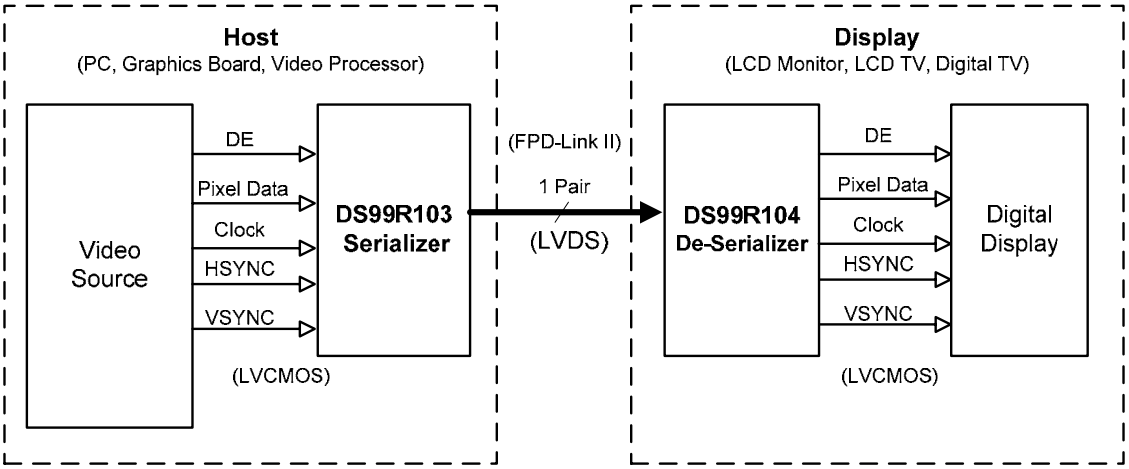


Figure 1a. Typical SERDES Application (18-bit RGB Color)

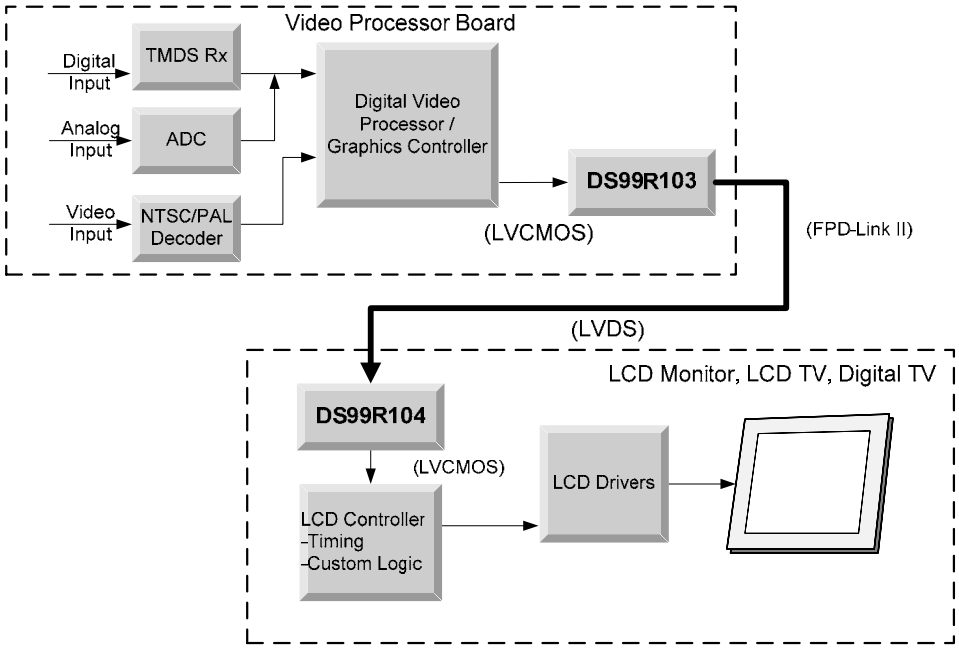


Figure 1b. Typical SERDES System Diagram

Figures 1a and 1b illustrate the use of the Chipset (Tx/Rx) in a Host to Flat Panel Interface.

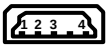
The chipsets support up to 18-bit color depth TFT LCD Panels.

Refer to the proper datasheet information on Chipsets (Tx/Rx) provided on each board for more detailed information.

How to set up the Evaluation Kit:

The PCB routing for the Tx input pins (DIN) have been laid out to accept incoming LVCMOS signals from 50-pin IDC connector. The TxOUT/RxIN (DOUT/RIN) interface uses a single twisted pair cable (provided). The PCB routing for the Rx output pins (ROUT) are accessed through a 50-pin IDC connector. Please follow these steps to set up the evaluation kit for bench testing and performance measurements:

1) A two (2) meter high speed USB 2.0 cable has been included in the kit. A two (2) meter USB connector/cable assembly has been included in the kit. Connect 4-pin USB A 

A side of cable harness to the serializer board and the other side 5-pin mini USB jack 

MIN to the de-serializer board. This completes the FPD-LINKII interface connection.
NOTE: The DS99R103 and DS99R104 are NOT USB compliant and should not be plugged into a USB device nor should a USB device be plugged into the demo boards.

2) Jumpers and switches have been configured at the factory; they should not require any changes for immediate operation of the chipset. See text on Configuration settings for more details.

3) From the Video Decoder board, connect a flat cable (not supplied) to the Serializer board and connect another flat cable (not supplied) from the De-serializer board to the panel. *Note: For non 50 ohm signal sources, provide 3.3V LVCMOS input signal levels into DIN[23:0] and TCLK or remove the 49.9 ohm parallel termination resistors R1-R25 on the DS99R103 Serializer board.*

4) Power for the Tx and Rx boards must be supplied externally through Power Jack (VDD). Grounds for both boards are connected through Power Jack (VSS) (see section below).

Power Connection:

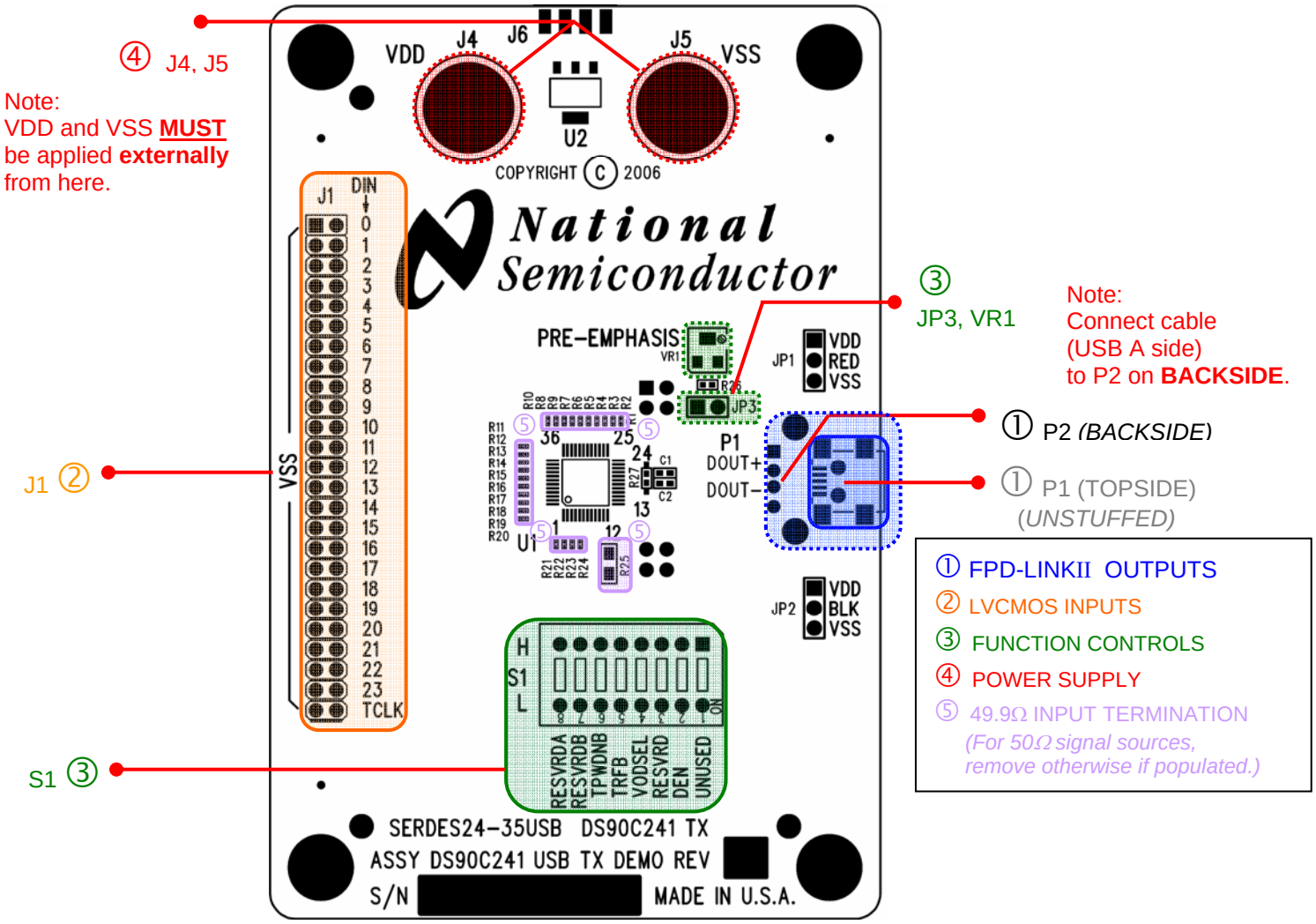
The Serializer and De-serializer boards must be powered by supplying power externally through J4 (VDD) and J5 (VSS) on Serializer Board and J4 (VDD) and J5 (VSS) on De-serializer board. Note +4V is the MAXIMUM voltage that should ever be applied to the SERDES Serializer (DS99R103) or De-serializer (DS99R104) VDD terminal. Damage to the device(s) can result if the voltage maximum is exceeded.

SERDES Serializer Board Description:

The 50-pin IDC connector J1 accepts 24 bits of LVCMOS RGB data along with the clock input.

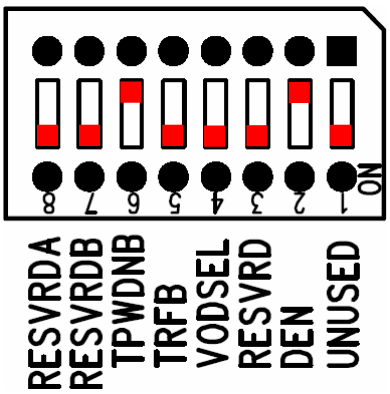
The SERDES Serializer board is powered externally from the J4 (VDD) and J5 (VSS) connectors shown below. For the Serializer to be operational, the Power Down (S1-TPWDNB) and Data Enable (S1-DEN) switches on S1 must be set HIGH. The board is factory configured (with series capacitors on the FPD-LINKII outputs) in AC coupled mode: S1- RESVRDA, RESVRDB, and VODSEL must be set LOW. Rising or falling edge reference clock is also selected on S1-TRFB: HIGH (rising) or LOW (falling).

The USB connector P2 (USB-A side) on the bottom side of the board provides the interface connection to the FPD-LINKII signals to the De-serializer board. Note: P1 (mini USB) on the top side is un-stuffed and not to be used with the cable provided in the kit.

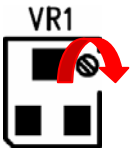
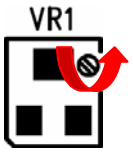


Configuration Settings for the Tx Board

S1: Serializer Input Features Selection

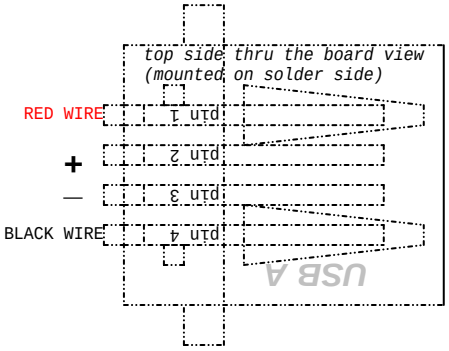
Reference	Description	Input = L	Input = H	S1
RESVRDA	**DCAOFF**	MUST be tied low for normal operation **(Default)**	-	
RESVRDB	**DCBOFF**	MUST be tied low for normal operation **(Default)**	-	
TPWDNB	**P**o**W**er**D**ow**N B**ar	Powers Down	Operational **(Default)**	
TRFB	Latch input data on **R**ising or **F**alling edge of TCLK	Falling Edge **(Default)**	Rising Edge	
VODSEL	FPD-LINKII output **VOD SEL**ect	≈350mV **(Default)**	≈700mV	
RESVRD	**RES**e**RV**e**D**	MUST be tied low for normal operation **(Default)**		
DEN	Output **D**ata **EN**abled	Disabled	Enabled **(Default)**	
UNUSED	UNUSED	Don't care	Don't care	

JP3,VR1: Pre-Emphasis Feature Selection

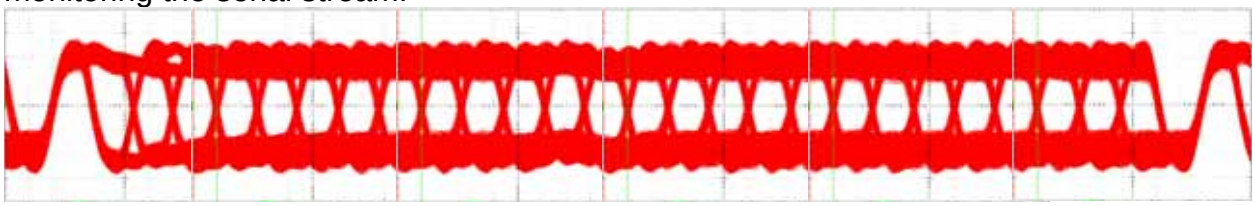
Reference	Description	OPEN (floating)	CLOSED (Path to GND)	
JP3	Pre-Emphasis – helps to increase the eye pattern opening in the FPD-LINKII stream	Disabled – no jumper **(Default)** 	Enabled – With jumper 	
JP3 & VR1	Pre-Emphasis adjustment (via screw) JP6 **MUST** have a jumper to use VR1 potentiometer. VR1 = 0Ω to 20KΩ, JP6 + VR1 + 6KΩ *(R6)* = ~6KΩ (maximum pre-emphasis) to ~26KΩ (minimum pre-emphasis*). $I_{PRE} = [1.2/(R_{PRE})] \times 40$, $R_{PRE\ (minimum)} \geq 6K\Omega$ **Note: maximum is based on resistor value. In this case ~26KΩ value is based on the ~6kΩ fixed resistor plus ~20KΩ maximum potentiometer value. User can use hundreds of Kohms to reduce the pre-emphasis value.*	Clockwise  increases R_{PRE} value which decreases pre-emphasis	Counter-Clockwise  decreases R_{PRE} value which increases pre-emphasis		

Pre-emphasis user note:
Pre-emphasis must be adjusted correctly based on application frequency, cable quality, cable length, and connector quality. Maximum pre-emphasis should only be used under extreme worse case conditions; for example at the upper frequency specification of the part and/or low grade cables at maximum cable lengths. Typically all that is needed is minimum pre-emphasis. Users should start with no pre-emphasis first and gradually apply pre-emphasis until there is clock lock and no data errors. The best way to monitor the pre-emphasis effect is to hook up a differential probe to the 100Ω termination resistor (R1) on the DS99R104 Rx demo board (NOT to R27 on the DS99R103 demo board). The reason for monitoring R1 on the Rx side is because you want to see what the receiver will see the attenuation signal AFTER the cable/connector.

JP1, JP2: USB Red and Black wire

Reference	Description	VDD	VSS	OPEN
JP1	Power wire in USB cable thru P2 *(and P1 not mounted)* connector Jumper RED to VSS – recommended *Note: Normally VDD in USB application*	Red wire tied to VDD 	Red wire tied to VSS **(Default)** 	Red wire floating (not recommended) 
JP2	Power wire in USB cable thru P2 *(and P1 not mounted)* connector Jumper BLACK to VSS – recommended *Note: Normally VSS in USB application*	Black wire tied to VDD 	Black wire tied to VSS **(Default)** 	Black wire floating (not recommended) 
 **P2**				

The following picture depicts a typical example of the FPD-Link II serial stream. This snapshot was taken with a differential probe across the 100 ohm termination resistor R1 on the DS99R104 Rx evaluation board. R1 is the termination resistor to the RxIN +/-. Note: The scope was triggered, with a separate probe, on TCLK, the input clock into the DS99R103 Tx. To view the serial stream correctly, do not trigger on the probe monitoring the serial stream.



Tx LVCMOS and FPD-LINKII Pinout by IDC Connector

The following three tables illustrate how the Tx inputs are mapped to the IDC connector J1, the FPD-LINKII outputs on the USB-A connector P2, and the mini USB P1 (not installed) pinouts. Note – labels are also printed on the demo boards for both the lvcmos input and FPD-LINKII outputs.

J1
LVCMOS INPUT

pin no.	name	name	pin no.
1	GND	**DIN0**	2
3	GND	**DIN1**	4
5	GND	**DIN2**	6
7	GND	**DIN3**	8
9	GND	**DIN4**	10
11	GND	**DIN5**	12
13	GND	**DIN6**	14
15	GND	**DIN7**	16
17	GND	**DIN8**	18
19	GND	**DIN9**	20
21	GND	**DIN10**	22
23	GND	**DIN11**	24
25	GND	**DIN12**	26
27	GND	**DIN13**	28
29	GND	**DIN14**	30
31	GND	**DIN15**	32
33	GND	**DIN16**	34
35	GND	**DIN17**	36
37	GND	**DIN18**	38
39	GND	**DIN19**	40
41	GND	**DIN20**	42
43	GND	**DIN21**	44
45	GND	**DIN22**	46
47	GND	**DIN23**	48
49	GND	**TCLK**	50

P2
(bottom side)

FPD-LINKII OUTPUT

pin no.	name
1	JP1
2	**DOUT+**
3	**DOUT-**
4	JP2

P1
(topside)

(not mounted)

FPD-LINKII OUTPUT

pin no.	*name*
5	*JP2*
4	*NC*
3	***DOUT-***
2	***DOUT+***
1	*JP1*

BOM (Bill of Materials) Serializer PCB:

DS99R103 Tx USB Demo Board - Board Stackup Revised: Thursday, March 23, 2006
DS99R103 Tx USB Demo Board Revision: 1
Bill Of Materials March 23,2006 18:52:42

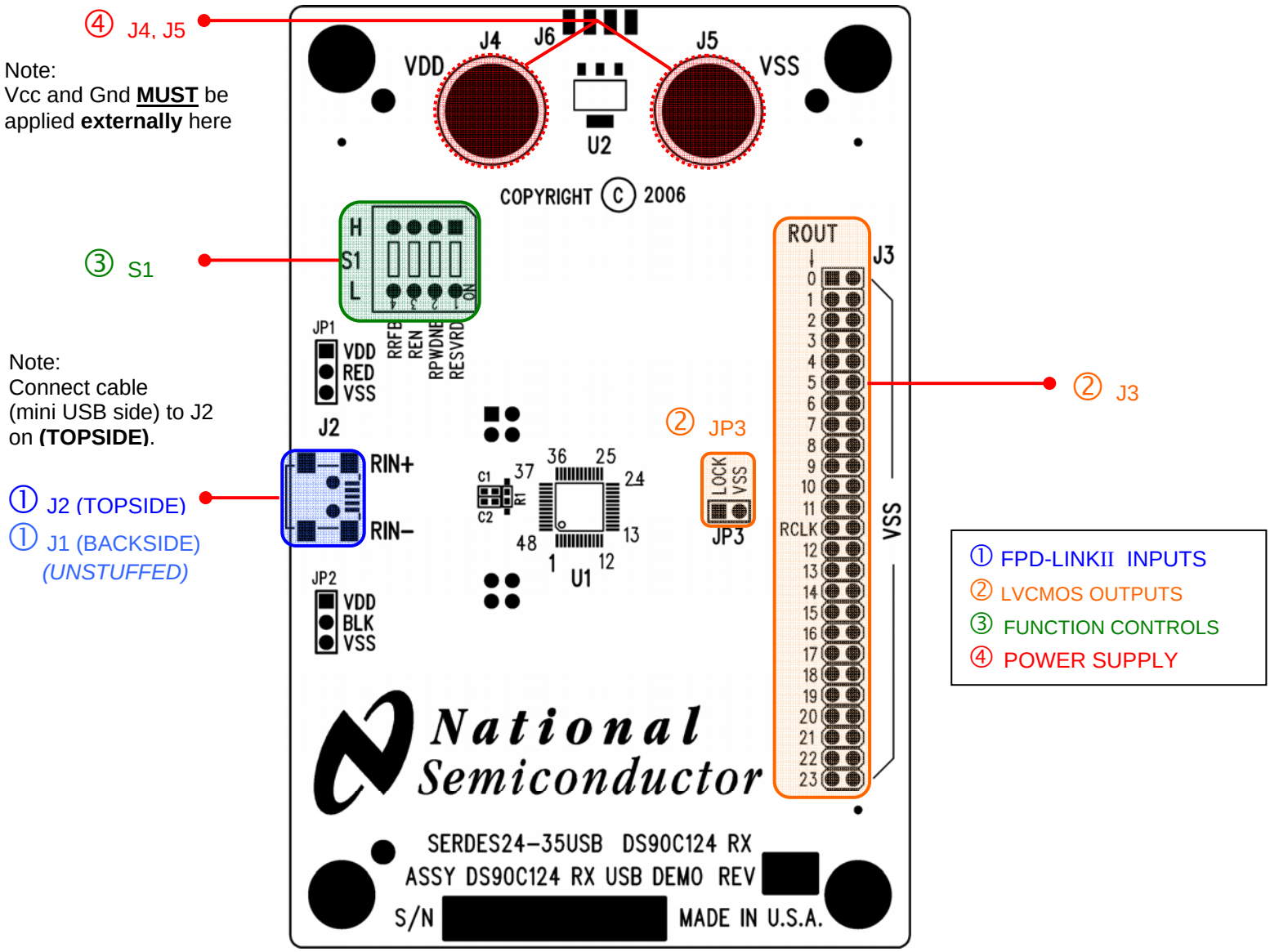
Item	Qty	Reference	Part	PCB Footprint
1	2	C1,C2	0.1uF	CAP/HDC-0402
2	1	C3	2.2uF	3528-21_EIA
3	1	C4	22uF	CAP/N
4	1	C5	0.1uF	CAP/HDC-1206
5	5	C6,C9,C10,C13,C20	22uF	CAP/EIA-B 3528-21
6	5	C7,C11,C15,C16,C19	0.01uF	CAP/HDC-0603
7	5	C8,C12,C14,C17,C18	0.1uF	CAP/HDC-0603
8	2	JP2,JP1	3-Pin Header	Header/3P
9	1	JP3	2-Pin Header	Header/2P
10	1	J1	IDC2X25_Unshrouded	IDC-50
11	2	J5,J4	BANANA	CON/BANANA-S
12	1	P1	mini USB 5pin_open	mini_USB_surface_mount
13	1	P2	USB A	USB_TYPE_A_4P
14	24	R1,R2,R3,R4,R5,R6,R7,R8, R9,R10,R11,R12,R13,R14, R15,R16,R17,R18,R19,R20, R21,R22,R23,R24	49.9ohm_open	RES/HDC-0201
15	1	R25	49.9ohm_open	RES/HDC-0805
16	1	R26	5.76K (3.01K)	RES/HDC-0402
17	1	R27	100 ohm,0402	RES/HDC-0402
18	5	R28,R30,R32,R33,R35	0 Ohm,0402	RES/HDC-0402
19	8	R38,R39,R40,R41,R42,R43, R44,R45	10K	RES/HDC-0805
20	1	S1	SW DIP-8	DIP-16
21	1	U1	DS99R103	48 ld TQFP
22	1	VR1	SVR20K	Surface Mount 4mm Square

Rx SERDES De-serializer Board:

The USB connector J2 (mini USB) on the topside of the board provides the interface connection for FPD-LINKII signals to the Serializer board. Note: J1 (mini USB) on the bottom side is un-stuffed and not used with the cable provided in the kit.

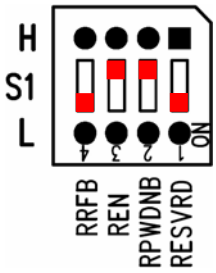
The SERDES De-serializer board is powered externally from the J4 (VDD) and J5 (VSS) connectors shown below. For the De-serializer to be operational, the Power Down (RPWDNB) and Receiver Enable (REN) switches on S1 must be set HIGH. Rising or falling edge reference clock is also selected by S1: HIGH (rising) or LOW (falling).

The 50 pin IDC Connector J3 provides access to the 24 bit LVCMOS and clock outputs.



Configuration Settings for the Rx Board

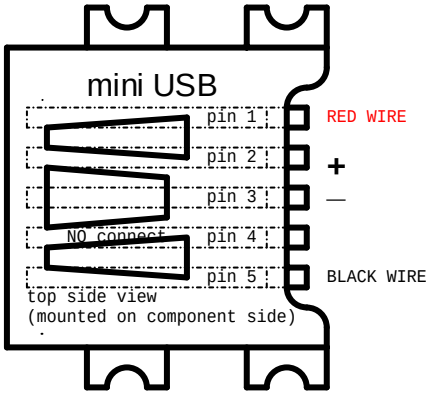
S1: De-serializer Input Features Selection

Reference	Description	Input = L	Input = H	S1
RFB	Latch output data on **R**ising or **F**alling Data Strobe of RCLK	Falling (Default)	Rising	
REN	**R**eceiver Output **EN**abled	Disabled	Enabled (Default)	
RPWDNB	**P**o**W**er**D**ow**N** **B**ar	Power Down (Disabled)	Operational (Default)	
RESVRD	**RES**e**RVeD**	Don't care	Don't care	

JP3: Output Lock Monitor

Reference	Description	Output = L	Output = H	JP3
LOCK	Receiver PLL **LOCK** **Note:** **DO NOT PUT A SHORTING JUMPER IN JP3.**	locked	unlocked	

JP1, JP2: USB Red and Black wire

Reference	Description	VDD	VSS	OPEN
JP1	Power wire in USB cable thru J2 *(and J1 not mounted)* connector Jumper RED to VSS – recommended *Note: Normally VDD in USB application*	Red wire tied to VDD 	Red wire tied to VSS **(Default)** 	Red wire floating (not recommended) 
JP2	Power wire in USB cable thru J2 *(and J1 not mounted)* connector Jumper BLACK to VSS – recommended *Note: Normally VSS in USB application*	Black wire tied to VDD 	Black wire tied to VSS **(Default)** 	Black wire floating (not recommended) 
J2 				

Rx FPD-LINKII Pinout and LVCMOS by IDC Connector

The following three tables illustrate how the Rx outputs are mapped to the IDC connector J3, the mini USB FPD-LINKII connector J2, and the mini USB FPD-LINKII connector J1 (not installed) pinouts. Note – labels are also printed on the demo boards for both the FPD-LINKII inputs and LVCMOS outputs.

J3 LVCMOS INPUT			
pin no.	**name**	**name**	**pin no.**
1	**ROUT0**	GND	2
3	**ROUT1**	GND	4
5	**ROUT2**	GND	6
7	**ROUT3**	GND	8
9	**ROUT4**	GND	10
11	**ROUT5**	GND	12
13	**ROUT6**	GND	14
15	**ROUT7**	GND	16
17	**ROUT8**	GND	18
19	**ROUT9**	GND	20
21	**ROUT10**	GND	22
23	**ROUT11**	GND	24
25	**RCLK**	GND	26
27	**ROUT12**	GND	28
29	**ROUT13**	GND	30
31	**ROUT14**	GND	32
33	**ROUT15**	GND	34
35	**ROUT16**	GND	36
37	**ROUT17**	GND	38
39	**ROUT18**	GND	40
41	**ROUT19**	GND	42
43	**ROUT20**	GND	44
45	**ROUT21**	GND	46
47	**ROUT22**	GND	48
49	**ROUT23**	GND	50

J2 (topside) FPD-LINKII OUTPUT	
pin no.	**name**
1	JP1
2	**DOUT+**
3	**DOUT-**
4	NC
5	JP2

J1 (bottom side) (not mounted) FPD-LINKII OUTPUT	
pin no.	*name*
5	*JP2*
4	*NC*
3	***DOUT-***
2	***DOUT+***
1	*JP1*

BOM (Bill of Materials) De-serializer PCB:

DS99R104 Rx USB Demo Board - Board Stackup Revised: Thursday, March 23, 2006
DS99R104 Rx USB Demo Board Revision: 1
Bill Of Materials March 23,2006 19:19:22

Item	Qty	Reference	Part	PCB Footprint
1	2	C2,C1	0.1uF	CAP/HDC-0402
2	1	C3	2.2uF	3528-21_EIA
3	1	C4	22uF	CAP/N
4	1	C5	0.1uF	CAP/HDC-1206
5	26	C6,C7,C8,C9,C10,C11,C12, C13,C14,C15,C16,C17,C18, C19,C20,C21,C22,C23,C24, C25,C26,C27,C28,C29,C30, C39	open0402	CAP/HDC-0402
6	8	C31,C32,C33,C38,C43,C49, C54,C55	22uF	CAP/EIA-B 3528-21
7	8	C34,C37,C40,C44,C45,C48, C52,C53	0.1uF	CAP/HDC-0603
8	8	C35,C36,C41,C42,C46,C47, C50,C51	0.01uF	CAP/HDC-0603
9	2	JP2,JP1	3-Pin Header	Header/3P
10	1	JP3	2-Pin Header	Header/2P
11	1	J1	mini USB 5pin_open	mini_USB_surface_mount
12	1	J2	mini USB 5pin	mini_USB_surface_mount
13	1	J3	IDC2X25_Unshrouded	IDC-50
14	2	J4,J5	BANANA	CON/BANANA-S
15	1	R1	100 ohm,0402	RES/HDC-0402
16	1	R2	10K_open	RES/HDC-0805
17	3	R3,R4,R5	10K	RES/HDC-0805
18	8	R7,R8,R9,R10,R11,R12,R13, R14	0 Ohm,0402	RES/HDC-0402
19	1	S1	SW DIP-4	DIP-4
20	1	U1	DS99R104	48 pin TQFP

Typical Connection and Test Equipment

The following is a list of typical test equipment that may be used to generate signals for the TX inputs:

1) Digital Video Source – for generation of specific display timing such as Digital Video Processor or Graphics Controller with digital RGB (LVCMOS) output.
2) Astro Systems VG-835 - This video generator may be used for video signal sources for 6-bit Digital LVCMOS/RGB.
3) Any other signal / video generator that generates the correct input levels as specified in the datasheet.
4) Optional – Logic Analyzer or Oscilloscope

The following is a list of typically test equipment that may be used to monitor the output signals from the RX:

1) LCD Display Panel which supports digital RGB (LVCMOS) inputs.
2) National Semiconductor DS99R103 Serializer (Tx)
3) Optional – Logic Analyzer or Oscilloscope
4) Any SCOPE with a bandwidth of at least 40MHz for LVCMOS and/or 1GHz for looking at the differential signal.

FPD-LINKII signals may be easily measured with high impedance / high bandwidth differential probes such as the TEK P6247 or P6248 differential probes.

The picture below shows a typical test set up using a Graphics Controller and LCD Panel.

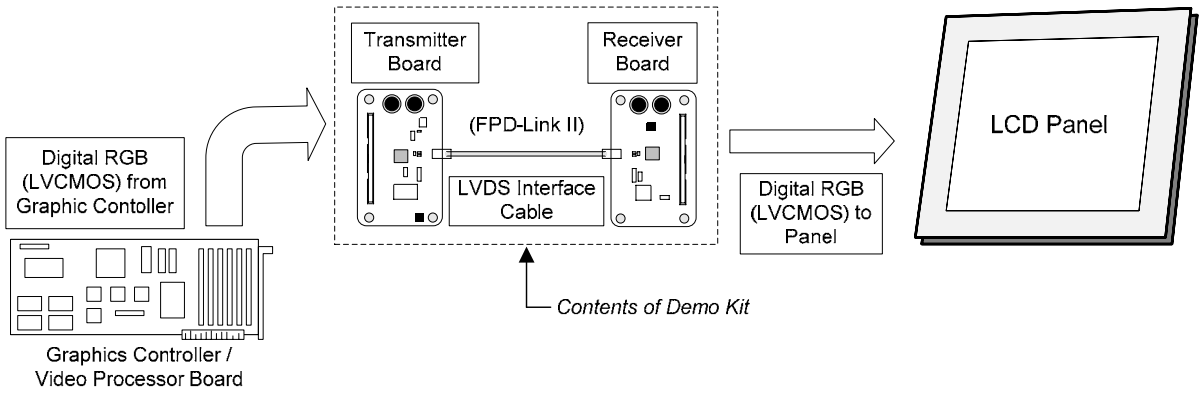


Figure 2. Typical SERDES Setup of LCD Panel Application

The picture below shows a typical test set up using a generator and scope.

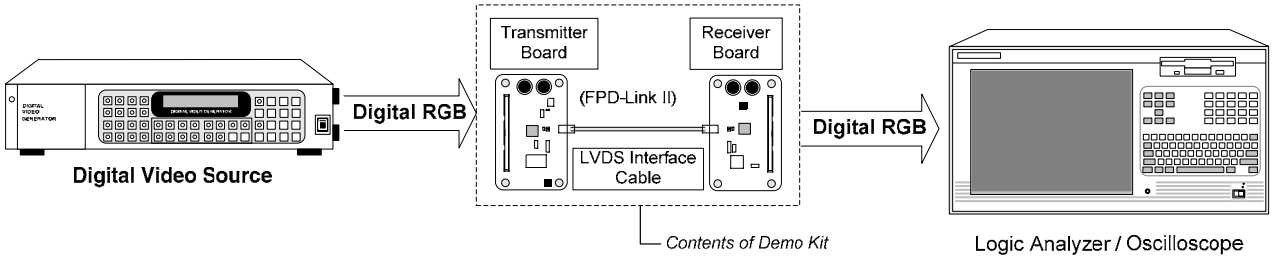


Figure 3. Typical SERDES Test Setup for Evaluation

Troubleshooting

NOTE: The DS99R103 and DS99R104 are NOT USB compliant and should not be plugged into a USB device nor should a USB device be plugged into the demo boards.

If the demo boards are not performing properly, use the following as a guide for quick solutions to potential problems. If the problem persists, please contact the local Sales Representative for assistance.

QUICK CHECKS:

1. Check that Power and Ground are connected to both Tx AND Rx boards.
2. Check the supply voltage (typical 3.3V) and also current draw with both Tx and Rx boards. The Serializer board should draw about 40-50mA with clock and all data bits switching at 40MHz. The De-serializer board should draw about 70-80mA with clock and all data bits switching at 40MHz.
3. Verify input clock and input data signals meet requirements (VIL, VIH, tset, thold), Also verify that data is strobed on the selected rising/falling (RFB pin) edge of the clock.
4. Check that the Jumpers and Switches are set correctly.
5. Check that the cable is properly connected.

TROUBLESHOOTING CHART

Problem…	**Solution…**
There is only the output clock. There is no output data.	Make sure the data is applied to the correct input pin. Make sure data is valid at the input.
No output data and clock.	Make sure Power is on. Input data and clock are active and connected correctly. Make sure that the cable is secured to both demo boards.
Power, ground, input data and input clock are connected correctly, but no outputs.	Check the Power Down pins of both Serializer and De-serializer boards to make sure that the devices are enabled (/PD=Vcc) for operation. Also check DEN on the Serializer board and REN on the Deserializer board is set HIGH.
The devices are pulling more than 1A of current.	Check for shorts in the cables connecting the TX and RX boards.
After powering up the demo boards, the power supply reads less than 3V when it is set to 3.3V.	Use a larger power supply that will provide enough current for the demo boards, a 500mA minimum power supply is recommended.

Note: Please note that the following references are supplied only as a courtesy to our valued customers. It is not intended to be an endorsement of any particular equipment or hardware supplier.

Equipment References

Digital Video Pattern Generator – Astro Systems VG-835 (or equivalent):

Astro Systems
425 S. Victory Blvd. Suite A
Burbank, CA 91502
Phone: (818) 848-7722
Fax: (818) 848-7799
www.astro-systems.com

Extra Component References

TDK Corporation of America
1740 Technology Drive, Suite 510
San Jose, CA 95110
Phone: (408) 437-9585
Fax: (408) 437-9591
www.component.tdk.com
Optional EMI Filters – TDK Chip Beads (or equivalent)

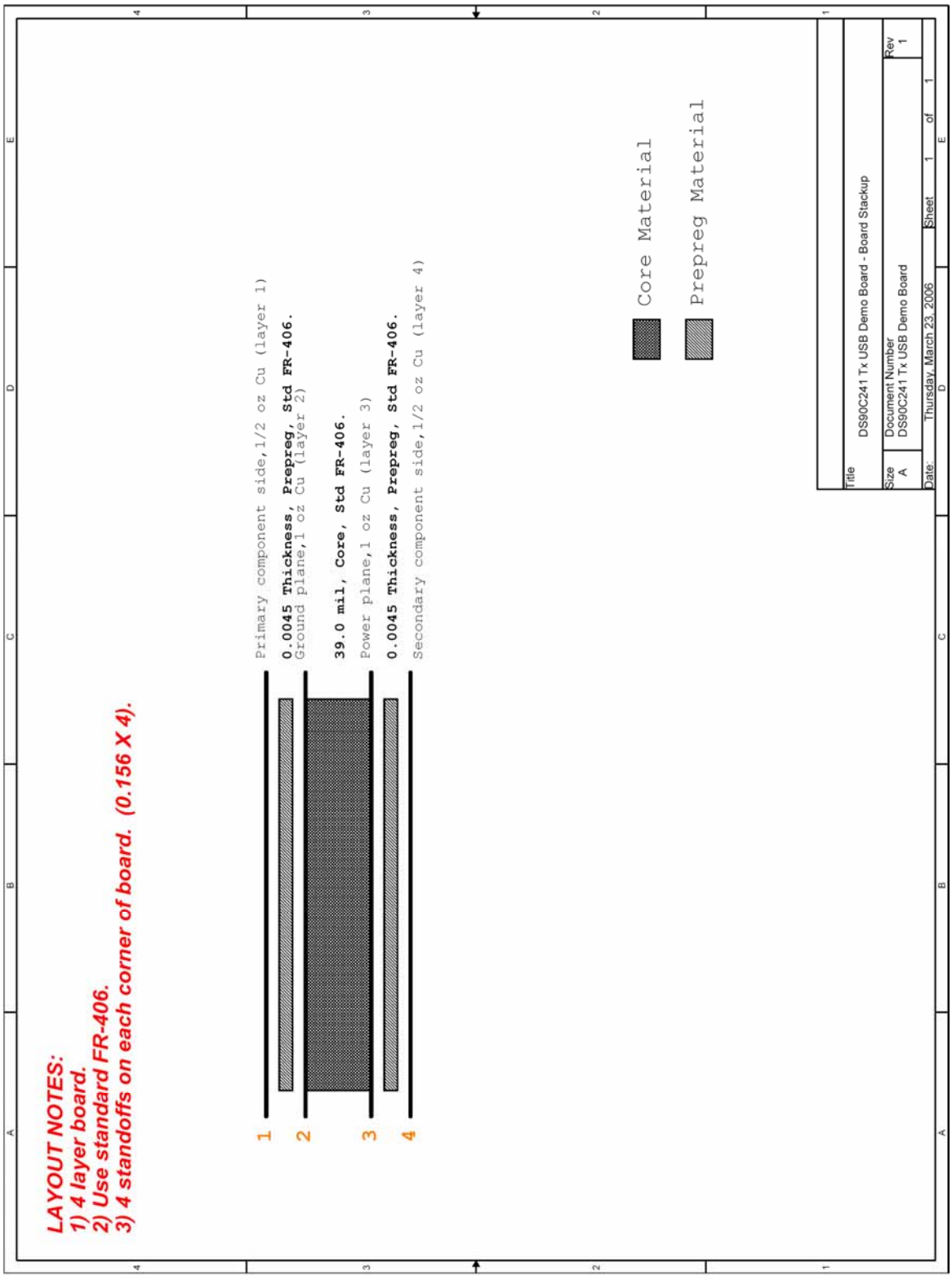
Cable References

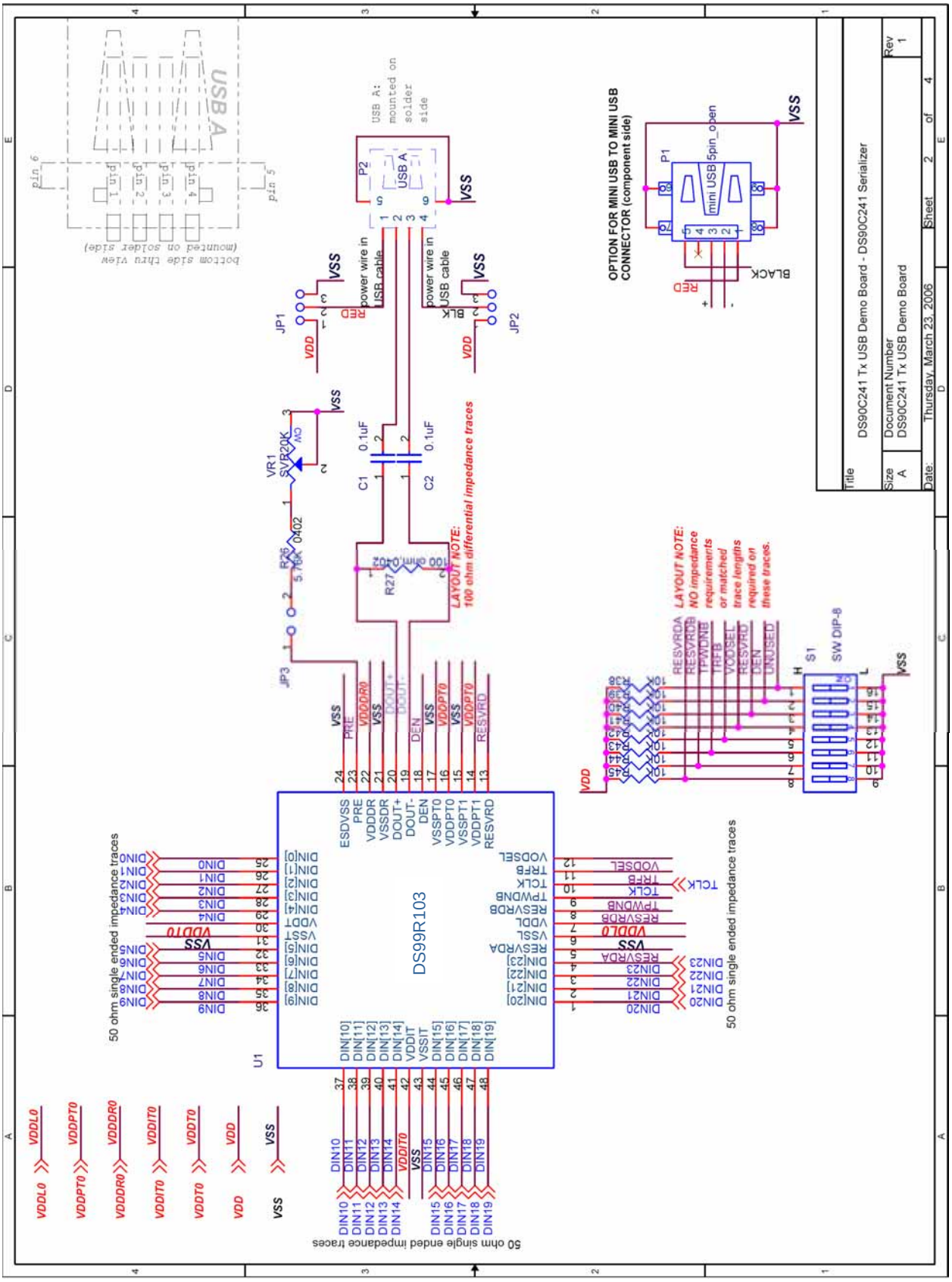
The FPD-LINKII interface cable included in the kit is a standard off-the-shelf high-speed USB 2.0 with a 4-pin USB A type on one end and a 5-pin mini USB on the other end and is included for demonstration purposes only.
NOTE: The DS99R103 and DS99R104 are NOT USB compliant and should not be plugged into a USB device nor should a USB device be plugged into the demo boards.
The inclusion of the USB cable in the kit is for:
1) Demonstrating the robustness of the FPD-LINKII link over ordinary twisted pair data cables.
2) Readily available and in different lengths without having custom cables made.

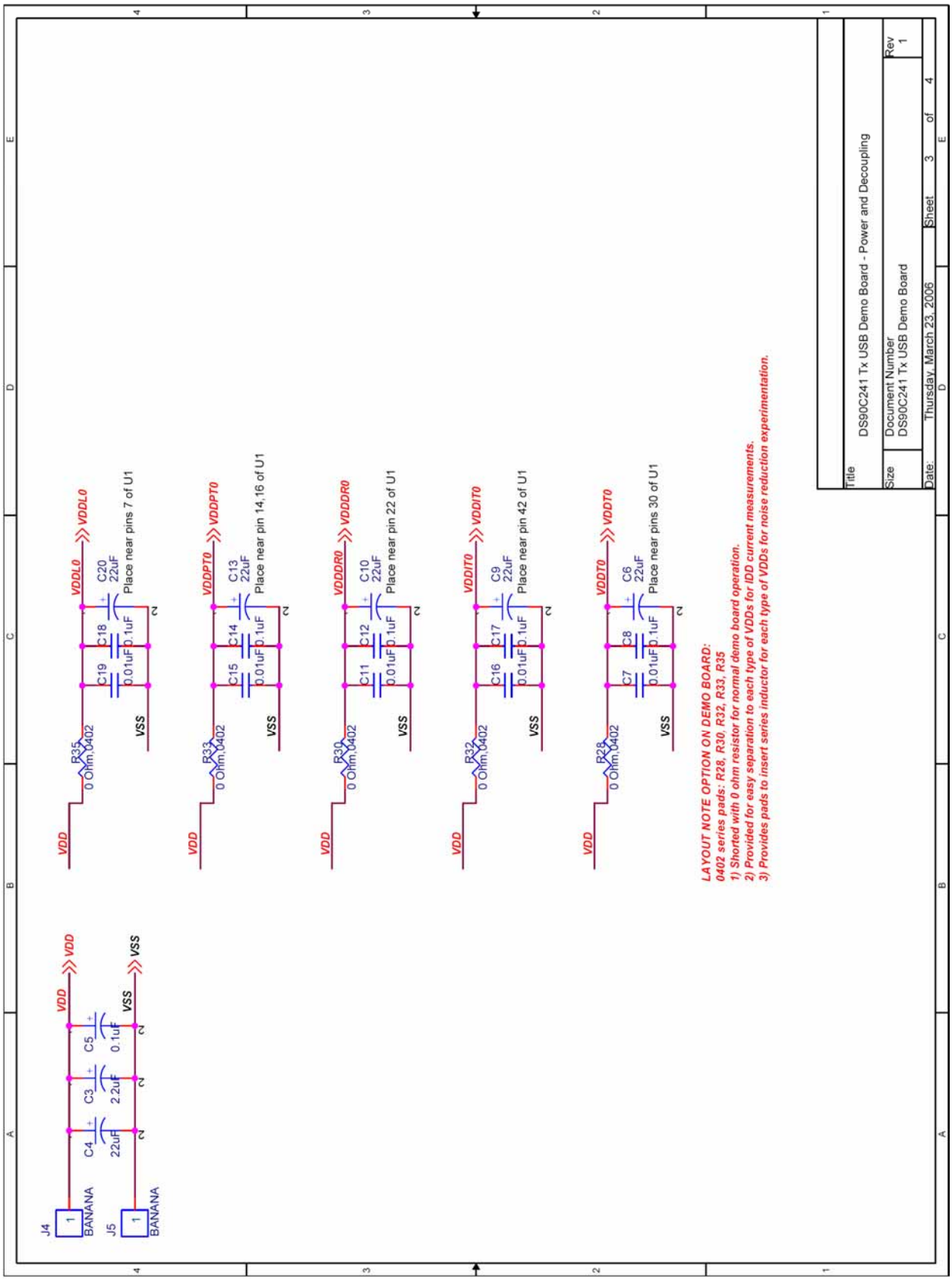
- For optimal performance, we recommend Shielded Twisted Pair (STP) 100Ω differential impedance cable for high-speed data applications.

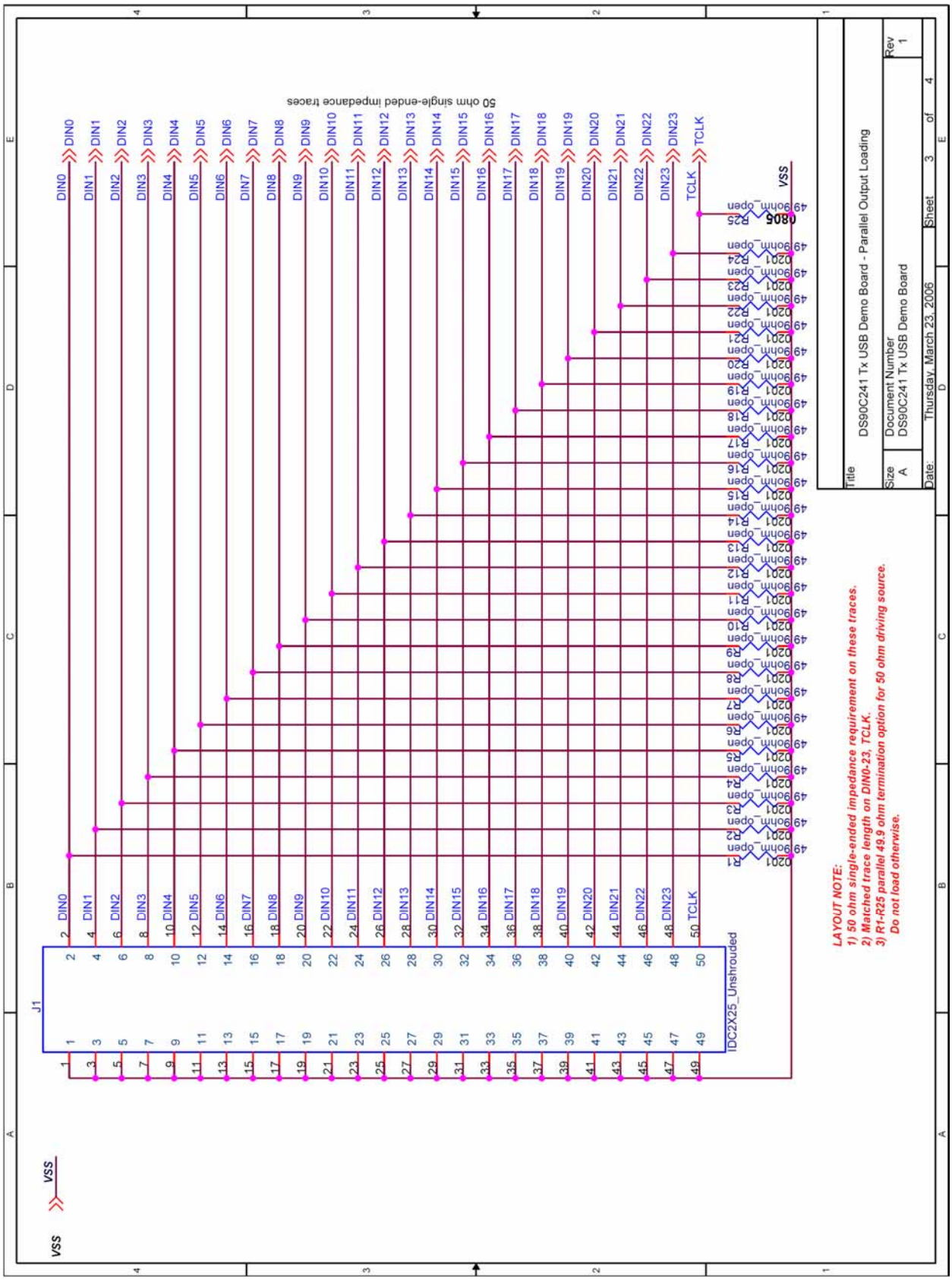
Appendix

Serializer (Tx) PCB Schematic:

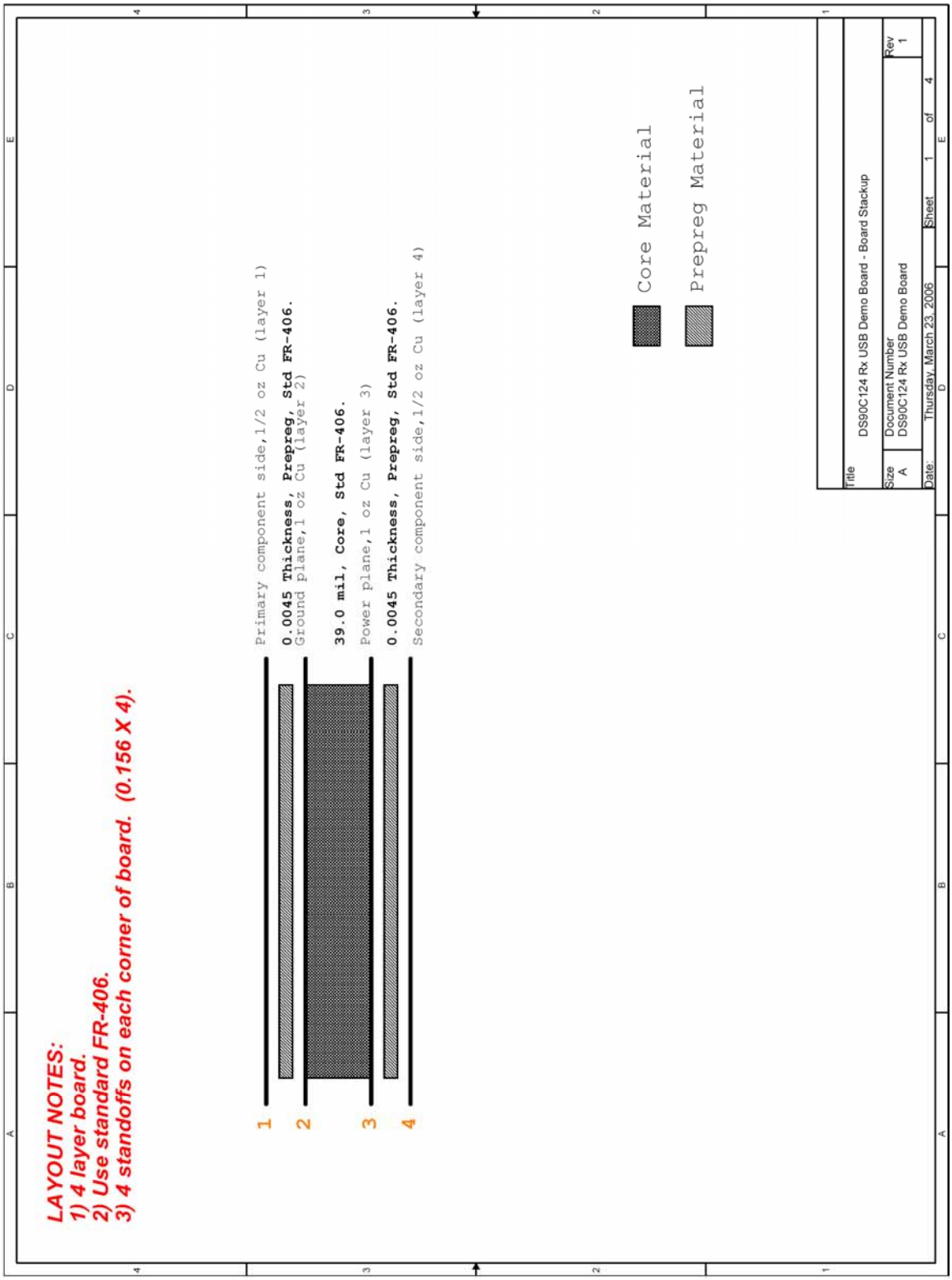


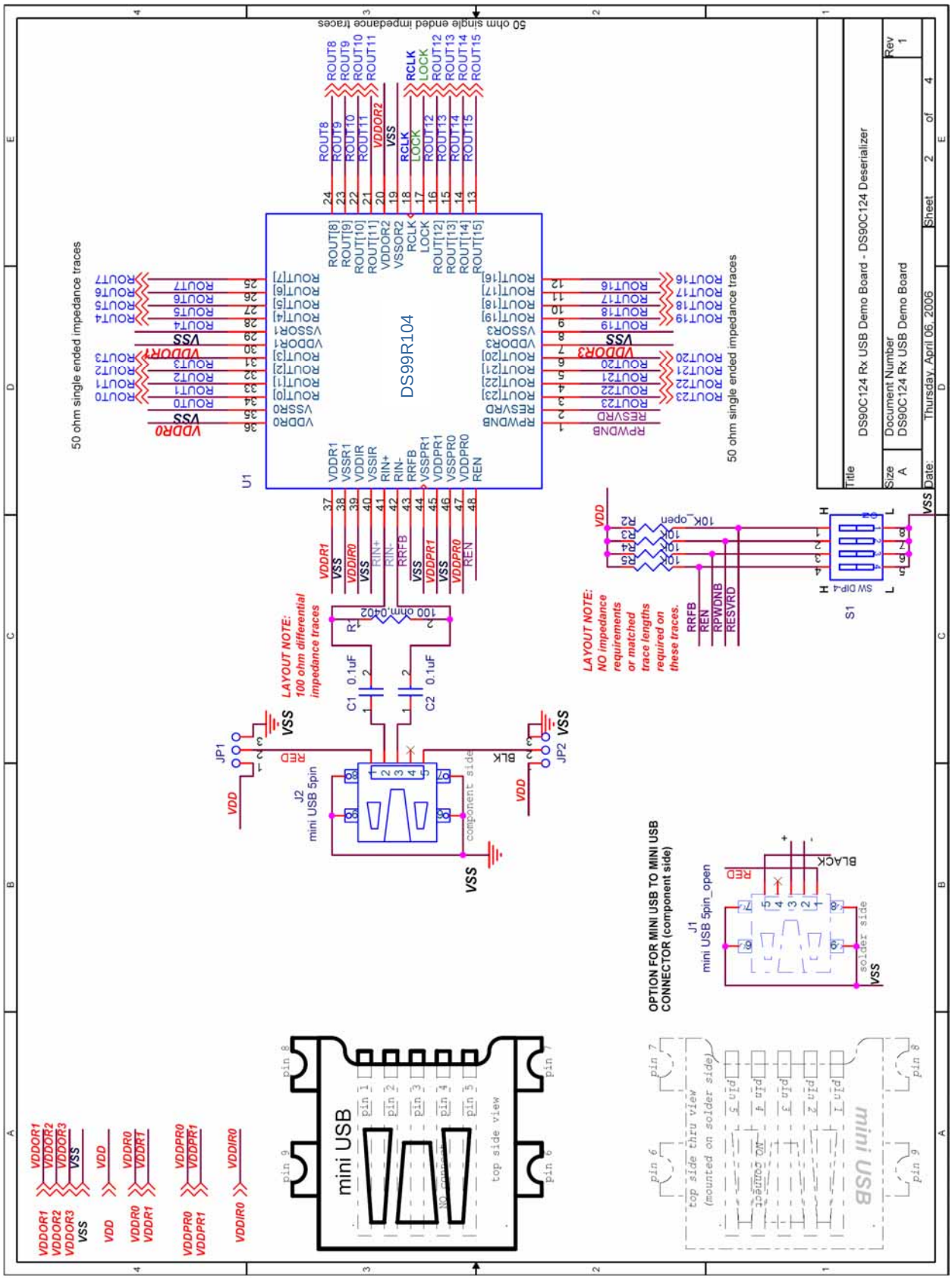

DS99R103
U1
USB A
P2
P1
JP1
JP2
JP3
VR1
SVR20K
C1
C2
0.1uF
R26
5.76K 0402
R27
100 ohm 0402
S1
SW DIP-8
mini USB 5pin_open
OPTION FOR MINI USB TO MINI USB CONNECTOR (component side)
power wire in USB cable
LAYOUT NOTE: 100 ohm differential impedance traces
LAYOUT NOTE: NO impedance requirements or matched trace lengths required on these traces.
50 ohm single ended impedance traces
Title
DS90C241 Tx USB Demo Board - DS90C241 Serializer
Document Number
DS90C241 Tx USB Demo Board
Rev
1
Sheet
2
of
4
Date:
Thursday, March 23, 2006
Size
A

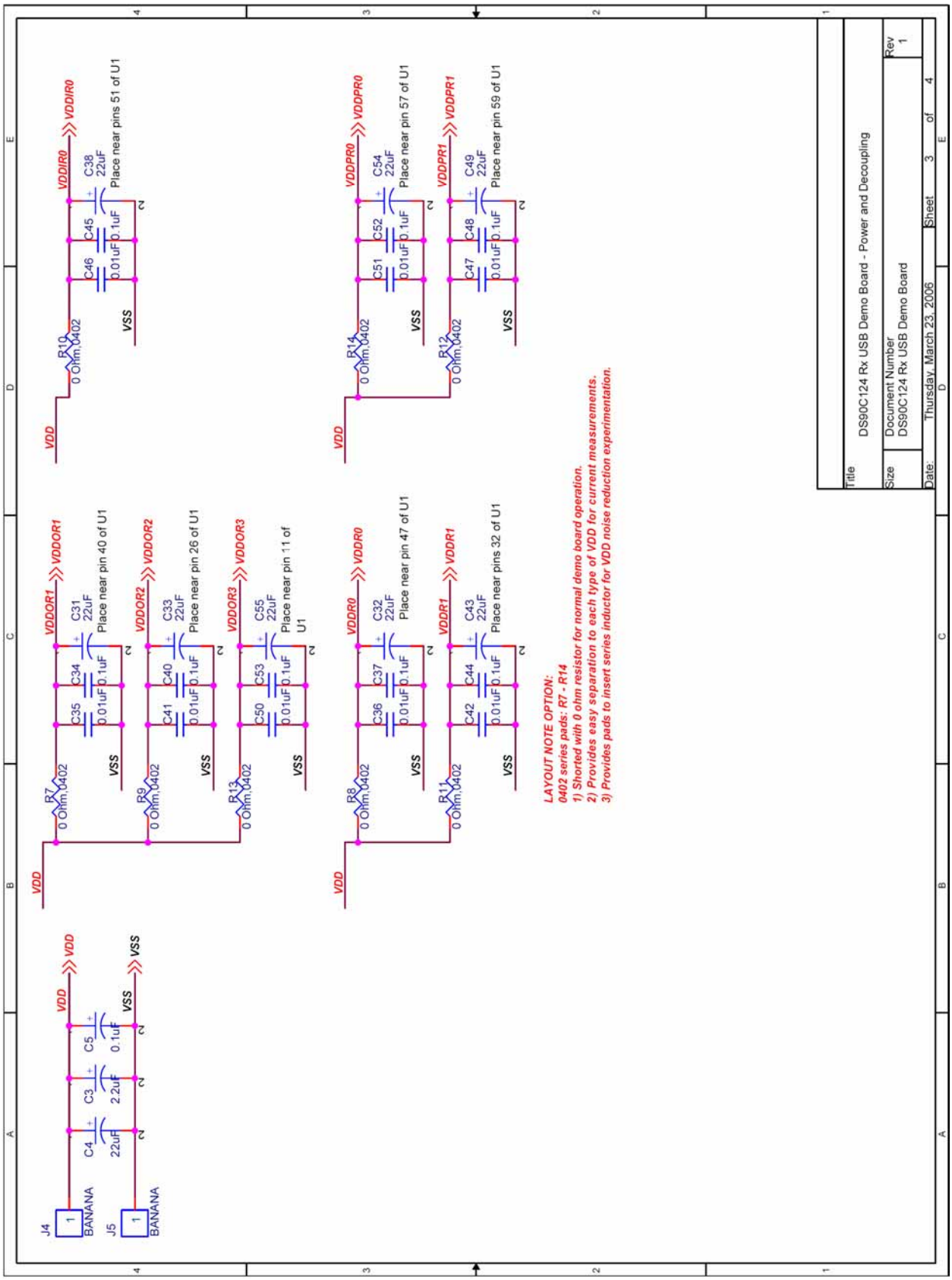

VDDL0
VDDPT0
VDDDR0
VDDIT0
VDDT0
VDD
VSS
R35 0 Ohm,0402
R33 0 Ohm,0402
R30 0 Ohm,0402
R32 0 Ohm,0402
R28 0 Ohm,0402
C20 22uF
C18 0.1uF
C19 0.01uF
C13 22uF
C14 0.1uF
C15 0.01uF
C10 22uF
C12 0.1uF
C11 0.01uF
C9 22uF
C17 0.1uF
C16 0.01uF
C6 22uF
C8 0.1uF
C7 0.01uF
Place near pins 7 of U1
Place near pin 14,16 of U1
Place near pin 22 of U1
Place near pin 42 of U1
Place near pins 30 of U1
J4 BANANA
J5 BANANA
C5 0.1uF
C3 2.2uF
C4 22uF
LAYOUT NOTE OPTION ON DEMO BOARD:
0402 series pads: R28, R30, R32, R33, R35
1) Shorted with 0 ohm resistor for normal demo board operation.
2) Provided for easy separation to each type of VDDs for IDD current measurements.
3) Provides pads to insert series inductor for each type of VDDs for noise reduction experimentation.
Title
DS90C241 Tx USB Demo Board - Power and Decoupling
Size
Document Number
DS90C241 Tx USB Demo Board
Rev
1
Date: Thursday, March 23, 2006
Sheet 3 of 4

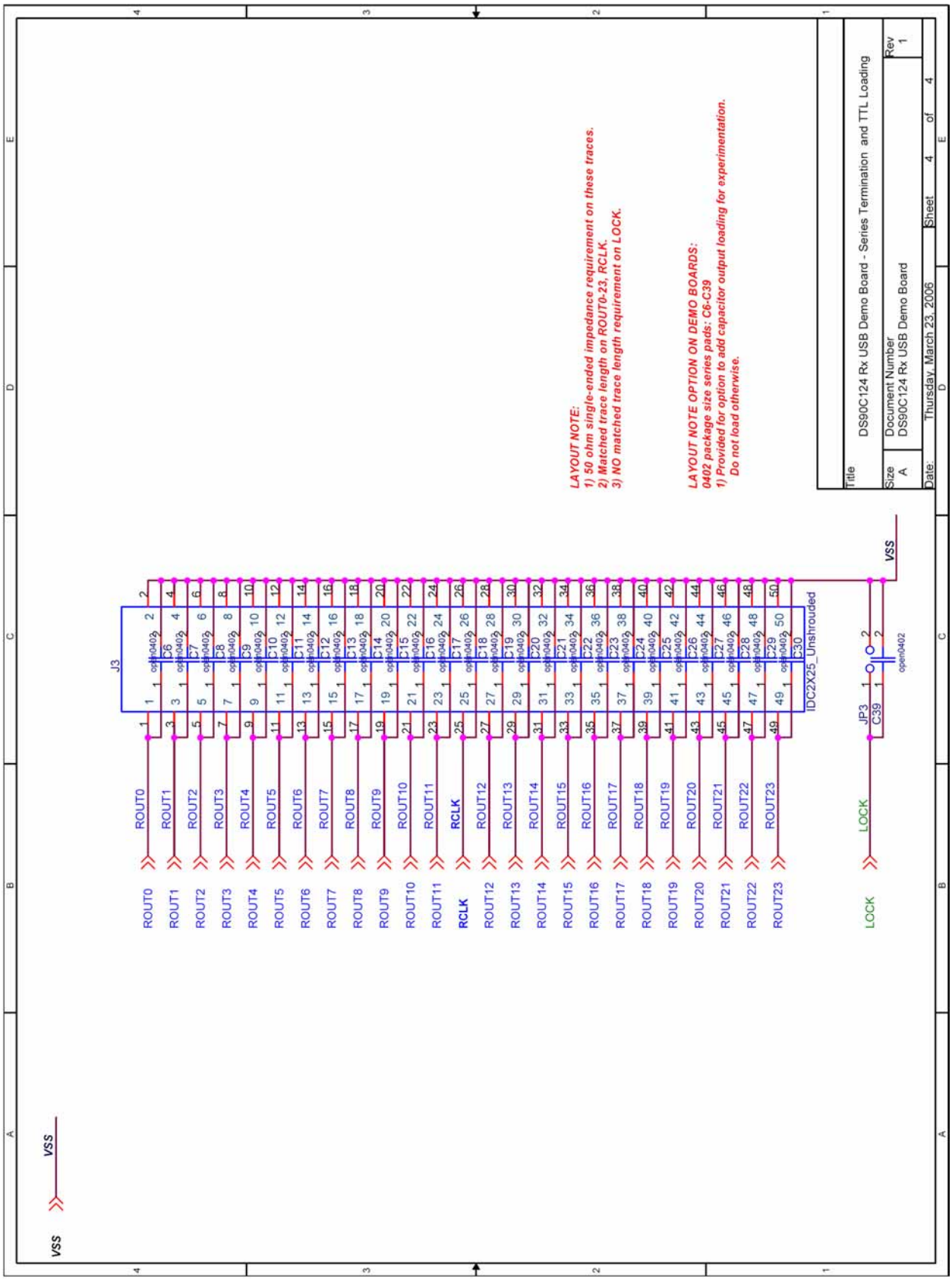

50 ohm single-ended impedance traces
DIN0
DIN1
DIN2
DIN3
DIN4
DIN5
DIN6
DIN7
DIN8
DIN9
DIN10
DIN11
DIN12
DIN13
DIN14
DIN15
DIN16
DIN17
DIN18
DIN19
DIN20
DIN21
DIN22
DIN23
TCLK
VSS
J1
IDC2X25_Unshrouded
0805
0201
49.9ohm_open
LAYOUT NOTE:
1) 50 ohm single-ended impedance requirement on these traces.
2) Matched trace length on DIN0-23, TCLK.
3) R1-R25 parallel 49.9 ohm termination option for 50 ohm driving source.
Do not load otherwise.
Title
DS90C241 Tx USB Demo Board - Parallel Output Loading
Size
A
Document Number
DS90C241 Tx USB Demo Board
Rev
1
Date:
Thursday, March 23, 2006
Sheet
3
of
4

De-serializer (Rx) PCB Schematic:

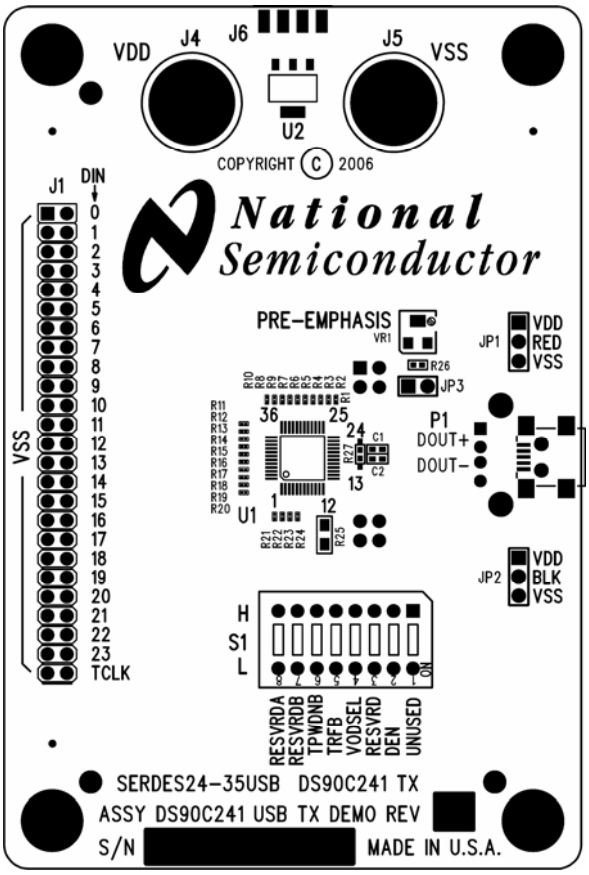



DS99R104
U1
50 ohm single ended impedance traces
50 ohm single ended impedance traces
LAYOUT NOTE:
100 ohm differential
impedance traces
LAYOUT NOTE:
NO impedance
requirements
or matched
trace lengths
required on
these traces.
OPTION FOR MINI USB TO MINI USB
CONNECTOR (component side)
mini USB
top side view
top side thru view
(mounted on solder side)
component side
solder side
Title
DS90C124 Rx USB Demo Board - DS90C124 Deserializer
Document Number
DS90C124 Rx USB Demo Board
Thursday, April 06, 2006

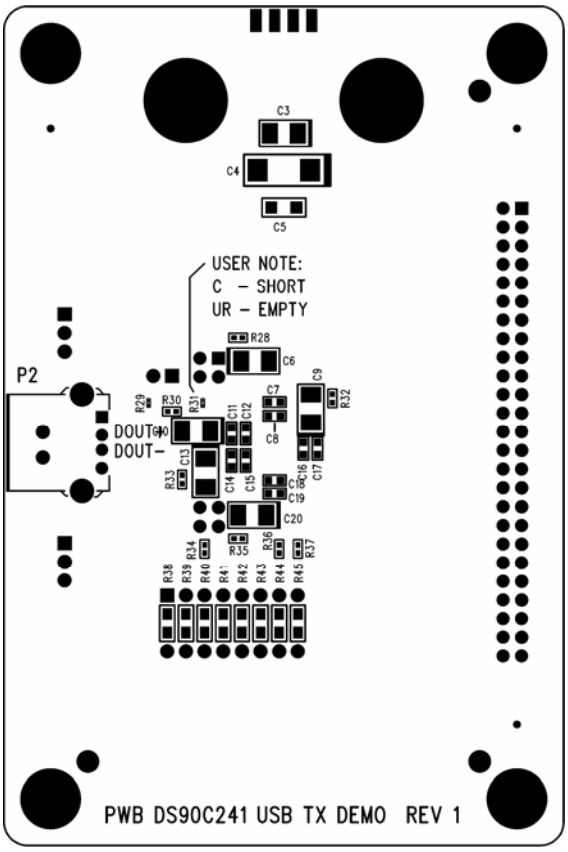

VDDIR0
C38 22uF Place near pins 51 of U1
C45 0.1uF
C46 0.01uF
R10 0 Ohm,0402
VDD
VSS
VDDPR0
C54 22uF Place near pin 57 of U1
C52 0.1uF
C51 0.01uF
R14 0 Ohm,0402
VDDPR1
C49 22uF Place near pin 59 of U1
C48 0.1uF
C47 0.01uF
R12 0 Ohm,0402
VDDOR1
C31 22uF Place near pin 40 of U1
C34 0.1uF
C35 0.01uF
R7 0 Ohm,0402
VDDOR2
C33 22uF Place near pin 26 of U1
C40 0.1uF
C41 0.01uF
R9 0 Ohm,0402
VDDOR3
C55 22uF Place near pin 11 of U1
C53 0.1uF
C50 0.01uF
R13 0 Ohm,0402
VDDR0
C32 22uF Place near pin 47 of U1
C37 0.1uF
C36 0.01uF
R8 0 Ohm,0402
VDDR1
C43 22uF Place near pins 32 of U1
C44 0.1uF
C42 0.01uF
R11 0 Ohm,0402
J4 BANANA
J5 BANANA
C5 0.1uF
C3 2.2uF
C4 22uF
LAYOUT NOTE OPTION:
0402 series pads: R7 - R14
1) Shorted with 0 ohm resistor for normal demo board operation.
2) Provides easy separation to each type of VDD for current measurements.
3) Provides pads to insert series inductor for VDD noise reduction experimentation.
Title
DS90C124 Rx USB Demo Board - Power and Decoupling
Size
Document Number
DS90C124 Rx USB Demo Board
Rev 1
Date: Thursday, March 23, 2006
Sheet 3 of 4


LAYOUT NOTE:
1) 50 ohm single-ended impedance requirement on these traces.
2) Matched trace length on ROUT0-23, RCLK.
3) NO matched trace length requirement on LOCK.
LAYOUT NOTE OPTION ON DEMO BOARDS:
0402 package size series pads: C6-C39
1) Provided for option to add capacitor output loading for experimentation.
Do not load otherwise.
Title
DS90C124 Rx USB Demo Board - Series Termination and TTL Loading
Size
A
Document Number
DS90C124 Rx USB Demo Board
Rev
1
Date:
Thursday, March 23, 2006
Sheet
4
of
4
J3
IDC2X25_Unshrouded
ROUT0
ROUT1
ROUT2
ROUT3
ROUT4
ROUT5
ROUT6
ROUT7
ROUT8
ROUT9
ROUT10
ROUT11
RCLK
ROUT12
ROUT13
ROUT14
ROUT15
ROUT16
ROUT17
ROUT18
ROUT19
ROUT20
ROUT21
ROUT22
ROUT23
LOCK
JP3
C39
open0402
VSS

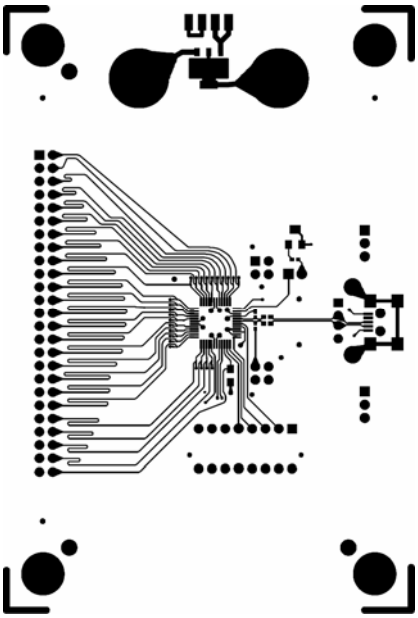
Serializer (Tx) PCB Layout:



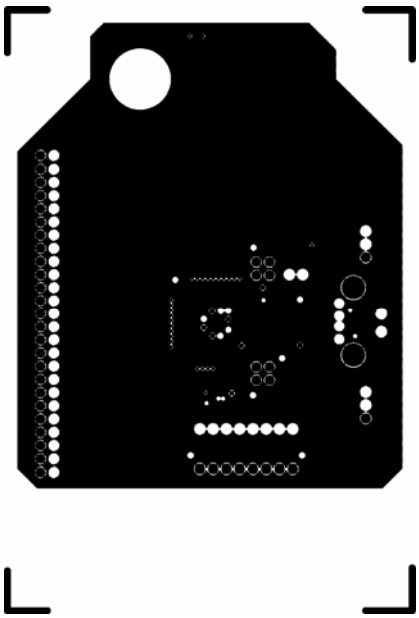
TOP VIEW



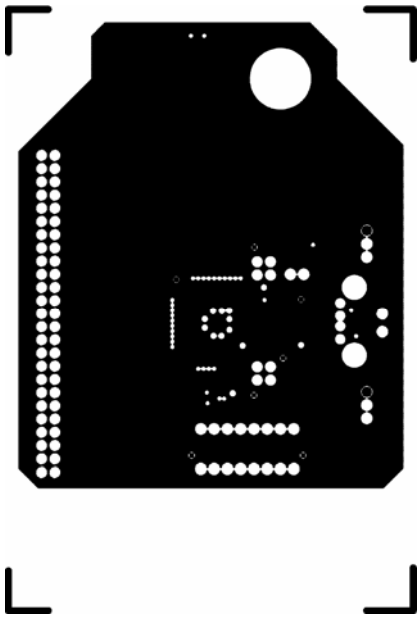
BOTTOMSIDE VIEW



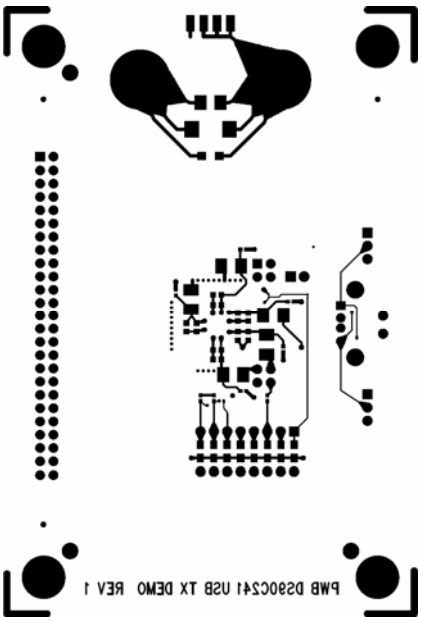
PRIMARY COMPONENT SIDE – LAYER 1



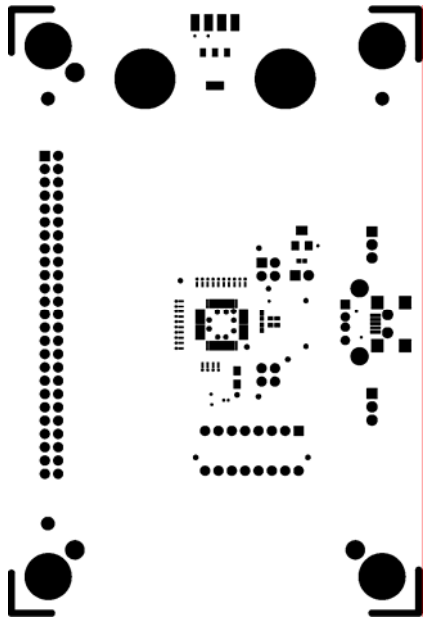
GROUND PLANE (VSS) – LAYER 2



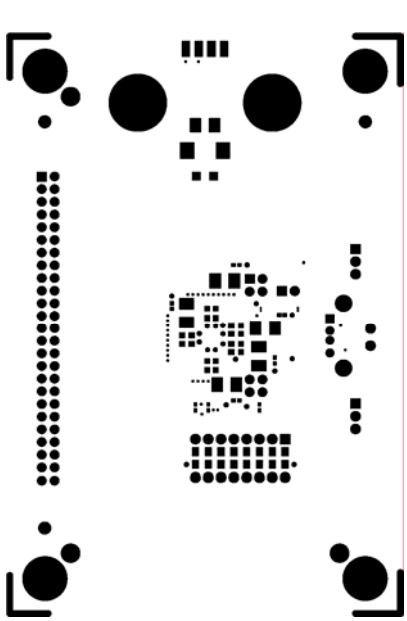
POWER PLANE (VDD) – LAYER 3



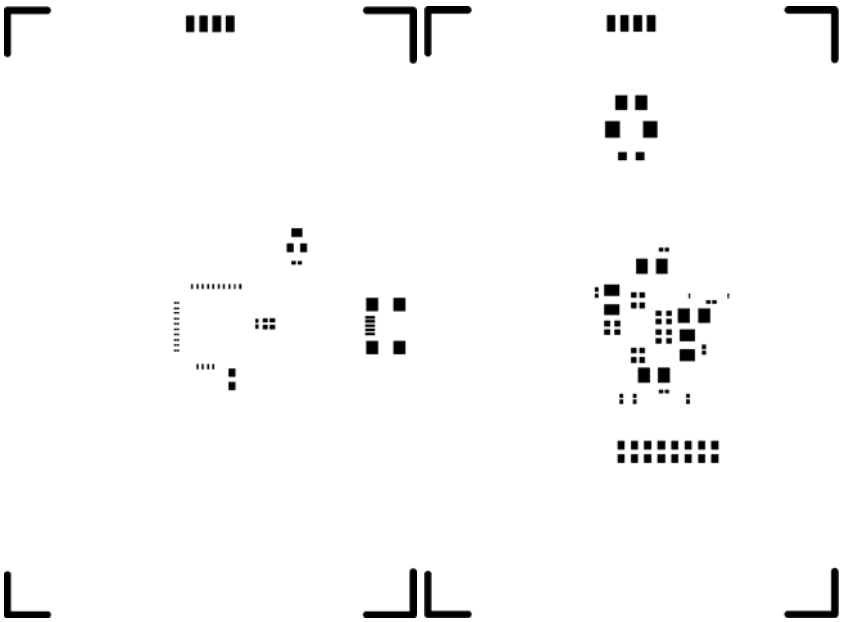
SECONDARY COMP SIDE – LAYER 4



PRIMARY COMP SIDE – SOLDER MASK (LAYER 1)

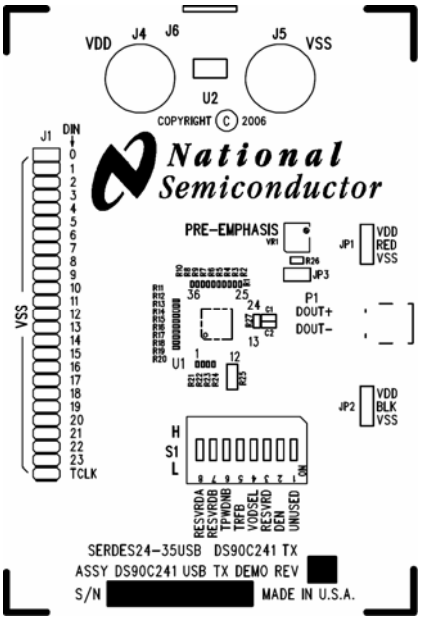


SECONDARY COMP SIDE – SOLDER MASK (LAYER 4)

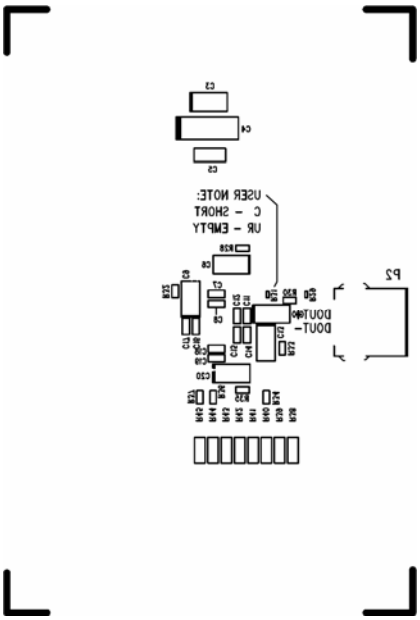


PRIMARY COMP SIDE – SOLDER PASTE (LAYER 1)

SECONDARY COMP SIDE – SOLDER PASTE (LAYER 4)

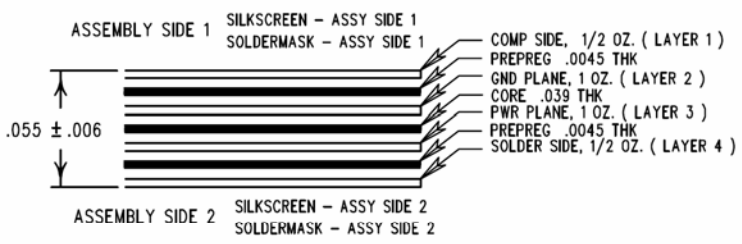


PRIMARY COMP SIDE – SILKSCREEN (LAYER 1)

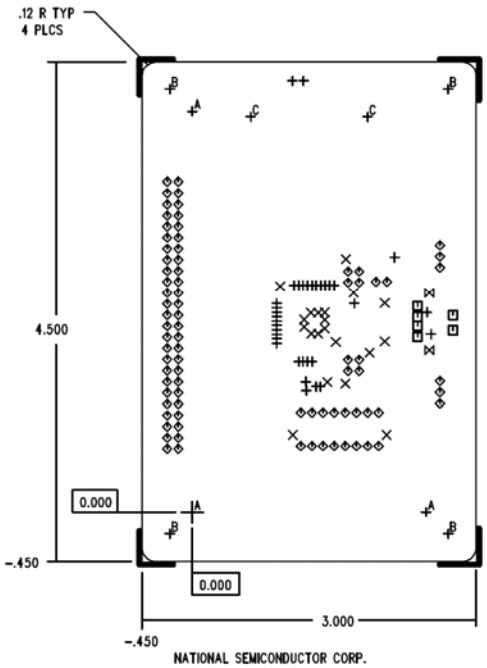


SILKSCREEN COMP SIDE – SILKSCREEN (LAYER 4)

Serializer (Tx) PCB Stackup:



HOLE CHART				
CODE	SIZE	QTY	PLATED	TOL
+	0.006	34	YES	± .003
×	0.014	20	YES	± .003
□	0.036	6	YES	± .003
◇	0.043	82	YES	± .003
⋈	0.091	2	YES	± .003
A	0.125	3	NO	+.003 – .000
B	0.156	4	YES	± .004
C	0.265	2	YES	± .005

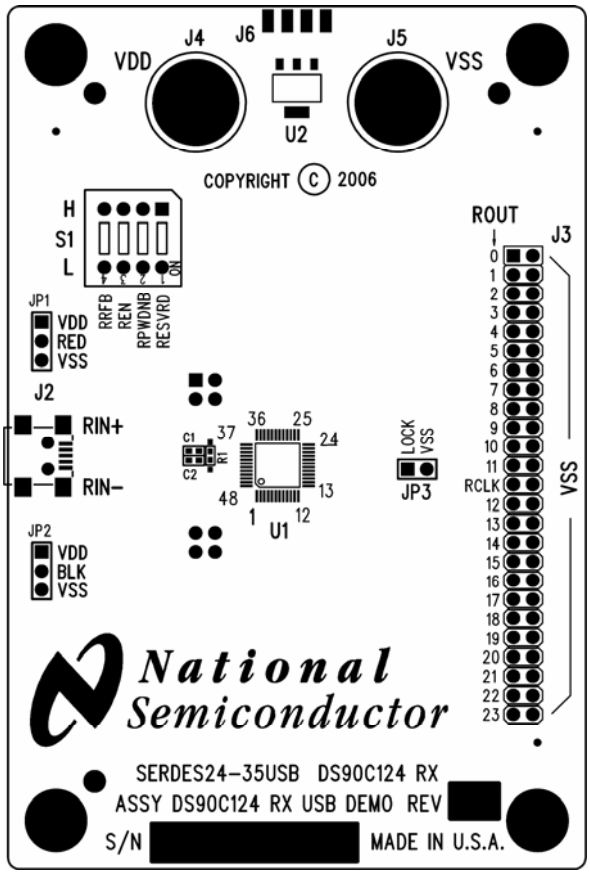


NATIONAL SEMICONDUCTOR CORP.
DS90C241 USB TX DEMO BOARD
PWB DS90C241 USB TX DEMO REV 1
DRILL DRAWING

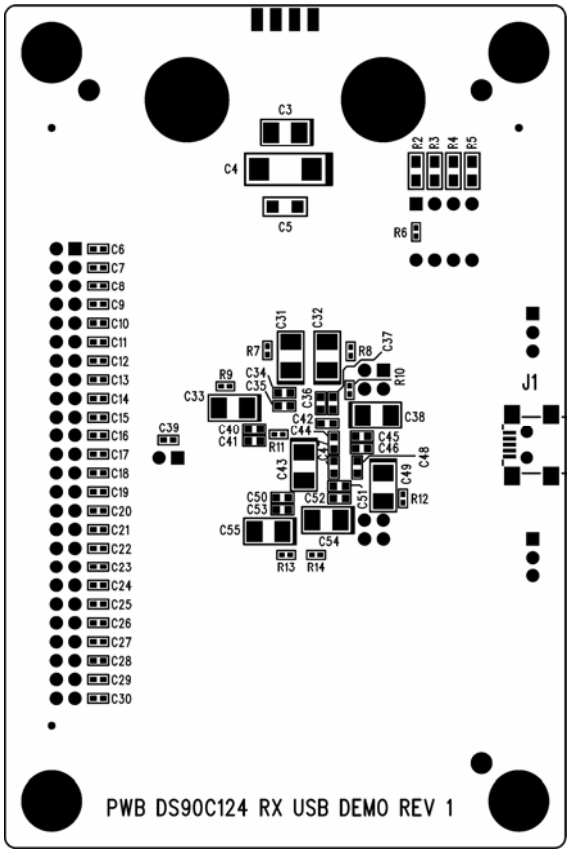
NOTES: UNLESS OTHERWISE SPECIFIED

1. PRIMARY COMPONENT SIDE IS SHOWN.
2. HOLES MARKED " A " ARE TOOLING HOLES, UNPLATED, AND SHALL BE "ONCE" DRILLED.
3. FABRICATE USING MASTER FILM DS90C241 USB TX DEMO REV 1. USE GERBER FILE A457B0A.PHO FOR BOARD ROUTE.
4. ACCEPTABILITY SHALL BE BASED ON IPC-A-600, CLASS 2
5. MATERIAL: BASE MATERIAL IS NEMAL-1 GRADE FR-406, COLOR GREEN, 0.062 INCH NOM. THICKNESS. COPPER CLADDING SHALL BE 1/2 OZ FOR OUTSIDE LAYERS AND 1 OZ FOR INSIDE LAYERS.
6. PLATING: ALL HOLES AND CONDUCTIVE SURFACES SHALL BE PLATED WITH A MIN. OF .001 INCH COPPER.
   SURFACE FINISH: GOLD FLASH .000004 MIN.
7. FABRICATION TOLERANCES:
   END PRODUCT CONDUCTOR WIDTHS AND LAND DIAMETERS SHALL NOT VARY MORE THAN .002 INCH FROM THE 1:1 DIMENSIONS OF THE MASTER PATTERN. THE CONDUCTIVE PATTERN SHALL BE POSITIONED SO THAT THE LOCATION OF ANY LAND SHALL BE WITHIN .010 INCH DIAMETER TO THE TRUE POSITION OF THE HOLE IT CIRCUMSCRIBES THE MINIMUM ANNULAR RING SHALL BE .002 INCH. BOW AND TWIST SHALL NOT EXCEED .010 INCH PER INCH.
8. SOLDERMASK BOTH SIDES PER IPC-SM-840, TYPE A, CLASS B. COLOR-GREEN. THERE SHALL BE NO SOLDERMASK ON ANY LAND.
9. SILKSCREEN THE LEGEND ON BOTH SIDES USING NON CONDUCTIVE EPOXY INK, COLOR-WHITE. THERE SHALL BE NO INK ON ANY LAND.
10. THE .008 TRACES (LAYER 1) TO BE 50 OHM SINGLE ENDED IMPEDANCE THE .007 TRACES (LAYER 1) TO BE 100 OHM DIFFERENTIAL IMPEDANCE, AND THE DIELECTRIC REFERENCED IN BOARD STACK DETAIL IS SUGESTED. HOWEVER, TRACE WIDTHS AND OR DIELECTRIC THICKNESS MAY BE MICRO-MODIFIED IN ORDER TO FABRICATE BOARDS TO THE REQUIRED IMPEDANCE NOMINALS TO A TOLERANCE OF +/- 5%.
11. BOARD TO BE FABRICATED IN COMPLIANCY TO ROHS REQUIREMENTS.

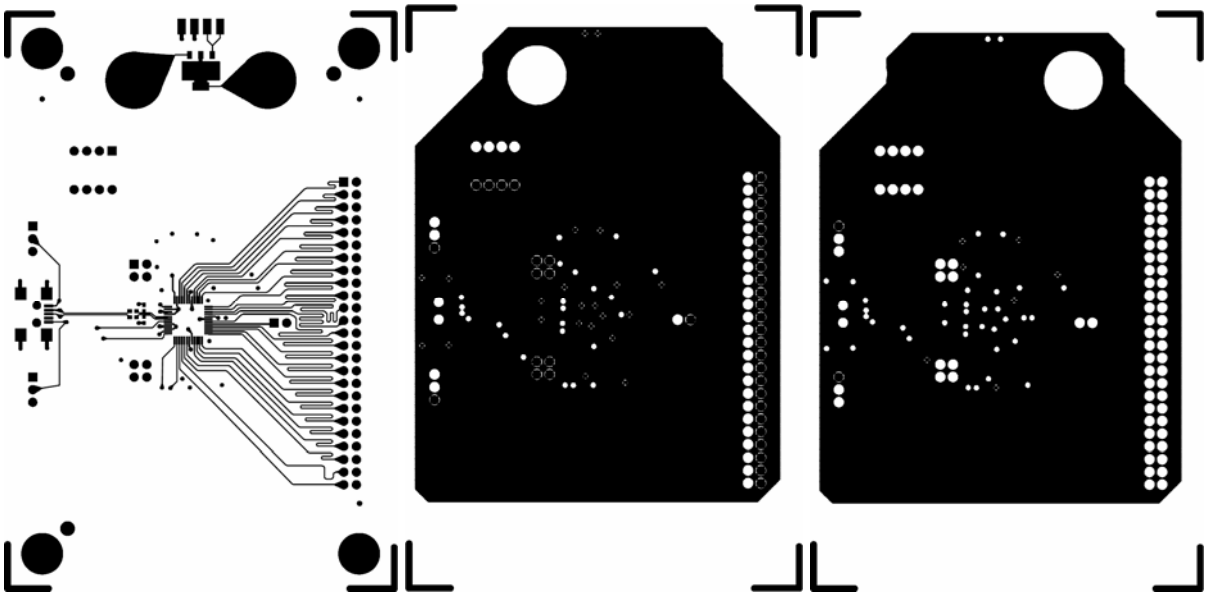
Deserializer (Rx) PCB Layout:



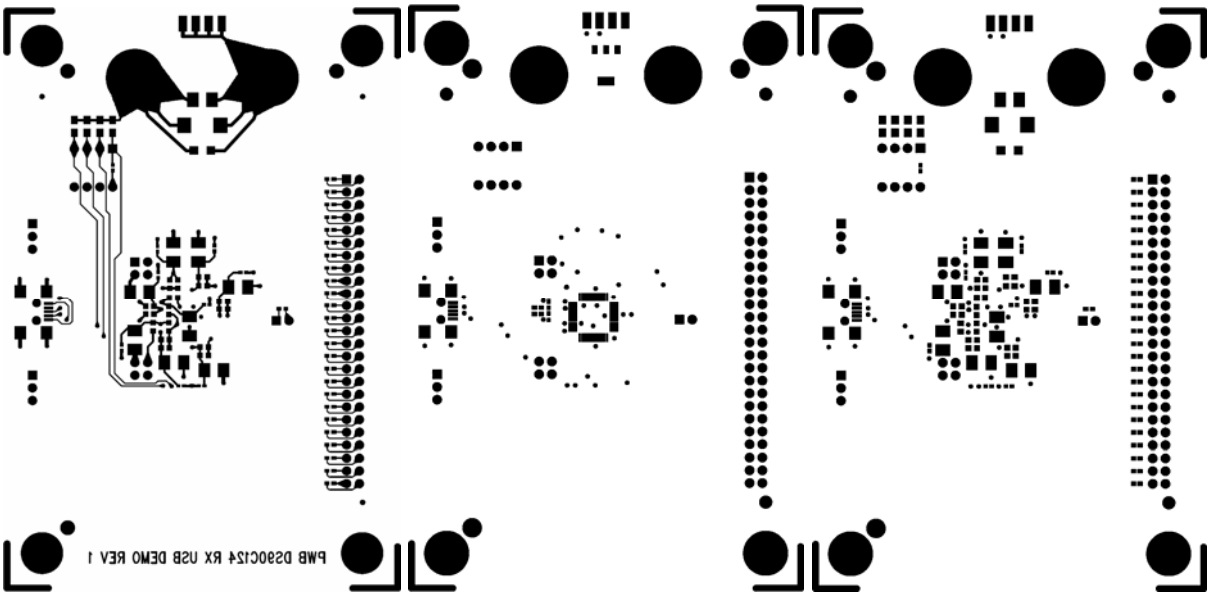
TOP VIEW



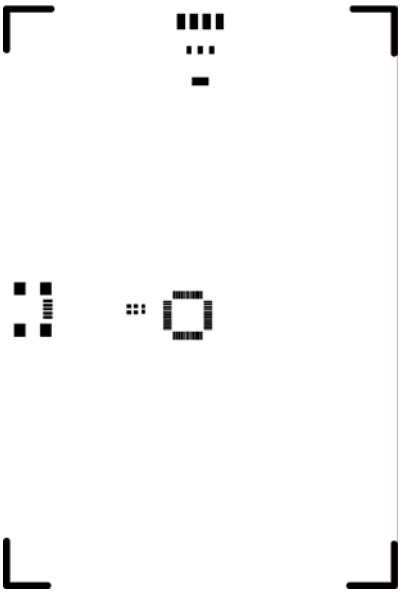
BOTTOMSIDE VIEW



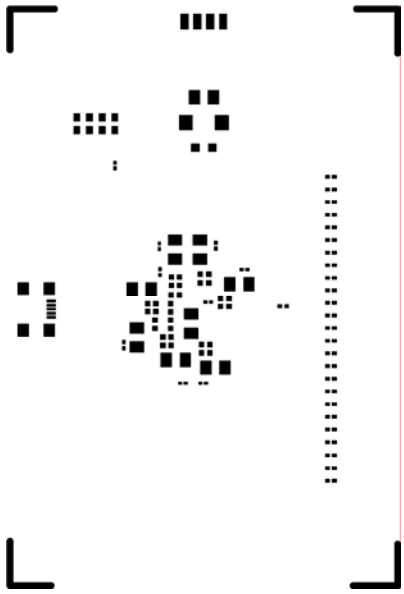
PRIMARY COMPONENT SIDE – LAYER 1 GROUND PLANE (VSS) – LAYER 2 POWER PLANE (VDD) – LAYER 3



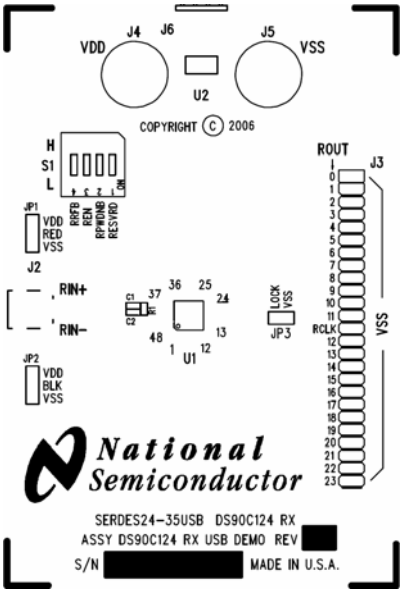
SECONDARY COMP SIDE – LAYER 4 PRIMARY COMP SIDE – SOLDER MASK (LAYER 1) SECONDARY COMP SIDE – SOLDER MASK (LAYER 4)



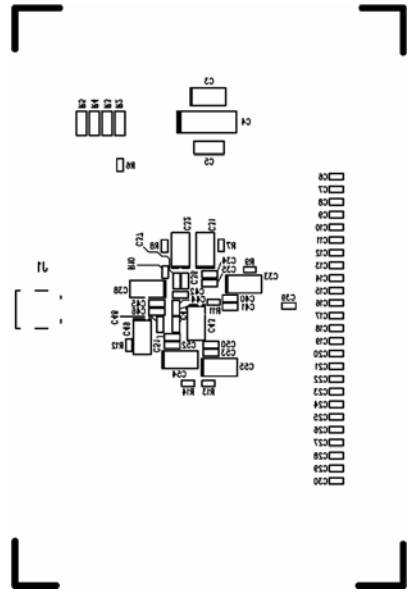
PRIMARY COMP SIDE – SOLDER PASTE (LAYER 1)



SECONDARY COMP SIDE – SOLDER PASTE (LAYER 4)

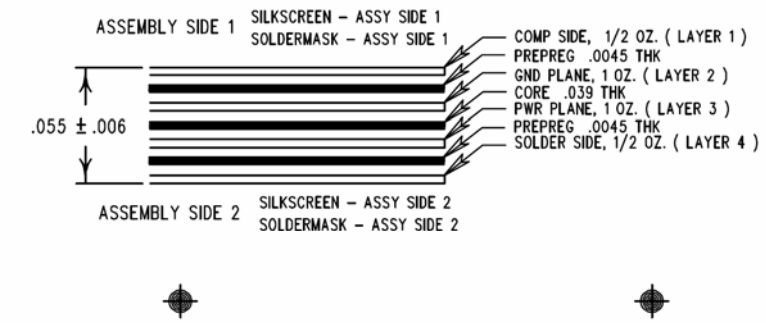


PRIMARY COMP SIDE – SILKSCREEN (LAYER 1)

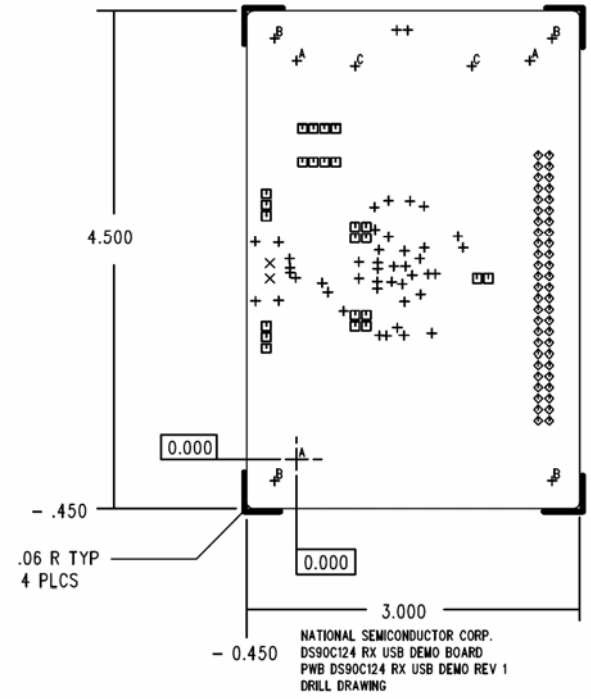


SILKSCREEN COMP SIDE – SILKSCREEN (LAYER 4)

Deserializer (Rx) PCB Stackup:



HOLE CHART				
CODE	SIZE	QTY	PLATED	TOL
+	0.012	45	YES	± .003
×	0.035	2	YES	± .003
□	0.040	24	YES	± .003
◇	0.045	50	YES	± .003
A	0.125	3	NO	+ .003 – .000
B	0.156	4	YES	± .005
C	0.265	2	YES	± .005



NOTES: UNLESS OTHERWISE SPECIFIED

1. PRIMARY COMPONENT SIDE IS SHOWN.
2. HOLES MARKED " A " ARE TOOLING HOLES, UNPLATED, AND SHALL BE "ONCE" DRILLED.
3. FABRICATE USING MASTER FILM DS90C124 RX USB DEMO REV 1. USE BOARD OUTLINE FILE A459BOA.PHO FOR BOARD ROUTE.
4. ACCEPTABILITY SHALL BE BASED ON IPC–A–600, CLASS 2
5. MATERIAL: BASE MATERIAL IS NEMAL–1 GRADE FR–406, COLOR GREEN, 0.062 INCH NOM. THICKNESS. COPPER CLADDING SHALL BE 1/2 OZ. OUTSIDE LAYERS AND 1 OZ INSIDE LAYERS.
6. PLATING: ALL HOLES AND CONDUCTIVE SURFACES SHALL BE PLATED WITH A MIN. OF .001 INCH COPPER. GOLD FLASH .000005 MIN.
7. FABRICATION TOLERANCES:
   END PRODUCT CONDUCTOR WIDTHS AND LAND DIAMETERS SHALL NOT VARY MORE THAN .003 INCH FROM THE 1:1 DIMENSIONS OF THE MASTER PATTERN. THE CONDUCTIVE PATTERN SHALL BE POSITIONED SO THAT THE LOCATION OF ANY LAND SHALL BE WITHIN .010 INCH DIAMETER TO THE TRUE POSITION OF THE HOLE IT CIRCUMSCRIBES THE MINIMUM ANNULAR RING SHALL BE .002 INCH. BOW AND TWIST SHALL NOT EXCEED .010 INCH PER INCH.
8. SOLDERMASK BOTH SIDES PER IPC–SM–840, TYPE A, CLASS B. COLOR–GREEN. THERE SHALL BE NO SOLDERMASK ON ANY LAND.
9. SILKSCREEN THE LEGEND ON BOTH SIDES USING NON CONDUCTIVE EPOXY INK, COLOR–WHITE. THERE SHALL BE NO INK ON ANY LAND.
10. THE .008 TRACES (LAYER 1) TO BE 50 OHM SINGLE ENDED IMPEDANCE AND THE .007 TRACES (LAYER 1) TO BE 100 OHM DIFFERENTAIL IMPEDANCE AND THE DIELECTRIC REFERENCED IN BOARD STACK DETAIL IS SUGGESTED. HOWEVER, TRACE WIDTHS AND OR DIELECTRIC THICKNESS MAY BE MICRO–MODIFIED IN ORDER TO FABRICATE BOARDS TO THE REQUIRED IMPEDANCE NOMINALS TO A TOLERANCE OF +/– 5%.
11. BOARD TO BE FABRICATED IN COMPLIANCY TO ROHS REQUIREMENTS.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265