FPD to Serdes (UR) Translator Chip
DS99R421
Evaluation Kit

User's Manual

NSID: FPDXSDUR-43USB

Rev 0.0

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Introduction:

National Semiconductor's DS99R421 standard multi-channel LVDS to FPD-LinkII translator SERDES evaluation kit contains 1 - DS99R421 translator board and 1 - DS90UR124 De-serializer (Rx) board, and 1 - two (2) meter high speed USB 2.0 cable. *Note: the evaluation boards are not for EMI testing. The evaluation boards were designed for easy accessibility to device pins with tap points for monitoring or applying signals, additional pads for termination, loading, and multiple connector options.*

The DS99R421 and DS90UR124 chipset supports a variety of display and general purpose applications. The single LVDS (FPD-LinkII) interface is well-suited for any display system interface. Typical applications include: navigation displays, automated teller machines (ATMs), POS, video cameras, global positioning systems (GPS), portable equipment/instruments, factory automation, etc.

The DS99R421 can be used to take existing standard multi-channel LVDS and convert them to a single channel FPD-Link II format. DS99R421 can be used as a 21-bit general purpose LVDS translator used in conjunction with the DS90UR124 FPD-LinkII De-serializer chipset and transmit data at clocks speeds ranging from 5 to 43 MHz.

The DS99R421 LVDS to FPD-LinkII translator board accepts four (4) standard LVDS multi-channel LVDS input signals and converts them into a single serialized FPD-LinkII data pair with an embedded LVDS clock. The serial data stream toggles at 28 times the base clock rate with an input clock at up to 43 MHz. The maximum transmission rate for the FPD-LinkII line is 1.204Gbps.

The DS90UR124 de-serializer board accepts the FPD-LinkII serialized data stream with embedded clock and converts the serialized data back into parallel 3.3V_LVCMOS signals and clock. Note that NO reference clock is needed to prevent harmonic lock.

Suggested equipment to evaluate the chipset are: a standard LVDS signal source such as a video generator, or FPD or Channel Link or equivalent transmitter and/or word generator or pulse generator and oscilloscope with a bandwidth of at least 43 MHz will be needed.

The user needs to provide the standard multi-channel LVDS inputs to the FPD-LINKII translator and also provide a proper interface from the de-serializer output to an LCD panel or test equipment. The translator and de-serializer boards can also be used to evaluate device parameters. A cable conversion board or harness scramble may be necessary depending on type of cable/connector interface used on the input to the DS99R421 and to the output of the DS90UR124.

Example of suggested display setup:

1) video generator with an 18 bit data LVDS output
2) 18-bit LCD panel with a 3.3V_LVCMOS input interface.

Contents of the Evaluation Kit:

1) One DS99R421 LVDS to FPD-LinkII translator board
2) One DS90UR124 De-serializer board
3) One 2-meter high speed USB 2.0 cable (4-pin USB A to 5-pin mini USB)
4) Evaluation Kit Documentation (this manual)
5) DS99R421 and DS90UR241/124 Datasheet

SERDES Typical Application:

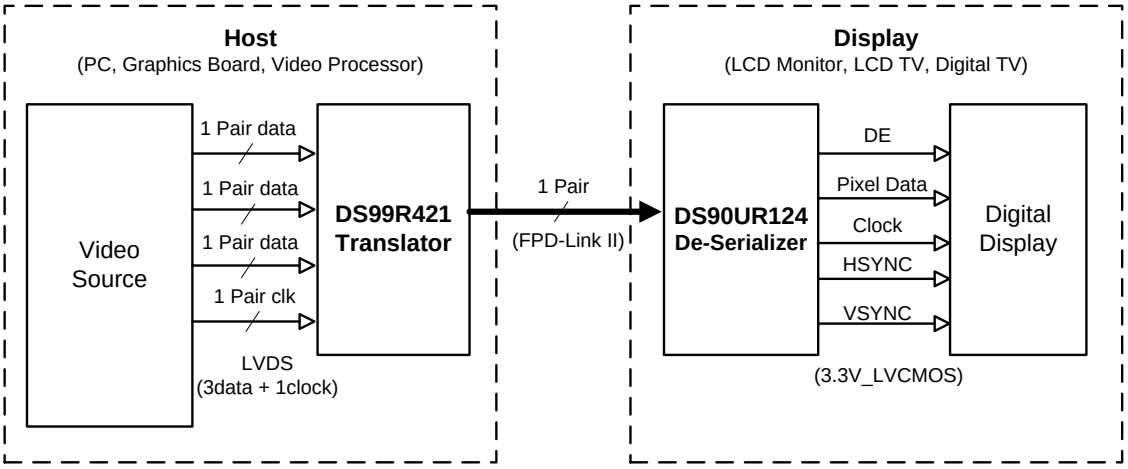


Figure 1a. Typical Application (18-bit RGB Color)

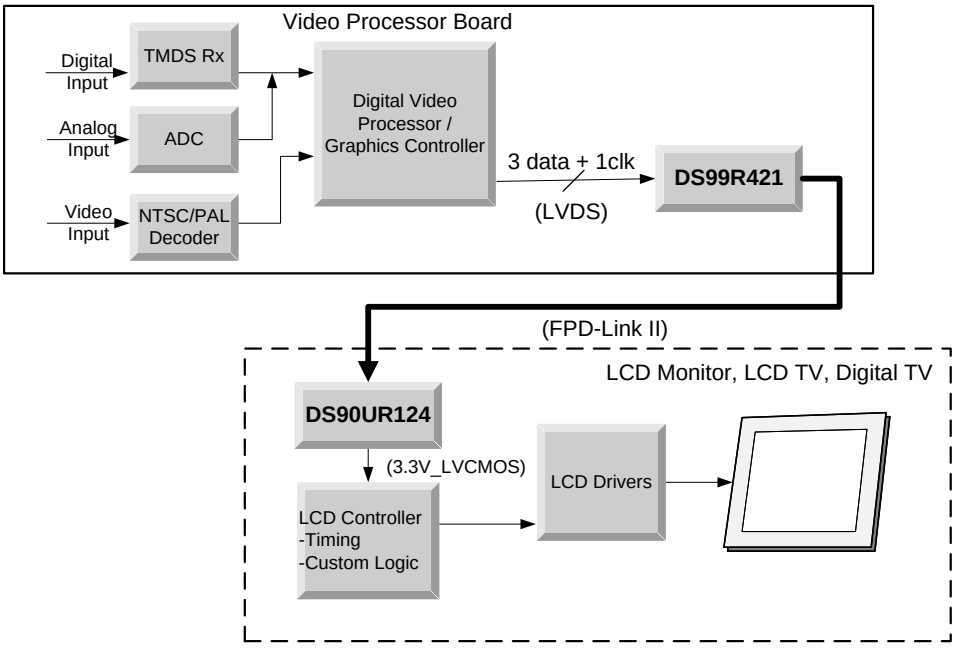


Figure 1b. Typical SERDES System Diagram

Figures 1a and 1b illustrate the use of the chipset (DS99R421/DS90UR124) in a Host to Flat Panel Interface.

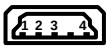
The chipsets support up to 18-bit color depth TFT LCD Panels.

Refer to the proper datasheet information on chipset provided on each board for more detailed information.

How to set up the Evaluation Kit:

The PCB routing for the translator LVDS input pins (RxIN) have been laid out to plug directly into FPD HSL Tx demo board (note only 6 bit mapping is used). The FPD-Link II TxOUT/RxIN (DOUT/RIN) interface uses a standard USB 2.0 connector/cable assembly. The PCB routing for the Rx output pins (ROUT) are accessed through a 50-pin IDC connector. Please follow these steps to set up the evaluation kit for bench testing and performance measurements:

1) A two (2) meter high speed USB 2.0 cable has been included in the kit. Connect the 4-pin USB A 

A side of cable harness to the DS99R421 board and the other side the 5-pin mini USB jack 

MIN to the DS90UR124 de-serializer board. This completes the FPD-Link II interface connection.
NOTE: The DS99R421 and DS90C124 are NOT USB compliant and should not be plugged into a USB device nor should a USB device be plugged into the evaluation boards.

2) Jumpers and switches have been configured at the factory; they should not require any changes for immediate operation of the chipset. See text on Configuration settings for more details. From the Video Decoder board, connect a flat cable (not supplied) to the translator board and connect another flat cable (not supplied) from the De-serializer board to the panel.

3) Power for the Tx and Rx boards must be supplied externally through Power Jack (VDD). Grounds for both boards are connected through Power Jack (VSS) (see section below).

Evaluation Board Power Connection:

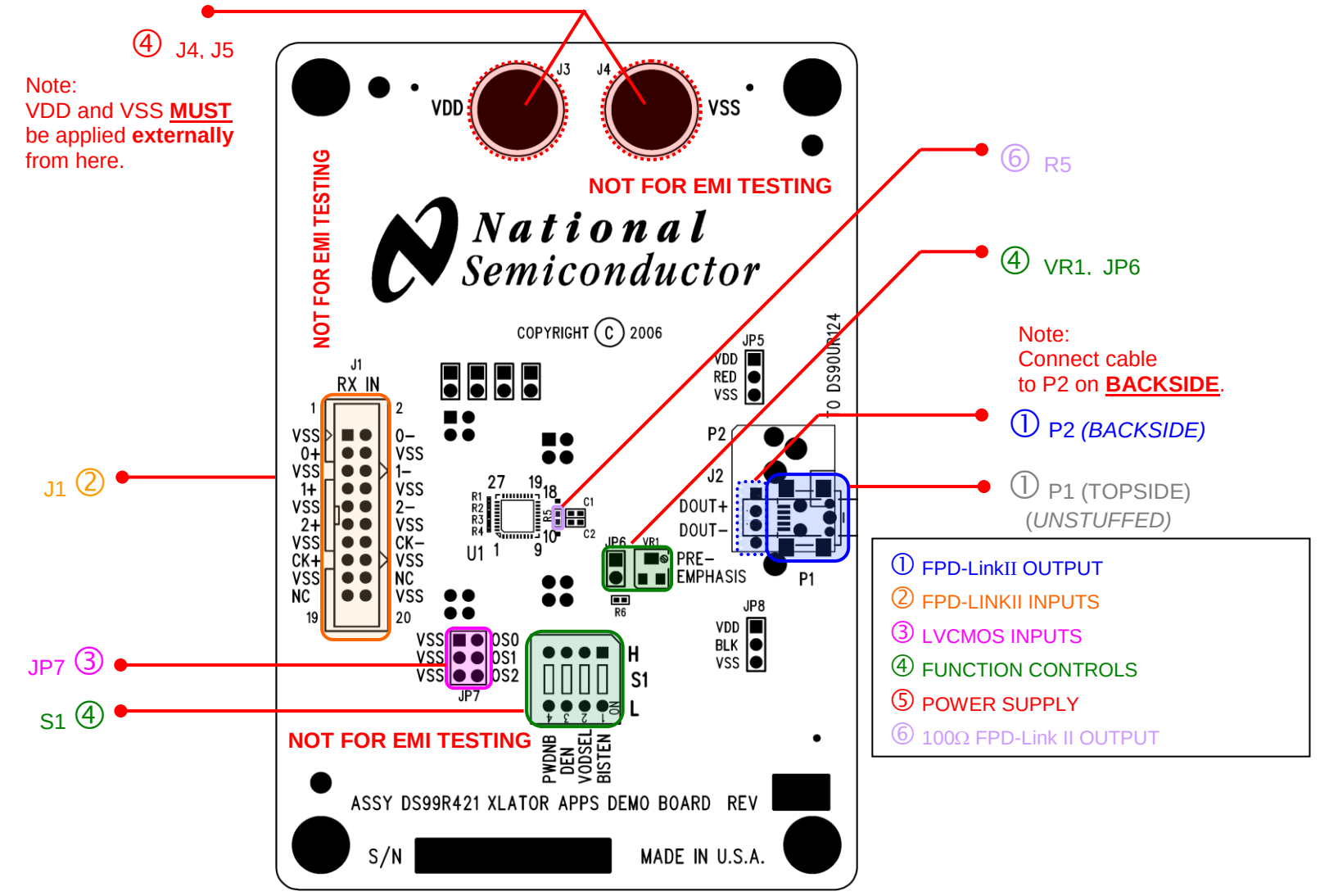
The translator and de-serializer boards must be powered by supplying power externally through J3 (VDD) and J4 (VSS) on the translator board and J4 (VDD) and J5 (VSS) on de-serializer board. Note +4V is the absolute MAXIMUM voltage (not operating voltage) that should ever be applied to the translator (DS99R421) or de-serializer (DS90UR124) VDD terminal. **Damage to the device(s) can result if the voltage maximum is exceeded.**

DS99R421 Translator Board Description:

The 20-pin IDC connector J1 accepts standard 18-bit 3-channels of LVDS RGB data (RxIN0+/-, RxIN1+/-, RxIN2+/-) and clock (RxCLK+/-). The 100 ohm terminations are integrated in the DS99R421 FPD-LINKII RxIN inputs so no external resistors are required.

The translator board is powered externally from the J3 (VDD) and J4 (VSS) connectors shown below. For the serializer to be operational, the Power Down (S1-PWDNB) and Data Enable (S1-DEN) switches on S1 must be set HIGH. The board is factory configured. JP1 and JP2 are configured from the factory to be shorted to VSS; these are the unused power wires in the cable harness.

The USB connector P2 (USB-A side) on the bottom side of the board provides the interface connection to the FPD-Link II signals to the De-serializer board. Note: P1 (mini USB) on the top side is un-stuffed and not to be used with the cable provided in the kit.



Configuration Settings for the Serializer Board

Table 1.

S1: Serializer Input Features Selection

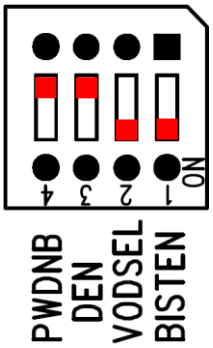
Reference	Description	Input = L	Input = H	S1
PWDNB	**P**o**W**er**D**ow**N** **B**ar	Powered Down	Normal operation **(Default)**	
DEN	Serializer Output **D**ata **EN**abled	Disabled	Enabled **(Default)**	
VODSEL	FPD-LINKII output **VOD SEL**ect	≈350mV **(Default)**	≈700mV	
BISTEN	**BIST EN**abled	BIST DISABLED MUST be low for normal operation **(Default)**	BIST ENABLED. *Note: DS90**UR**124 BISTEN MUST also be set High. (see datasheet for operational modes)*	

Table 2.

JP6,VR1: Pre-Emphasis Feature Selection

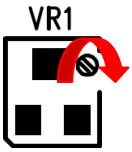
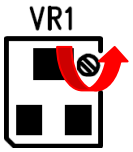
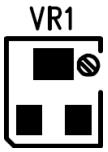
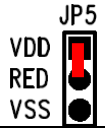
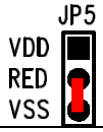
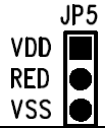
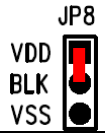
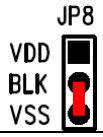
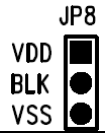
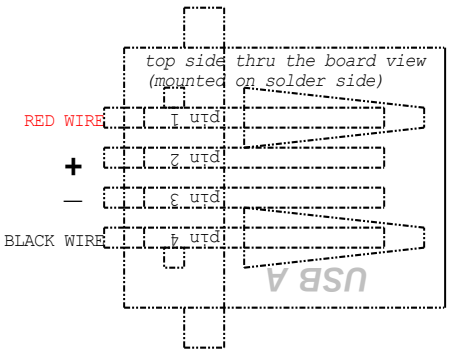
Reference	Description	OPEN (floating)	CLOSED (Path to GND)	
JP6	Pre-Emphasis – helps to increase the eye pattern opening in the FPD-LINKII stream	Disabled – no jumper **(Default)** 	Enabled – With jumper 	
JP6 & VR1	Pre-Emphasis adjustment (via screw) JP6 **MUST** have a jumper to use VR1 potentiometer. VR1 = 0Ω to 20KΩ, JP6 + VR1 + 6KΩ *(R6)* = ~6KΩ (maximum pre-emphasis) to ~26KΩ (minimum pre-emphasis*). $I_{PRE} = [1.2/(R_{PRE})] \times 40$, $R_{PRE\ (minimum)} \geq 6K\Omega$ **Note: maximum is based on resistor value. In this case ~26KΩ value is based on the ~6kΩ fixed resistor plus ~20KΩ maximum potentiometer value. User can use hundreds of Kohms to reduce the pre-emphasis value.*	Clockwise  increases R_{PRE} value which decreases pre-emphasis	Counter-Clockwise  decreases R_{PRE} value which increases pre-emphasis		
Pre-emphasis user note: Pre-emphasis must be adjusted correctly based on application frequency, cable quality, cable length, and connector quality. Maximum pre-emphasis should only be used under extreme worse case conditions; for example at the upper frequency specification of the part and/or low grade cables at maximum cable lengths. Typically all that is needed is minimum pre-emphasis. Users should start with no pre-emphasis first and gradually apply pre-emphasis until there is clock lock and no data errors. The best way to monitor the pre-emphasis effect is to hook up a differential probe to the 100Ω termination resistor (R1) on the DS90UR124 Rx demo board (NOT to R5 on the DS99R421 demo board). The reason for monitoring R1 on the Rx side is because you want to see what the receiver will see the attenuation signal AFTER the cable/connector.				

Table 3.

JP5, JP8: USB Red and Black wire

Reference	Description	VDD	VSS	OPEN
JP5	Power wire in USB cable thru P2 *(and P1 not mounted)* connector Jumper RED to VSS – recommended *Note: Normally VDD in USB application*	Red wire tied to VDD 	Red wire tied to VSS **(Default)** 	Red wire floating (not recommended) 
JP8	Power wire in USB cable thru P2 *(and P1 not mounted)* connector Jumper BLACK to VSS – recommended *Note: Normally VSS in USB application*	Black wire tied to VDD 	Black wire tied to VSS **(Default)** 	Black wire floating (not recommended) 
 **P2**				

Translator Input FPD-LINKII and Output FPD-Link II Pinout by IDC Connector

The following four tables illustrate how the LVDS and FPD-LINKII inputs are mapped to the IDC connector J1, the FPD-Link II outputs on the USB-A connector P3, and the mini USB P1 (not mounted) pinouts. There are also three (3) 3.3V_LVCMOS over-sampled bits OS1, OS2, OS3 (extra unused bits, not required for operation); see datasheet for description of these bits. Note – labels are also printed on the evaluation boards for both the LVDS input and FPD-Link II outputs.

LVDS INPUT	
J1 pin no.	**Symbol**
1	VSS
2	**RxIN0-**
3	**RxIN0+**
4	VSS
5	VSS
6	**RxIN1-**
7	**RxIN1+**
8	VSS
9	VSS
10	**RxIN2-**
11	**RxIN2+**
12	VSS
13	VSS
14	**RxCLKIN-**
15	**RxCLKIN+**
16	VSS
17	VSS
18	NC
19	NC
20	VSS

FPD-LinkII OUTPUT	
P3 pin no.	**Symbol**
1	RED
2	**DOUT+**
3	**DOUT-**
4	BLK

P1 (topside) (not mounted) FPD-LinkII OUTPUT	
pin no.	***name***
5	*JP2*
4	*NC*
3	***DOUT-***
2	***DOUT+***
1	*JP1*

OS INPUT (3.3v_LVCMOS)	
JP3 pin no.	**Symbol**
1	**OS1**
2	VSS
3	**OS2**
4	VSS
5	**OS3**
6	VSS

BOM (Bill of Materials) Translator PCB:

DS99R421 Xlator Bench Board - Board Stackup Revised: Friday, February 29, 2008
DS99R421 Xlator Bench Board Revision: 1
Bill Of Materials February 29,2008 18:31:46

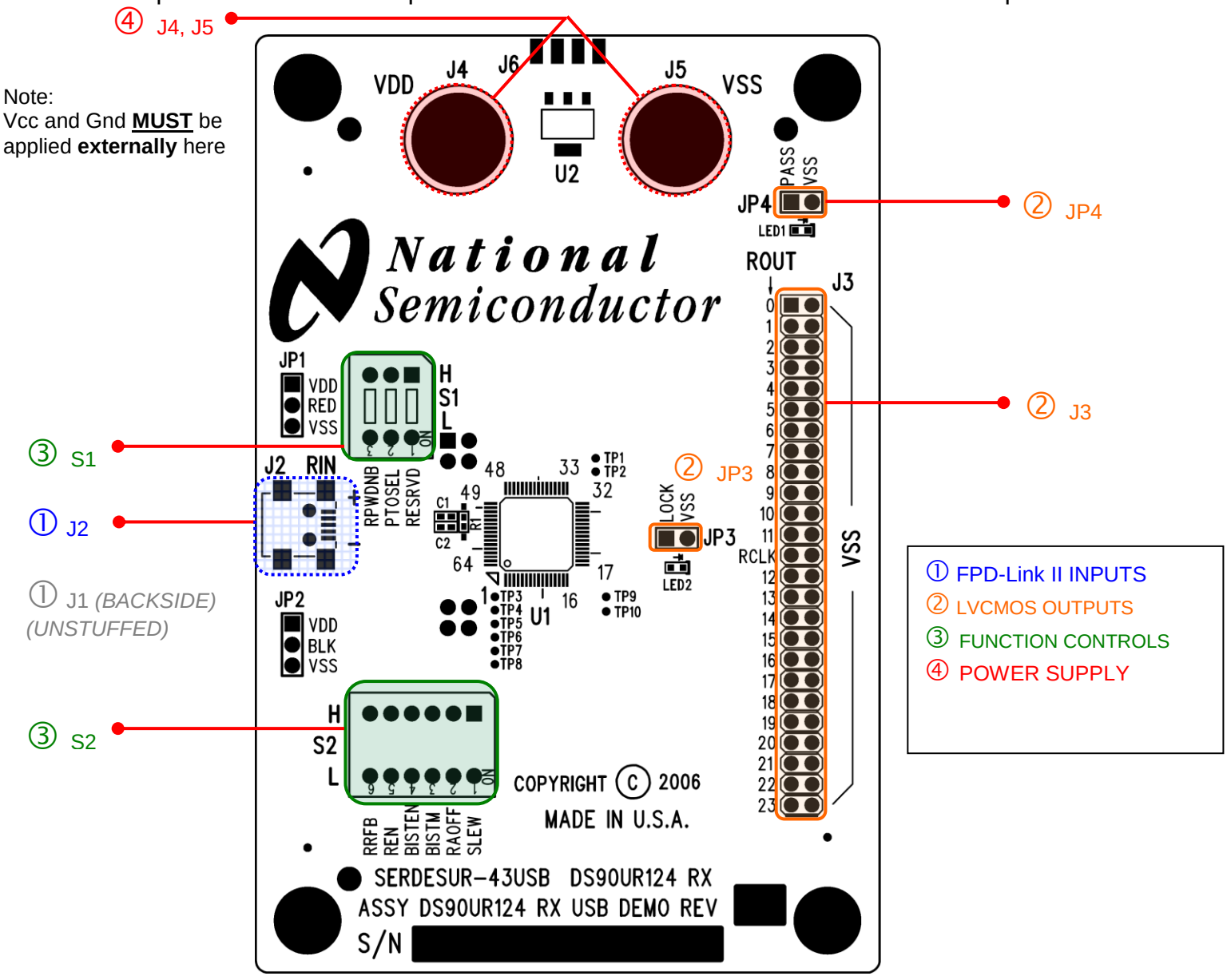
Item	Qty	Reference	Part	PCB Footprint
1	2	C1,C2	0.1uF	CAP/HDC-0402
2	1	C18	22uF	CAP/N
3	1	C19	2.2uF	3528-21_EIA
4	1	C20	0.1uF	CAP/HDC-1206
5	7	C21,C22,C23,C30,C33,C36, C41	22uF	CAP/EIA-B 3528-21
6	7	C24,C26,C28,C32,C35,C37, C40	0.1uF	CAP/HDC-0603
7	7	C25,C27,C29,C31,C34,C38, C39	0.01uF	CAP/HDC-0603
8	2	JP2,JP1	3-Pin Header	Header/3P
9	1	JP2	2-Pin Header	Header/2P
10	1	JP3	2X3-Pin Header	Header/2X3P
11	1	J1	2X10-Pin Header, open	Header/2X10P
12	1	J2	2mm_2X5	CON/HDR-10P-B
13	2	J5,J4	BANANA	CON/BANANA-S
14	1	P1	mini USB 5pin_open	mini_B_USB_surface_mount
15	1	P2	USB A	USB_TYPE_A_4P
16	1	R5	100 ohm,0402	RES/HDC-0402
17	1	R8	5.76K	RES/HDC-0402
18	7	R10,R11,R12,R13,R14,R15, R16	0 Ohm,0402	RES/HDC-0402
19	4	R18,R20,R21,R23	10K	RES/HDC-0805
20	1	S1	SW DIP-4	DIP-8
21	1	U1	DS99R421	36 ld LLP socket
22	1	VR1	SVR20K	Surface Mount 4mm Square
23	2	X2,X1	TP_0402	TP/0402

DS90UR124 Rx De-serializer Board:

The USB connector J2 (mini USB) on the topside of the board provides the interface connection for FPD-Link II signals to the Serializer board. Note: J1 (mini USB) on the bottom side is un-stuffed and not used with the cable provided in the kit.

The SERDES de-serializer board is powered externally from the J4 (VDD) and J5 (VSS) connectors shown below. For the de-serializer to be operational, the Power Down (RPWDNB) and Receiver Enable (REN) switches on S1 and S2 must be set HIGH. Rising or falling edge reference clock is also selected by S1: HIGH (rising) or LOW (falling).

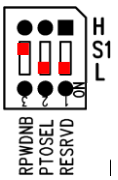
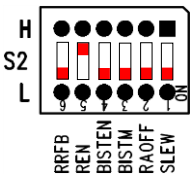
The 50 pin IDC Connector J3 provides access to the 24 bit LVCMOS and clock outputs.



Configuration Settings for the De-serializer Board

Table 4.

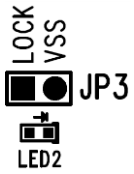
S1, S2: De-serializer Input Features Selection

Reference	Description	Input = L	Input = H	S1
RPWDNB	**P**o**W**er**D**ow**N** **B**ar	Power Down (Disabled)	Normal Operational **(Default)**	
PTOSEL	**P**rogressive **T**urn **O**n **SEL**ect	Enabled **(Default)**	Disabled	
RESRVD	**RES**e**RV**e**D**	Don't care	Don't care	
Reference	**Description**	**Input = L**	**Input = H**	**S2**
RRFB	Latch input data on **R**ising or **F**alling edge of TCLK	Falling Edge **(Default)**	Rising Edge	
REN	**R**eceiver Output Data **EN**abled	Disabled	Enabled **(Default)**	
BISTEN	**BIST EN**able *Note: MUST set DS99R421 BISTEN = H. Use in combination with BISTM pin.*	Normal Operating Mode, BIST Disabled **(Default)**	BIST Mode Enabled	
BISTM	**BIST M**ode Don't care if BISTEN=L. BISTEN MUST be High (enabled) for this pin to be functional.	Per Channel pass/fail; RxOUT[23:0] =H: pass; RxOUT[23:0] =H: fail	RxOUT[7:0]: binary error counting mode (up to 255 errors); RxOUT[23:8]: normal operation	
RAOFF	**RA**ndomizer **OFF**	Randomizer ON. **(Default)** *Note: DS99R421 RAOFF MUST also be set Low.*	Randomizer OFF. *Note: DS99R421 RAOFF MUST also be set High.*	
SLEW	**SLEW** rate control for ROUT[23:0] and RCLK	**(Default)**	~2X slew rate, ~2X drive strength	

Output Monitor Pins for the De-serializer Board

Table 5.

JP3: Output Lock Monitor

Reference	Description	Output = L	Output = H	JP3
LOCK	Receiver PLL **LOCK** **Note:** **DO NOT PUT A SHORTING JUMPER IN JP3.**	unlocked	PLL LOCKED (LED2 will illuminate) 	

JP4: PASS Monitor

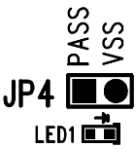
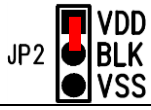
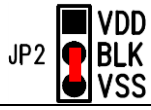
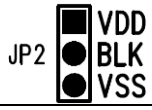
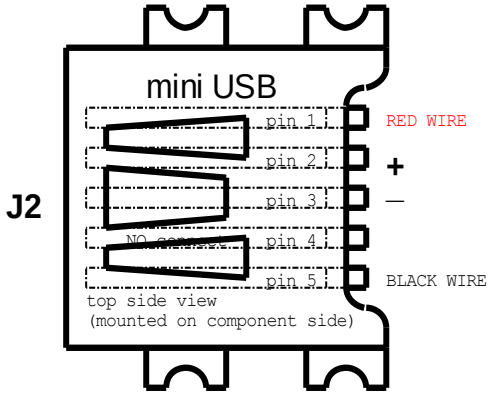
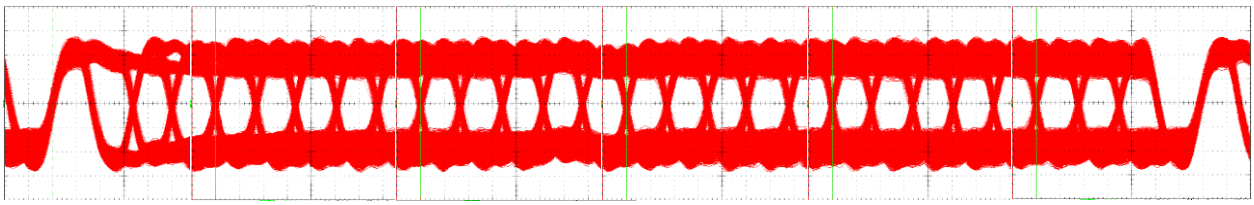
Reference	Description	Output = L	Output = H	JP4
PASS	Receiver BIST monitor **PASS** flag **Note:** **DO NOT PUT A SHORTING JUMPER IN JP1.**	FAIL	PASS (LED1 will illuminate) 	

Table 6.

JP1, JP2: USB Red and Black wire

Reference	Description	VDD	VSS	OPEN
JP1	Power wire in USB cable thru J2 *(and J1 not mounted)* connector Jumper RED to VSS – recommended *Note: Normally VDD in USB application*	Red wire tied to VDD 	Red wire tied to VSS **(Default)** 	Red wire floating (not recommended) 
JP2	Power wire in USB cable thru J2 *(and J1 not mounted)* connector Jumper BLACK to VSS – recommended *Note: Normally VSS in USB application*	Black wire tied to VDD 	Black wire tied to VSS **(Default)** 	Black wire floating (not recommended) 
				

The following picture depicts a typical example of the FPD-Link II serial stream. This snapshot was taken with a differential probe across the 100 ohm termination resistor R1 on the DS90UR124 Rx evaluation board. R1 is the termination resistor to the RxIN +/-. Note: The scope was triggered, with a separate probe, on TCLK, the input clock into the DS90UR241 Tx. To view the serial stream correctly, do not trigger on the probe monitoring the serial stream.



De-serializer FPD-LINKII Pinout and LVCMOS by IDC Connector

The following two tables illustrate how the FPD-LINKII inputs are mapped to the mini USB connector J2 and the Rx outputs are mapped to the IDC connector J3. Note – labels are also printed on the demo boards for both the FPD-LINKII inputs and LVCMOS outputs.

FPD-LINKII INPUT	
J2 pin no.	**Symbol**
1	RED
2	**DIN+**
3	**DIN-**
4	NC
5	BLK

LVCMOS OUTPUT	
J3 pin no.	**Symbol**
1	ROUT0
3	ROUT1
5	ROUT2
7	ROUT3
9	ROUT4
11	ROUT5
13	ROUT6
15	ROUT7
17	ROUT8
19	ROUT9
21	ROUT10
23	ROUT11
25	ROUT12
27	ROUT13
29	ROUT14
31	ROUT15
33	ROUT16
35	ROUT17
37	ROUT18
39	ROUT19
41	ROUT20
43	ROUT21
45	ROUT22
47	ROUT23
49	TCLK
all even pins	VSS

LVCMOS OUTPUT	
JP3 pin no.	**Symbol**
1	LOCK (PLL)
2	VSS

LVCMOS OUTPUT	
JP4 pin no.	**Symbol**
1	PASS (BIST)
2	VSS

BOM (Bill of Materials) De-serializer PCB:

DS90UR124 Rx USB Demo Board - Board Stackup Revised: Monday, October 23, 2006
DS90UR124 Rx USB Demo Board Revision: 1
Bill Of Materials October 23, 2006

Item	Qty	Reference	Part	PCB Footprint
1	2	C2,C1	0.1uF	CAP/HDC-0402
2	27	C3,C7,C8,C9,C10,C11,C12, C13,C14,C15,C16,C17,C18, C19,C20,C21,C22,C23,C24, C25,C26,C27,C28,C29,C30, C31,C42	open0402	CAP/HDC-0402
3	1	C4	2.2uF	3528-21_EIA
4	1	C5	22uF	CAP/N
5	1	C6	0.1uF	CAP/HDC-1206
6	8	C32,C33,C34,C41,C47,C50, C53,C54	22uF	CAP/EIA-B 3528-21
7	8	C35,C38,C40,C43,C46,C48, C52,C55	0.1uF	CAP/HDC-0603
8	8	C36,C37,C39,C44,C45,C49, C51,C56	0.01uF	CAP/HDC-0603
9	2	JP2,JP1	3-Pin Header	Header/3P
10	2	JP4,JP3	2-Pin Header_open	Header/2P
11	1	J1	mini USB 5pin_open	mini_USB_surface_mount
12	1	J2	Hirose GT17H-4P-2H	Hirose GT17H-4P-2H
13	1	J3	IDC2X25_Unshrouded	IDC-50
14	2	J4,J5	BANANA	CON/BANANA-S
15	1	LED1	0402_orange_LED	0402
16	1	LED2	0603_green_LED	0603 (Super Thin)
17	1	R1	100 ohm,0402	RES/HDC-0402
18	9	R2,R3,R4,R34,R35,R36,R37, R38,R39	10K	RES/HDC-0805
19	1	S1	SW DIP-3	DIP-6
20	1	S2	SW DIP-6	DIP-12
21	1	U1	DS90UR124	64 pin TQFP

Typical Connection and Test Equipment

The following is a list of typical test equipment that may be used to generate signals for the TX inputs:

1) Digital Video Source – for generation of specific display timing such as Digital Video Processor or Graphics Controller with 18-bit RGB LVDS output.
2) Astro Systems VG-835 - This video generator may be used for video signal sources for 18-bit RGB LVDS output.
3) Any other signal / video generator that generates the correct input levels as specified in the datasheet.
4) Optional – Logic Analyzer or Oscilloscope

The following is a list of typical test equipment that may be used to monitor the output signals from the RX:

1) LCD Display Panel which supports digital RGB (3.3V_LVCMOS) inputs.
2) National Semiconductor DS99R421 LVDS to FPD-Link II translator
3) Optional – Logic Analyzer or Oscilloscope
4) Any SCOPE with a bandwidth of at least 43MHz for LVCMOS and/or 2GHz for looking at the differential signal.

LVDS/ FPD-LinkII signals may be easily measured with high impedance / high bandwidth differential probes such as the TEK P6330 differential probes.

The picture below shows a typical test set up using a Graphics Controller and LCD Panel.

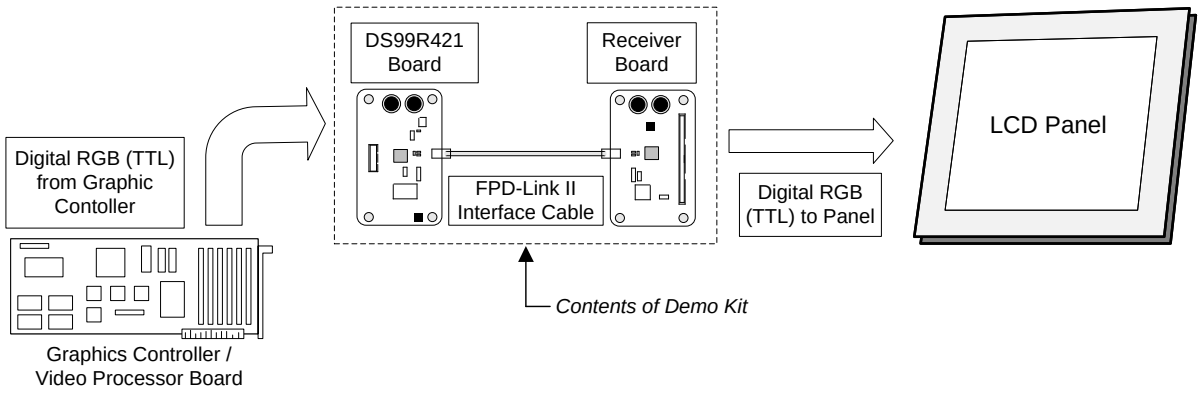


Figure 2. Typical SERDES Setup of LCD Panel Application

The picture below shows a typical test set up using a generator and scope.

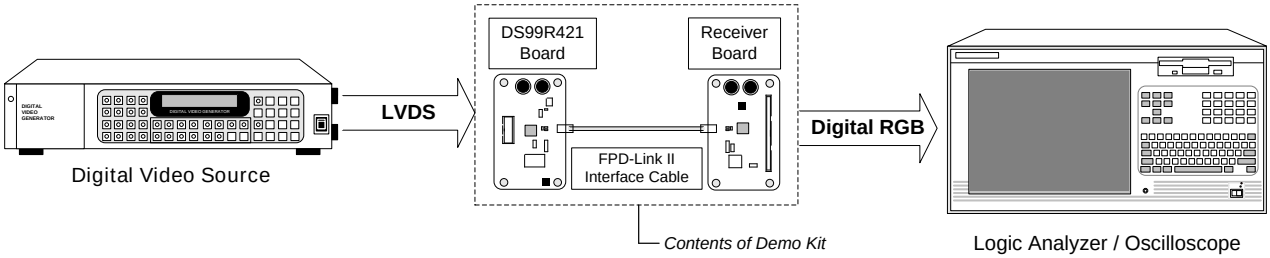
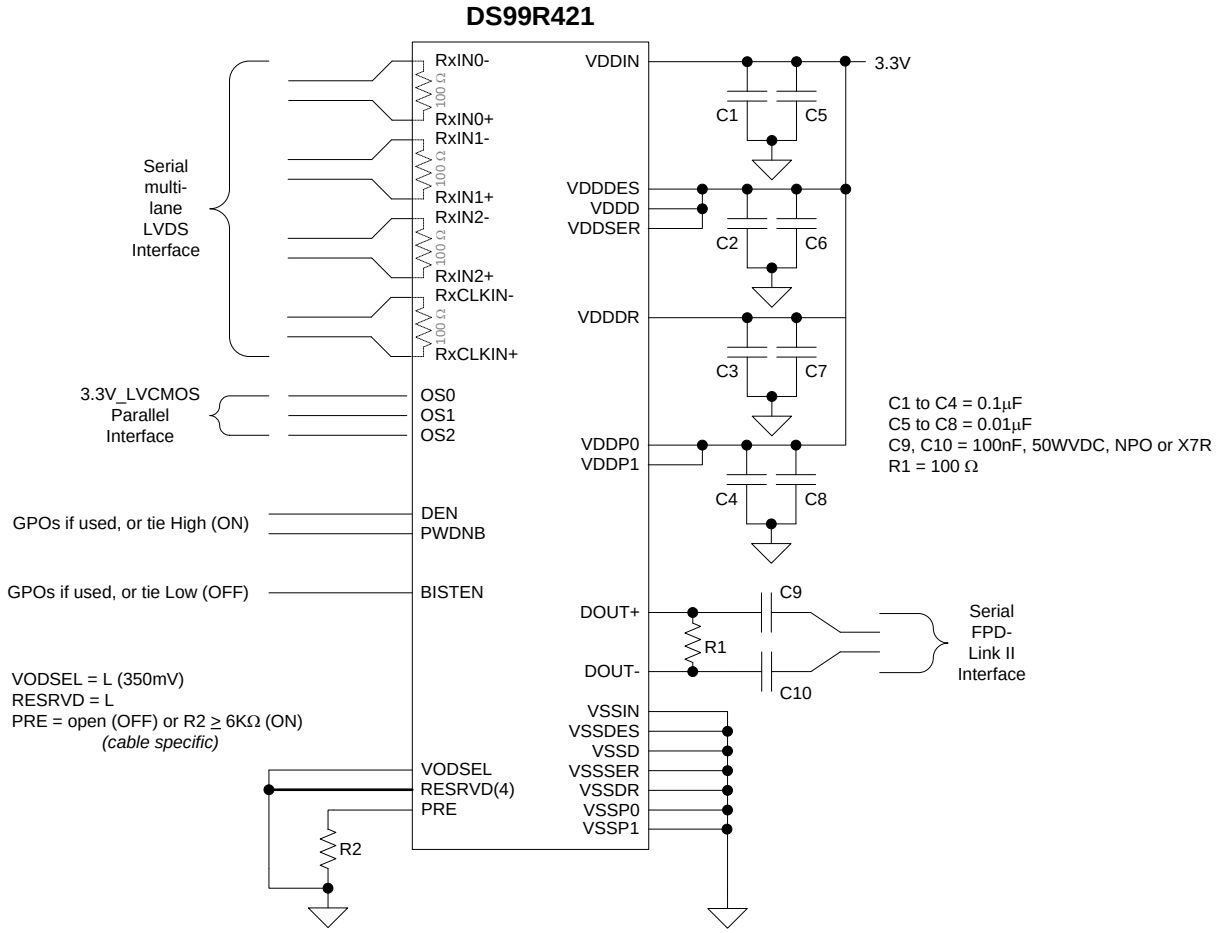


Figure 3. Typical SERDES Test Setup for Evaluation

Typical Connection Diagram DS99R421 – User Quick Reference

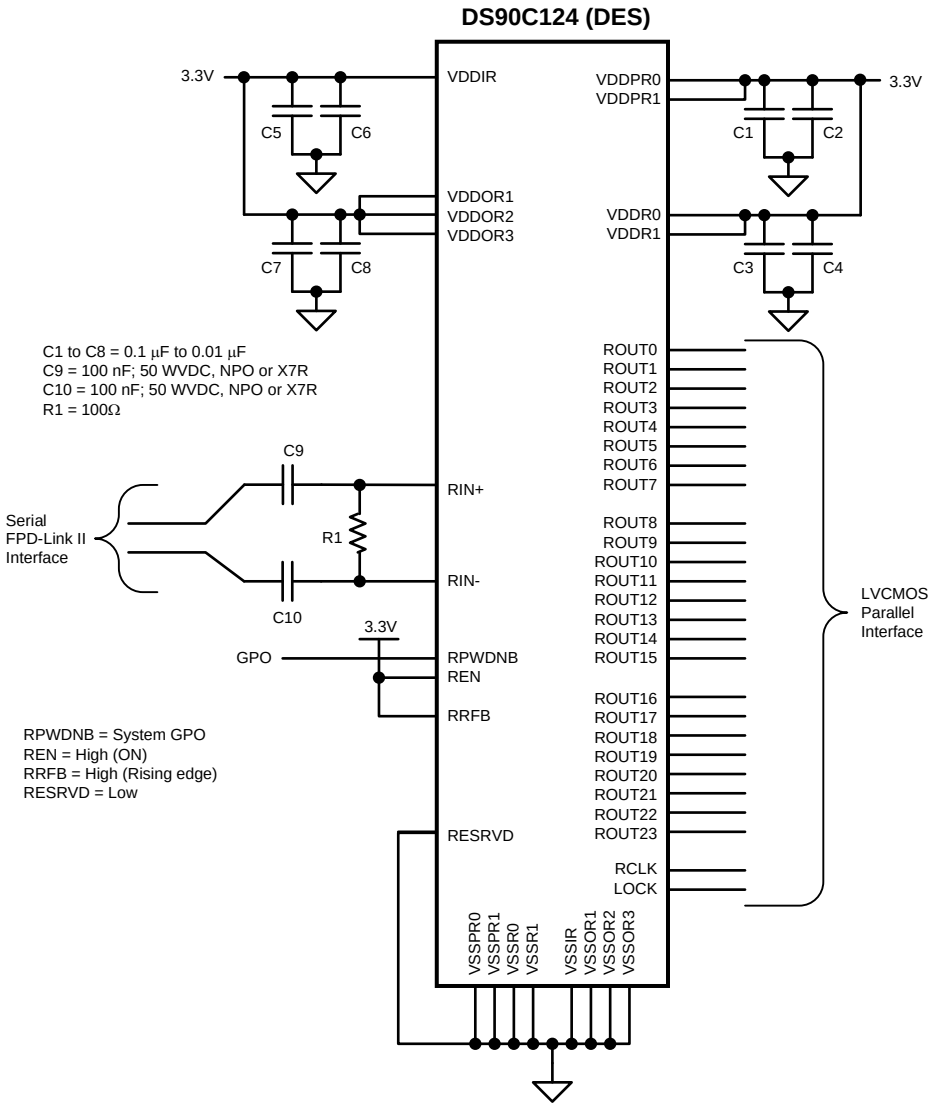


Note:
VDDs can be combined into four (4) groupings as shown (top to bottom):
1-Analog-LVDS, 2-Digital, 3-Analog-FPD-Link II, and 4-Analog-PLL/VCO for best performance.
Absolute minimum grouping should be Analog Power and Digital Power.

Decoupling specified (C1-C8) is the minimum that should be used.

Figure 6. Typical DS90C241 Tx SERDES Hookup

Typical Connection Diagram Rx – User Quick Reference



Note:
VDDs can be combined into a minimum of four (4) groupings as shown above: Analog-PLL/VCO, Digital-Logic, Analog-LVDS, Digital-LVCMOS O/P
Decoupling specified (C1-C8) is the minimum that should be used.

Figure 7. Typical DS90C124 Rx SERDES Hookup

Troubleshooting

If the demo boards are not performing properly, use the following as a guide for quick solutions to potential problems. If the problem persists, please contact the local Sales Representative for assistance.

QUICK CHECKS:

1. Check that Power and Ground are connected to both Tx AND Rx boards.
2. Check the supply voltage (typical 3.3V) and also current draw with both Tx and Rx boards. The Serializer board should draw about 55-65mA with clock and all data bits switching at 43MHz, (R_{PRE}=9KΩ). The De-serializer board should draw about 75-85mA with clock and all data bits switching at 43MHz, (minimum ROUT loading).
3. Verify input clock and input data signals meet requirements for VILmin, VILmax, VIHmin, VIHmax, tset, thold), also verify that data is strobed on the selected rising/falling (RFB pin) edge of the clock.
4. Check that the Jumpers and Switches are set correctly.
5. Check that the cable is properly connected.

TROUBLESHOOTING CHART

Problem…	**Solution…**
There is only the output clock. There is no output data.	Make sure the data is applied to the correct input pin. Make sure data is valid at the input.
No output data and clock.	Make sure Power is on. Input data and clock are active and connected correctly. Make sure that the cable is secured to both demo boards.
Power, ground, input data and input clock are connected correctly, but no outputs.	Check the Power Down pins of both Translator and De-serializer boards to make sure that the devices are enabled (/PD=Vcc) for operation. Also check DEN on the Serializer board and REN on the Deserializer board is set HIGH.
The devices are pulling more than 1A of current.	Check for shorts in the cables connecting the Translator and RX boards.
After powering up the demo boards, the power supply reads less than 3V when it is set to 3.3V.	Use a larger power supply that will provide enough current for the demo boards, a 500mA minimum power supply is recommended.

Note: Please note that the following references are supplied only as a courtesy to our valued customers. It is not intended to be an endorsement of any particular equipment or hardware supplier.

Connector References

Hirose Electric Europe B.V.
Beech Avenue 46
1119 PV Schiphol-Rijk
The Netherlands
Phone: +31 20 655 7467, Fax: +31 20 655 7469
www.HiroseEurope.com

Cable References

Nissei Electric Co., LTD
1509 Okubo-Cho, Hamamatsu-City
Shizuoka-Pref, 432-8006 Japan
Phone: +81 53 485 4114, Fax: +81 53 485 6908
www.nissei-el.co.jp

Cable Recommendations

- For optimal performance, we recommend Shielded Twisted Pair (STP) 100Ω differential impedance cable for high-speed data applications.

Equipment References

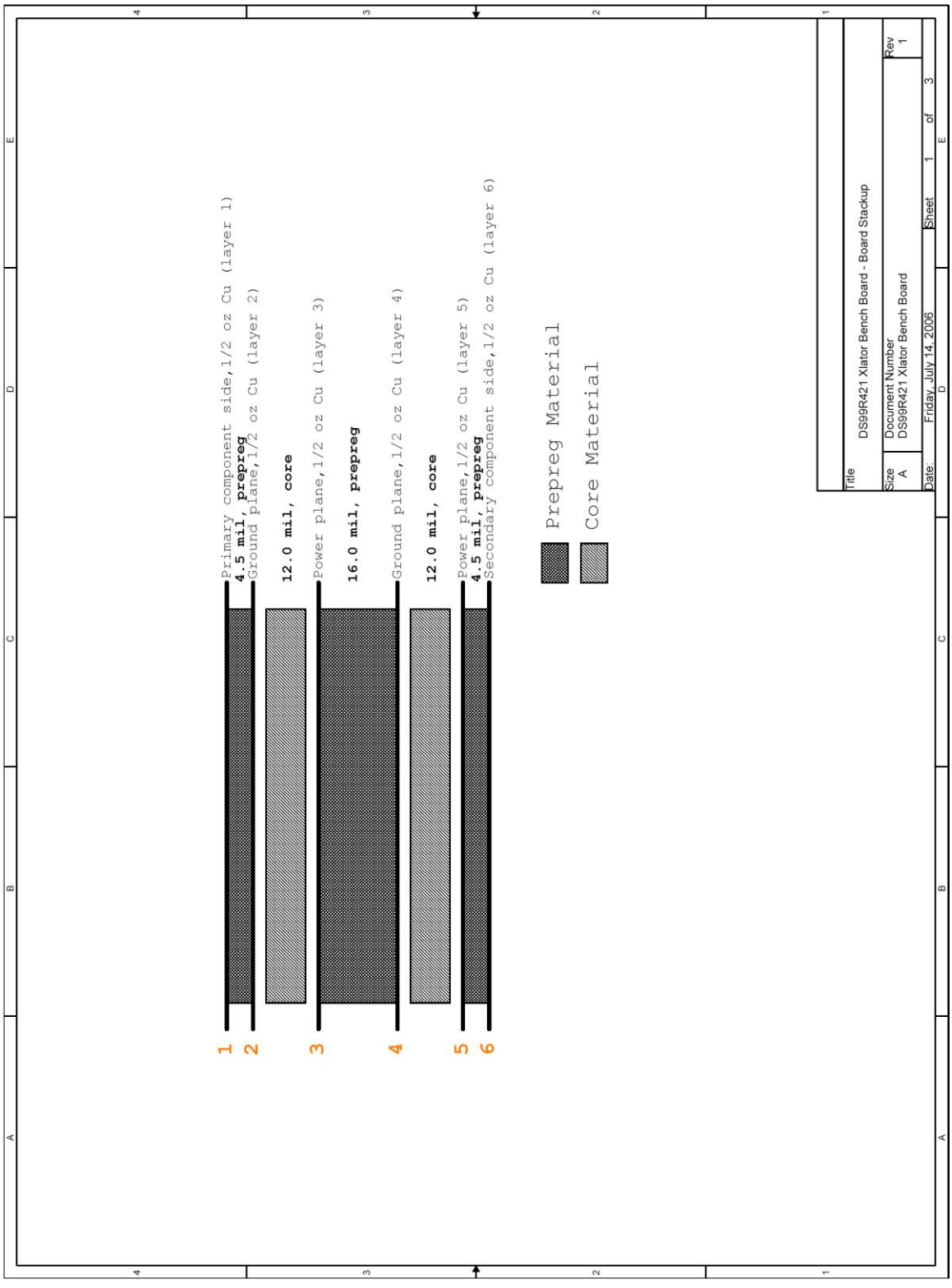
Astro Systems
425 S. Victory Blvd. Suite A
Burbank, CA 91502
Phone: (818) 848-7722 , Fax: (818) 848-7799
www.astro-systems.com
Digital Video Pattern Generator – Astro Systems VG-835 (or equivalent):

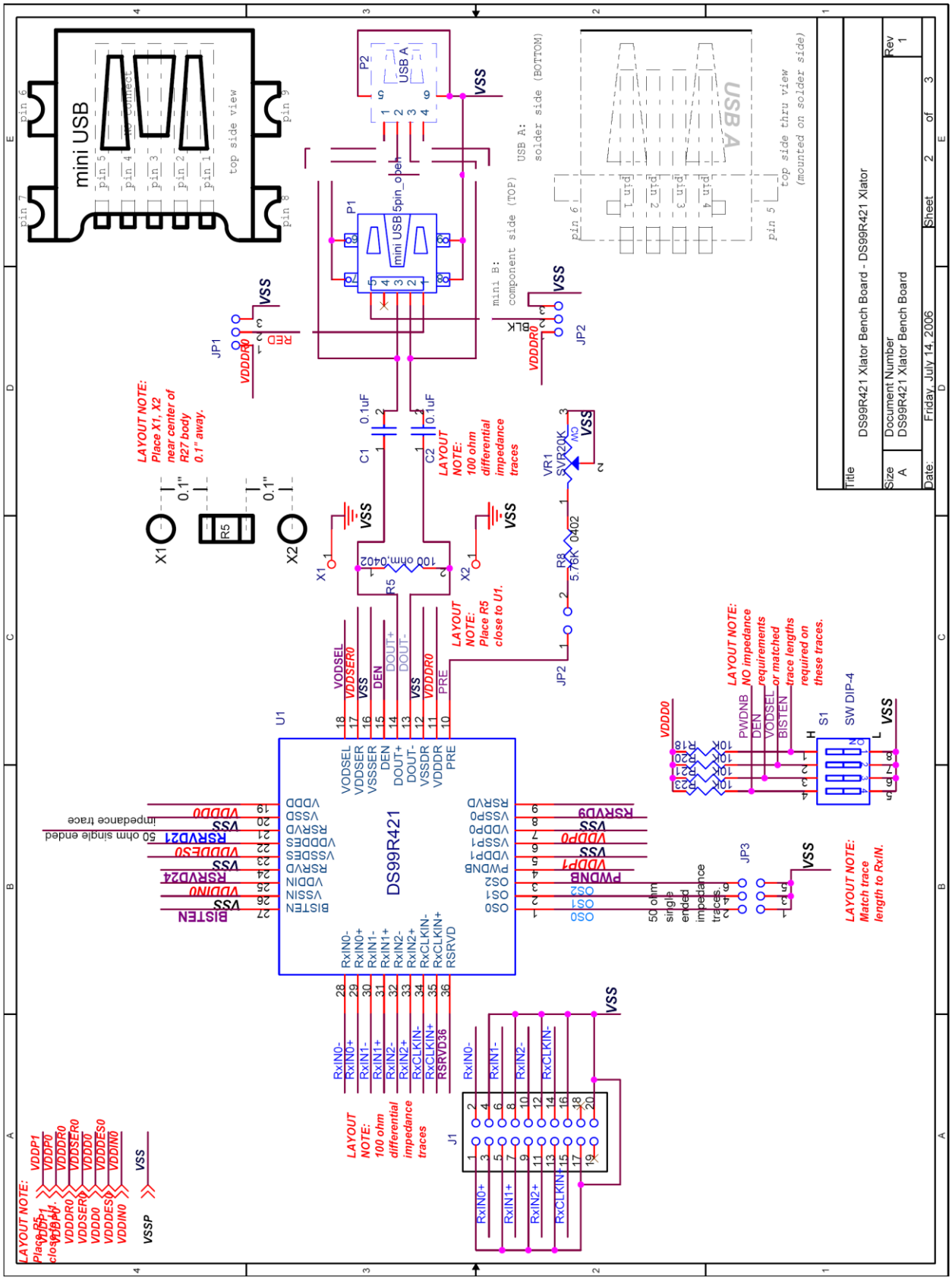
Extra Component References

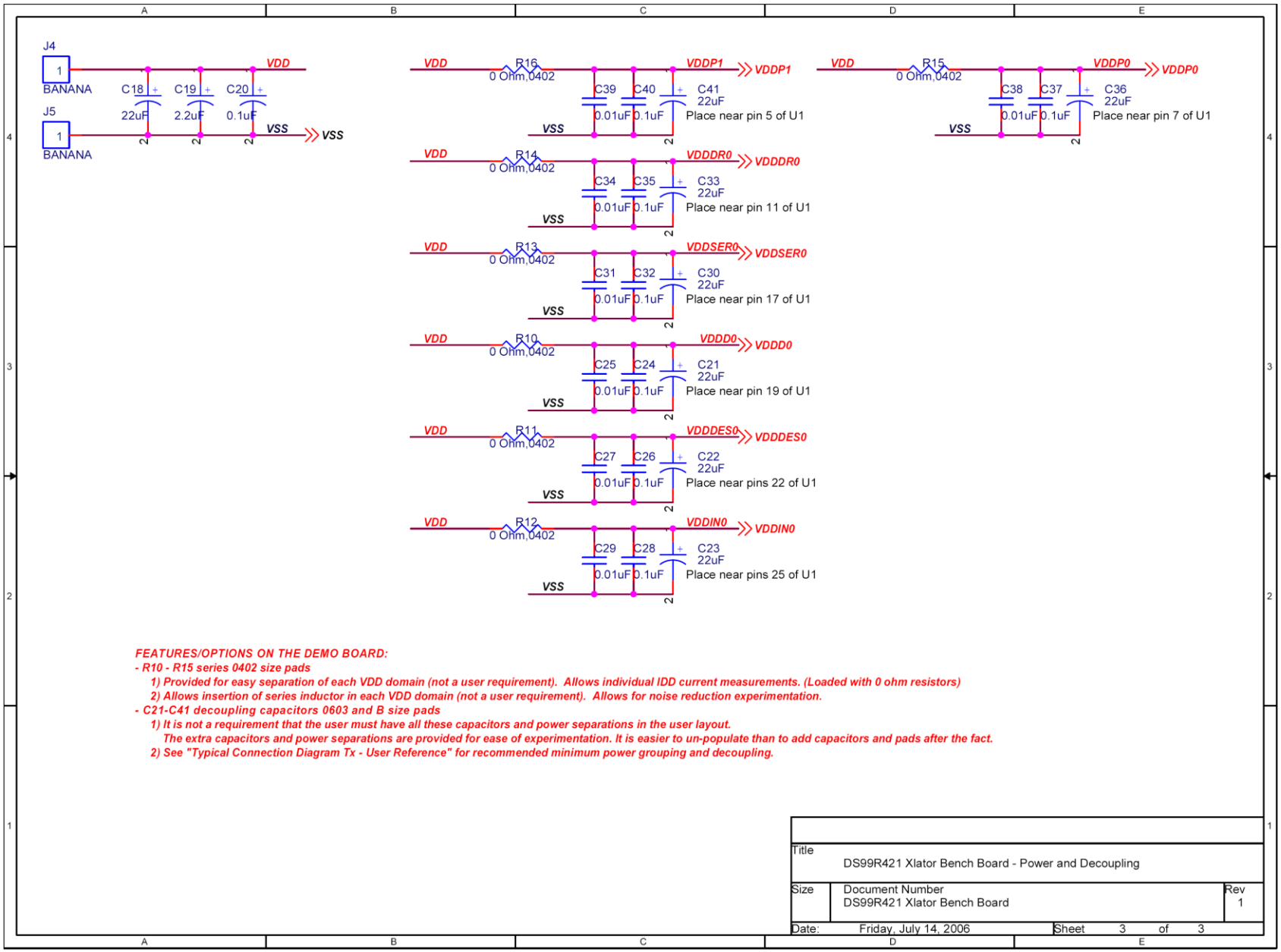
TDK Corporation of America
1740 Technology Drive, Suite 510
San Jose, CA 95110
Phone: (408) 437-9585, Fax: (408) 437-9591
www.component.tdk.com
Optional EMI Filters – TDK Chip Beads (or equivalent)

Appendix

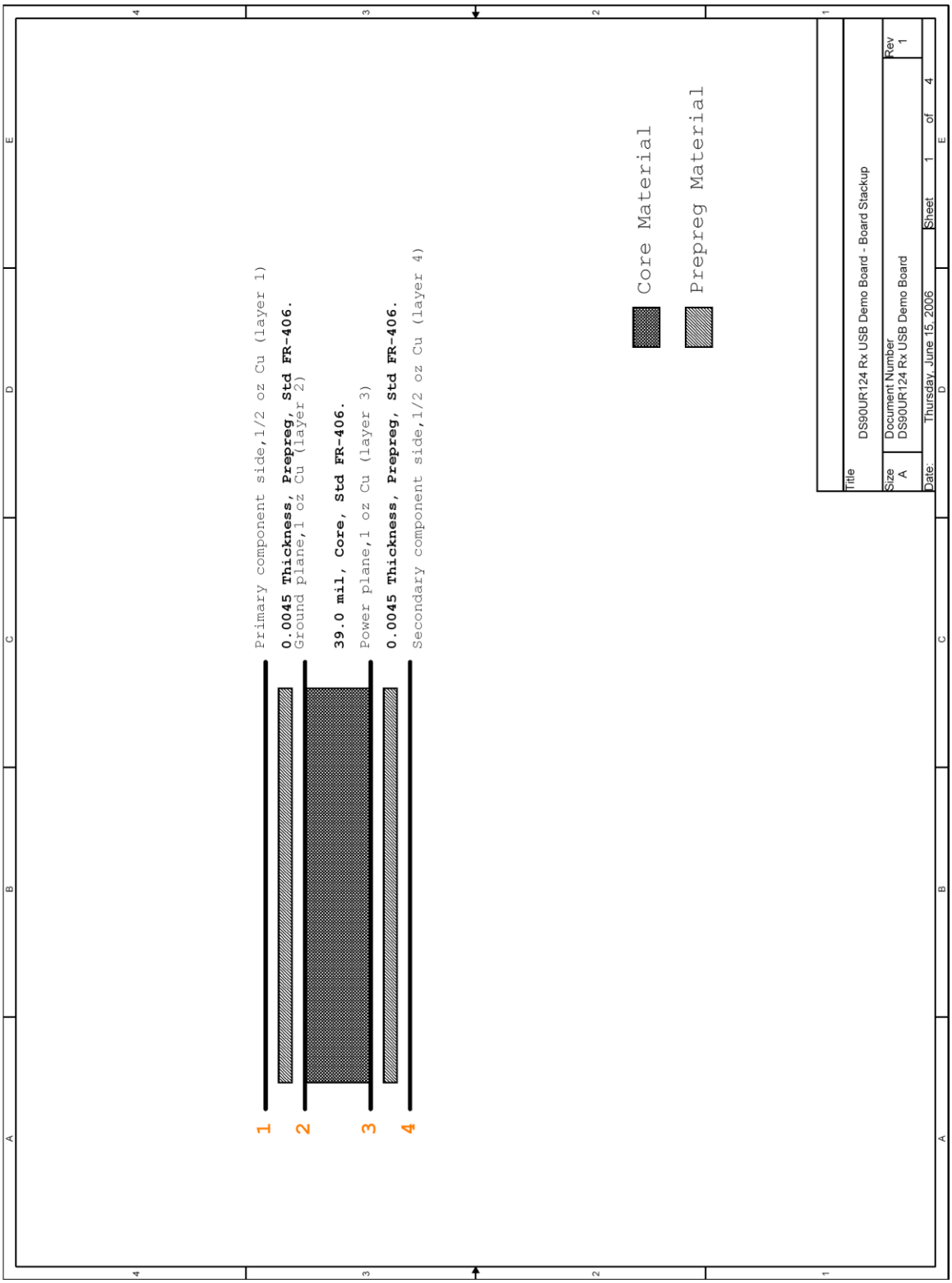
Serializer (Tx) PCB Schematic:

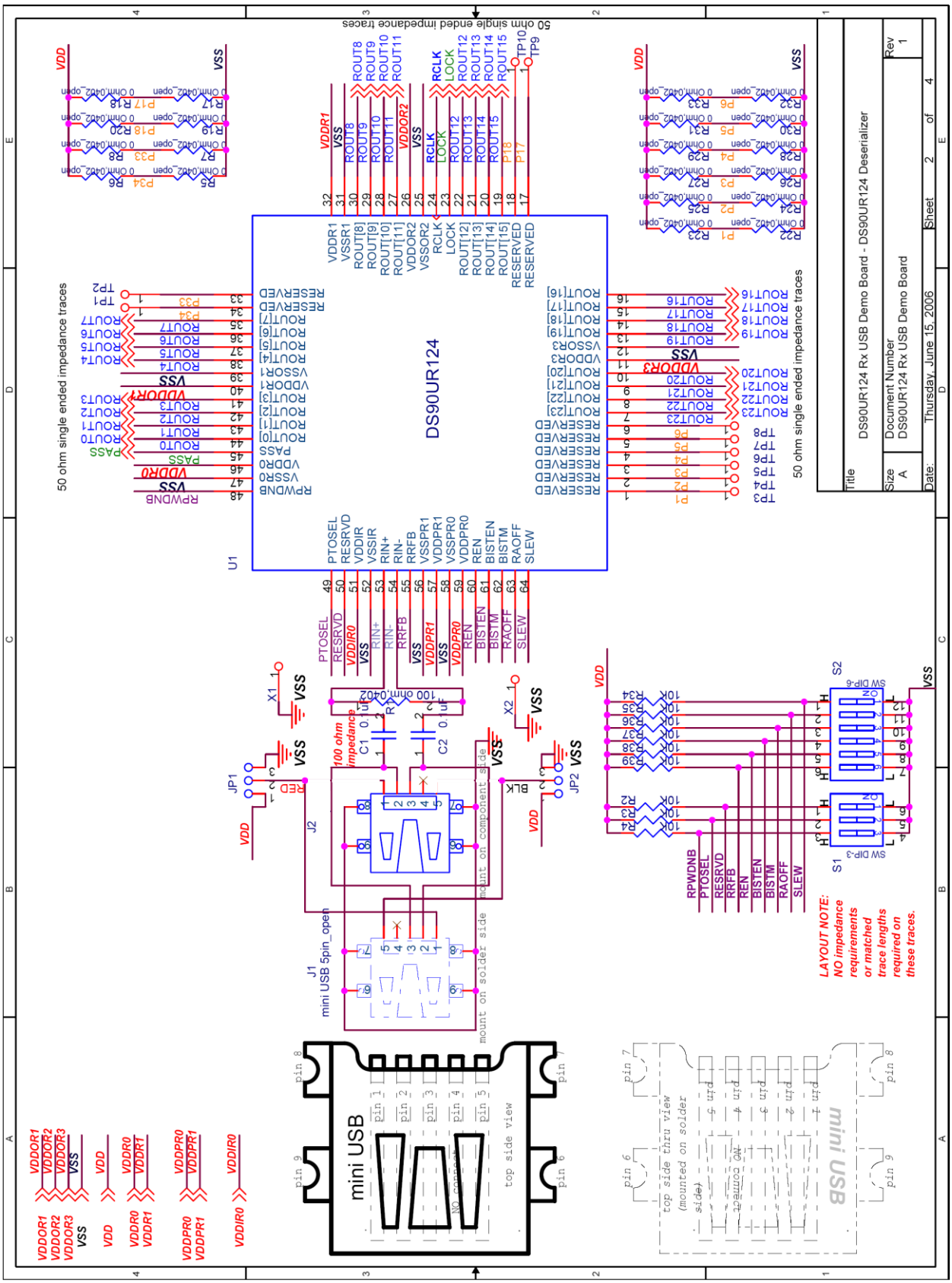


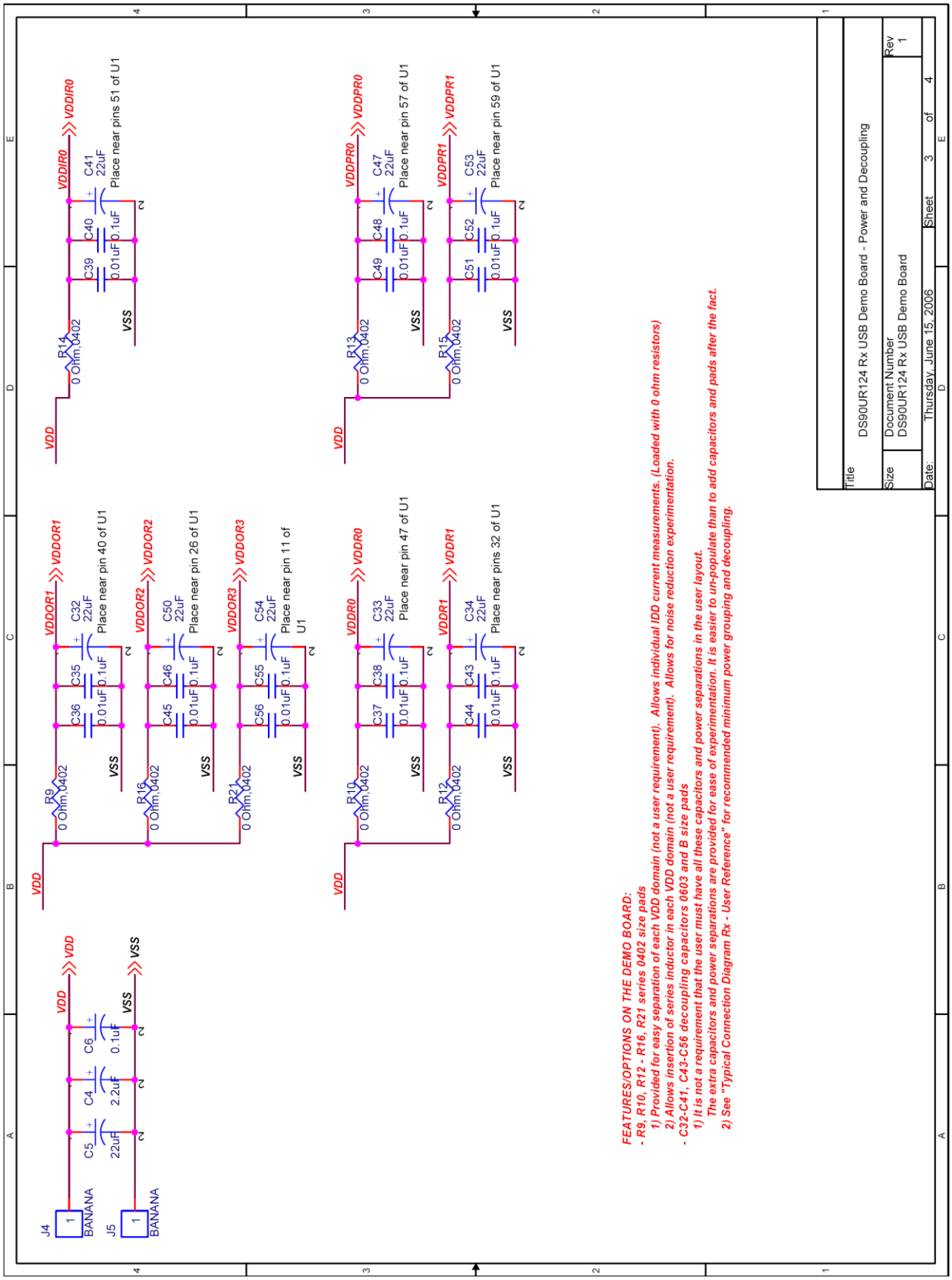

DS99R421 Xlator Bench Board - DS99R421 Xlator
Document Number
DS99R421 Xlator Bench Board
Rev 1
Friday, July 14, 2006
Sheet 2 of 3
DS99R421
U1
J1
JP1
JP2
JP3
S1
SW DIP-4
P1
P2
mini USB
USB A
LAYOUT NOTE:
Place X1, X2 near center of R27 body 0.1" away.
LAYOUT NOTE:
100 ohm differential impedance traces
LAYOUT NOTE:
Place R5 close to U1.
LAYOUT NOTE:
NO impedance requirements or matched trace lengths required on these traces.
LAYOUT NOTE:
Match trace length to RxIN.
50 ohm single ended impedance traces
50 ohm single ended impedance trace
VDDP1
VDDP0
VDDR0
VDDSER0
VDDD0
VDDDES0
VDDIN0
VSSP
VSS

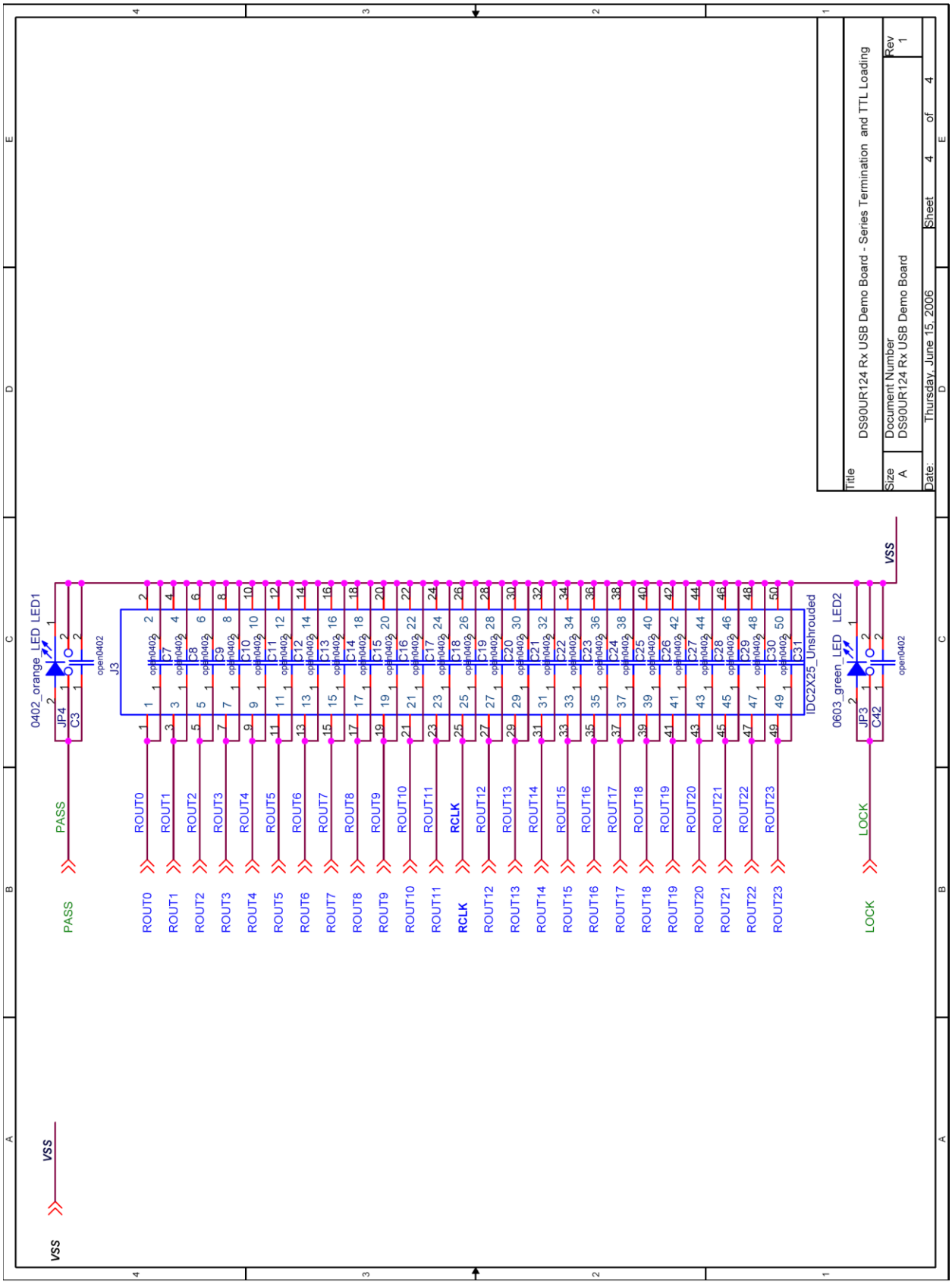

J4
1
BANANA
J5
1
BANANA
C18
22uF
C19
2.2uF
C20
0.1uF
VDD
VSS
VSS
R16
0 Ohm,0402
C39
0.01uF
C40
0.1uF
C41
22uF
VDDP1
VDDP1
Place near pin 5 of U1
R15
0 Ohm,0402
C38
0.01uF
C37
0.1uF
C36
22uF
VDDP0
VDDP0
Place near pin 7 of U1
R14
0 Ohm,0402
C34
0.01uF
C35
0.1uF
C33
22uF
VDDDR0
VDDDR0
Place near pin 11 of U1
R13
0 Ohm,0402
C31
0.01uF
C32
0.1uF
C30
22uF
VDDSER0
VDDSER0
Place near pin 17 of U1
R10
0 Ohm,0402
C25
0.01uF
C24
0.1uF
C21
22uF
VDDD0
VDDD0
Place near pin 19 of U1
R11
0 Ohm,0402
C27
0.01uF
C26
0.1uF
C22
22uF
VDDDES0
VDDDES0
Place near pins 22 of U1
R12
0 Ohm,0402
C29
0.01uF
C28
0.1uF
C23
22uF
VDDIN0
VDDIN0
Place near pins 25 of U1
FEATURES/OPTIONS ON THE DEMO BOARD:
- R10 - R15 series 0402 size pads
1) Provided for easy separation of each VDD domain (not a user requirement). Allows individual IDD current measurements. (Loaded with 0 ohm resistors)
2) Allows insertion of series inductor in each VDD domain (not a user requirement). Allows for noise reduction experimentation.
- C21-C41 decoupling capacitors 0603 and B size pads
1) It is not a requirement that the user must have all these capacitors and power separations in the user layout.
The extra capacitors and power separations are provided for ease of experimentation. It is easier to un-populate than to add capacitors and pads after the fact.
2) See "Typical Connection Diagram Tx - User Reference" for recommended minimum power grouping and decoupling.
Title
DS99R421 Xlator Bench Board - Power and Decoupling
Size
Document Number
DS99R421 Xlator Bench Board
Rev
1
Date:
Friday, July 14, 2006
Sheet
3
of
3

De-serializer (Rx) PCB Schematic:

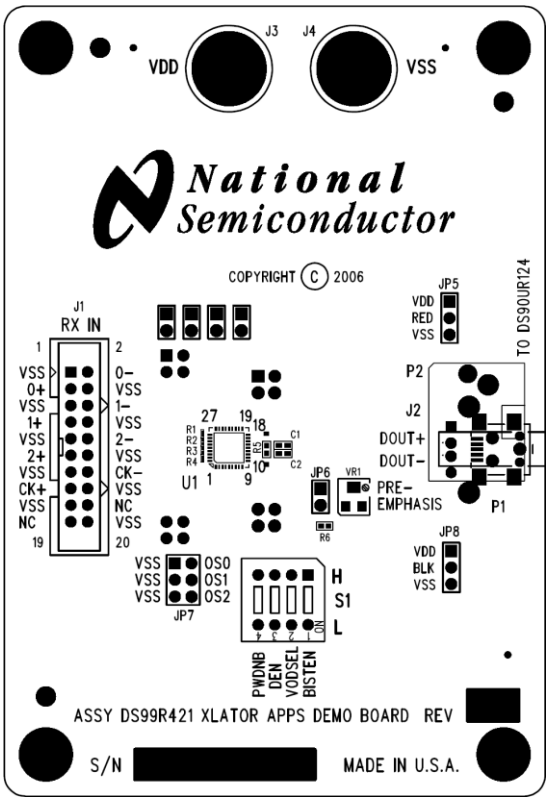



DS90UR124
50 ohm single ended impedance traces
50 ohm single ended impedance traces
50 ohm single ended impedance traces
Title
DS90UR124 Rx USB Demo Board - DS90UR124 Deserializer
Size
A
Document Number
DS90UR124 Rx USB Demo Board
Rev
1
Date:
Thursday, June 15, 2006
Sheet
2
of
4
mini USB
top side thru view
(mounted on solder side)
top side view
mini USB
mount on component side
mount on solder side
mini USB 5pin_open
LAYOUT NOTE:
NO impedance requirements or matched trace lengths required on these traces.

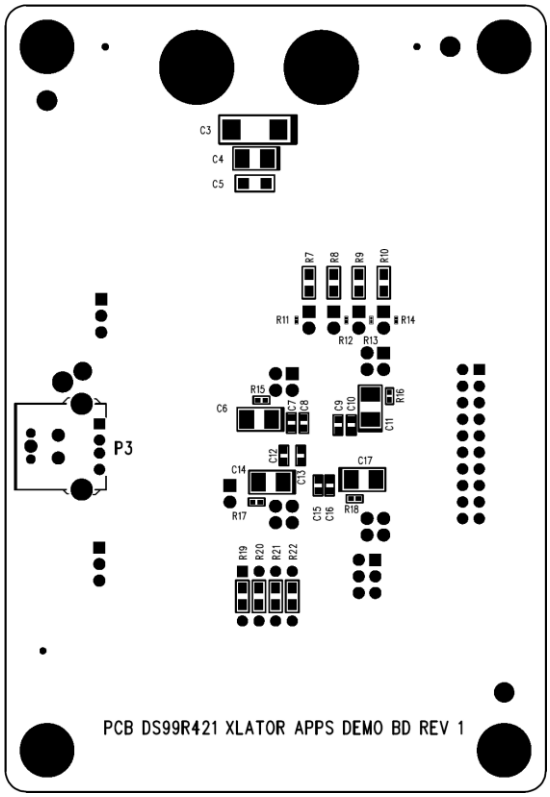

J4
BANANA
J5
BANANA
C5 22uF
C4 2.2uF
C6 0.1uF
VDD
VSS
VDDOR1
VDDOR2
VDDOR3
VDDR0
VDDR1
VDDIR0
VDDPR0
VDDPR1
R9 0 Ohm,0402
R16 0 Ohm,0402
R21 0 Ohm,0402
R10 0 Ohm,0402
R12 0 Ohm,0402
R14 0 Ohm,0402
R13 0 Ohm,0402
R15 0 Ohm,0402
C32 22uF
C35 0.01uF
C36 0.1uF
Place near pin 40 of U1
C50 22uF
C46 0.01uF
C45 0.1uF
Place near pin 26 of U1
C54 22uF
C55 0.01uF
C56 0.1uF
Place near pin 11 of U1
C33 22uF
C38 0.01uF
C37 0.1uF
Place near pin 47 of U1
C34 22uF
C43 0.01uF
C44 0.1uF
Place near pins 32 of U1
C41 22uF
C40 0.01uF
C39 0.1uF
Place near pins 51 of U1
C47 22uF
C48 0.01uF
C49 0.1uF
Place near pin 57 of U1
C53 22uF
C52 0.01uF
C51 0.1uF
Place near pin 59 of U1
FEATURES/OPTIONS ON THE DEMO BOARD:
- R9, R10, R12 - R16, R21 series 0402 size pads
1) Provided for easy separation of each VDD domain (not a user requirement). Allows individual IDD current measurements. (Loaded with 0 ohm resistors)
2) Allows insertion of series inductor in each VDD domain (not a user requirement). Allows for noise reduction experimentation.
- C32-C41, C43-C56 decoupling capacitors 0603 and B size pads
1) It is not a requirement that the user must have all these capacitors and power separations in the user layout.
The extra capacitors and power separations are provided for ease of experimentation. It is easier to un-populate than to add capacitors and pads after the fact.
2) See "Typical Connection Diagram Rx - User Reference" for recommended minimum power grouping and decoupling.
Title
DS90UR124 Rx USB Demo Board - Power and Decoupling
Size
Document Number
DS90UR124 Rx USB Demo Board
Rev
1
Date: Thursday, June 15, 2006
Sheet 3 of 4


Title
DS90UR124 Rx USB Demo Board - Series Termination and TTL Loading
Size
A
Document Number
DS90UR124 Rx USB Demo Board
Rev
1
Date:
Thursday, June 15, 2006
Sheet
4
of
4
0402_orange_LED LED1
0603_green_LED LED2
IDC2X25_Unshrouded
PASS
LOCK
VSS
ROUT0
ROUT1
ROUT2
ROUT3
ROUT4
ROUT5
ROUT6
ROUT7
ROUT8
ROUT9
ROUT10
ROUT11
RCLK
ROUT12
ROUT13
ROUT14
ROUT15
ROUT16
ROUT17
ROUT18
ROUT19
ROUT20
ROUT21
ROUT22
ROUT23

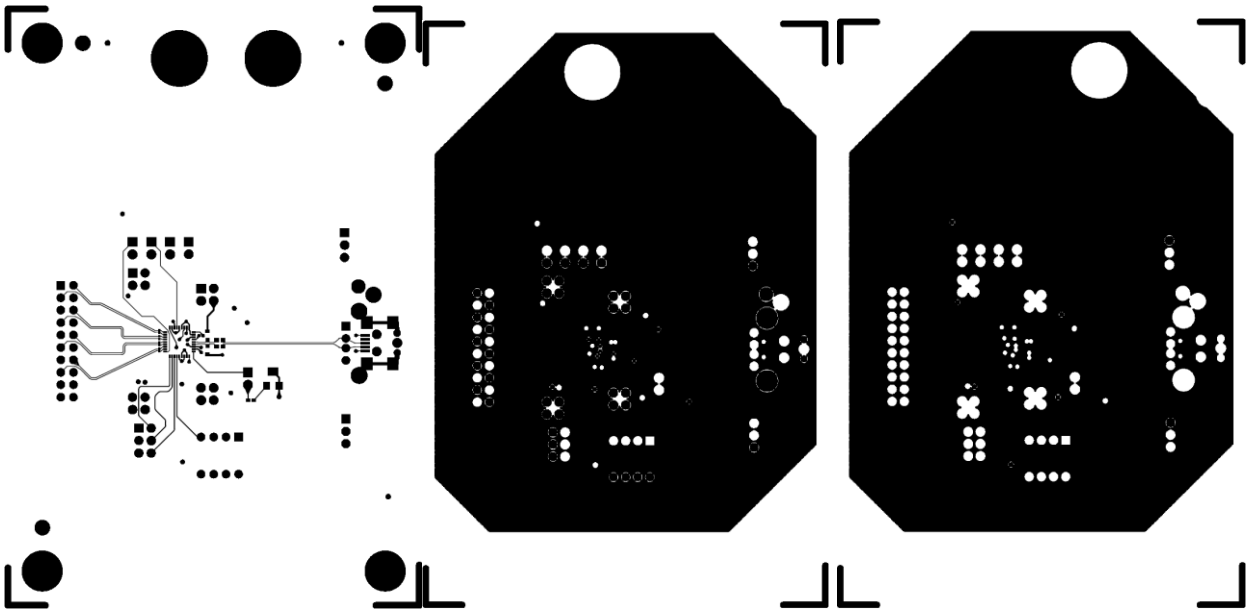
Serializer (Tx) PCB Layout:



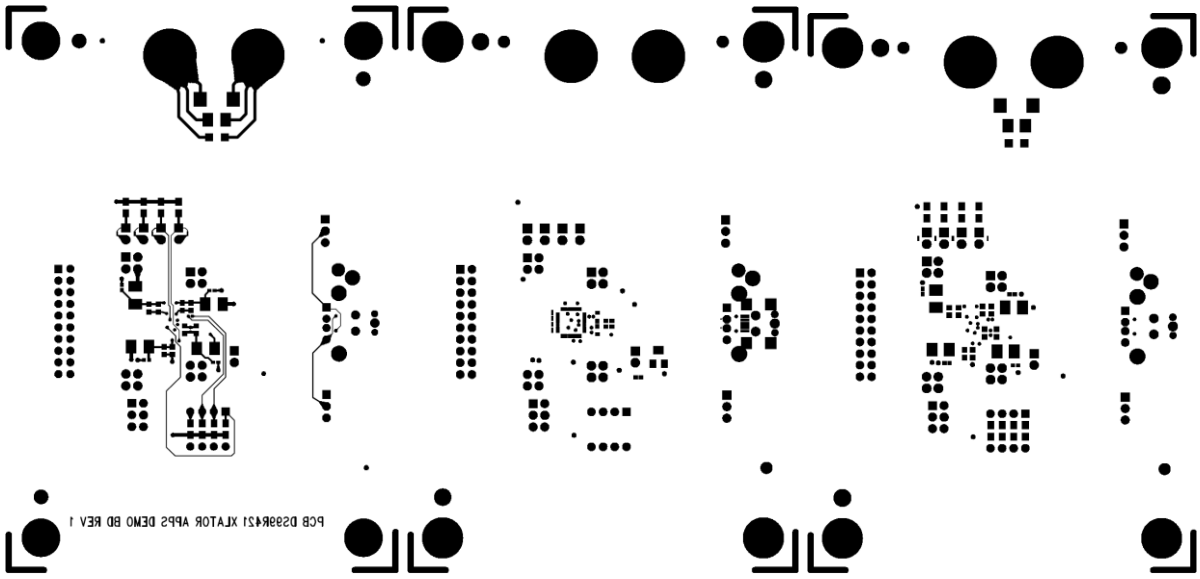
TOP VIEW



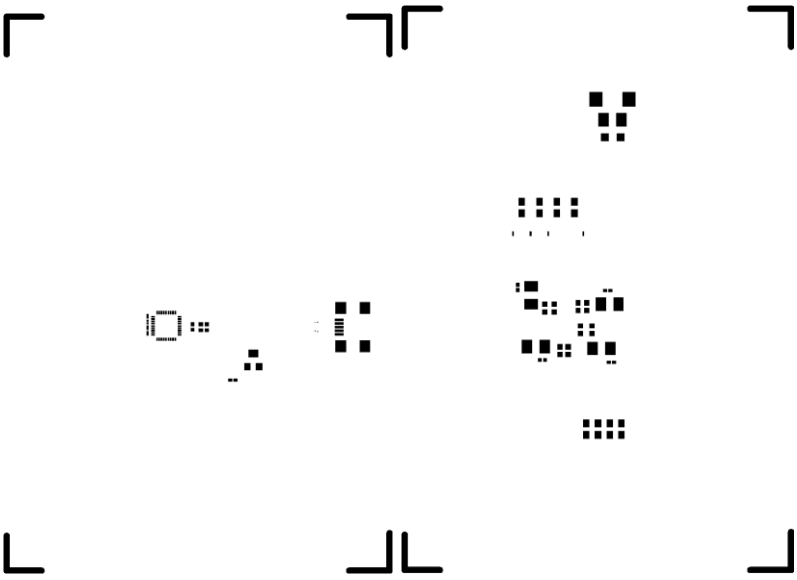
BOTTOMSIDE VIEW



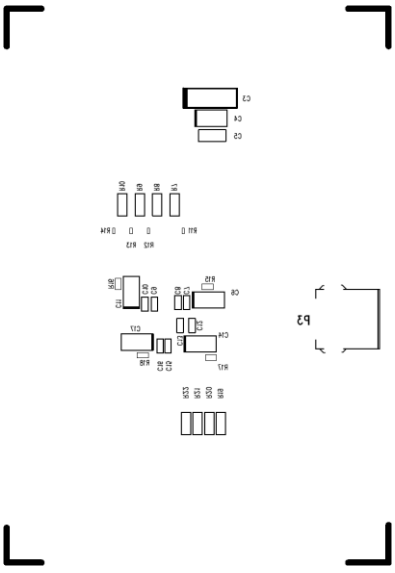
PRIMARY COMPONENT SIDE – LAYER 1 GROUND PLANE (VSS) – LAYER 2 POWER PLANE (VDD) – LAYER 3



SECONDARY COMP SIDE – LAYER 4 PRIMARY COMP SIDE – SOLDER MASK (LAYER 1) SECONDARY COMP SIDE – SOLDER MASK (LAYER 4)

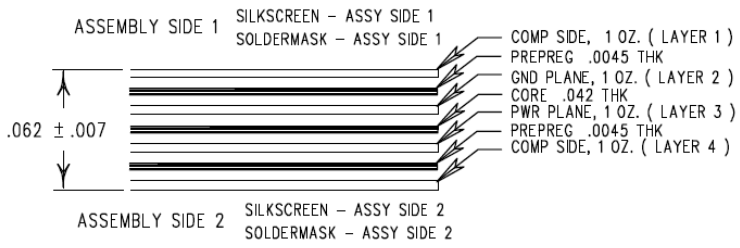


PRIMARY COMP SIDE – SOLDER PASTE (LAYER 1) SECONDARY COMP SIDE – SOLDER PASTE (LAYER 4)

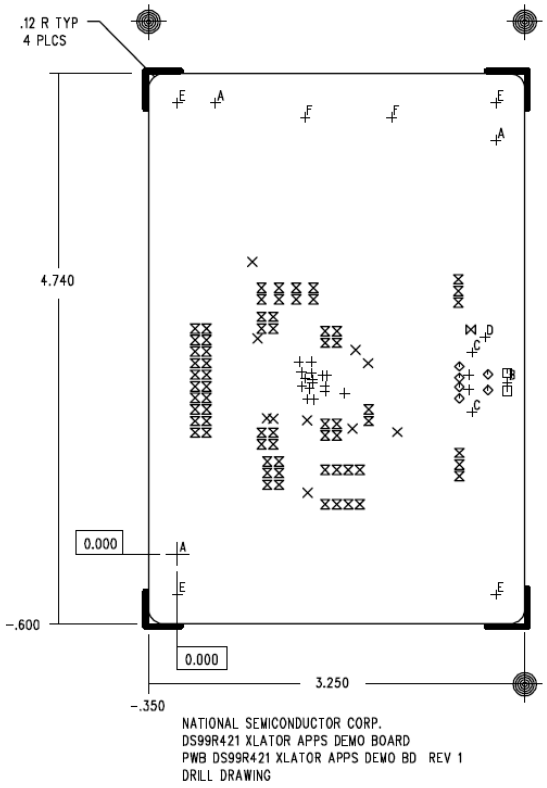


SILKSCREEN COMP SIDE – SILKSCREEN (LAYER 4)

Serializer (Tx) PCB Stackup:



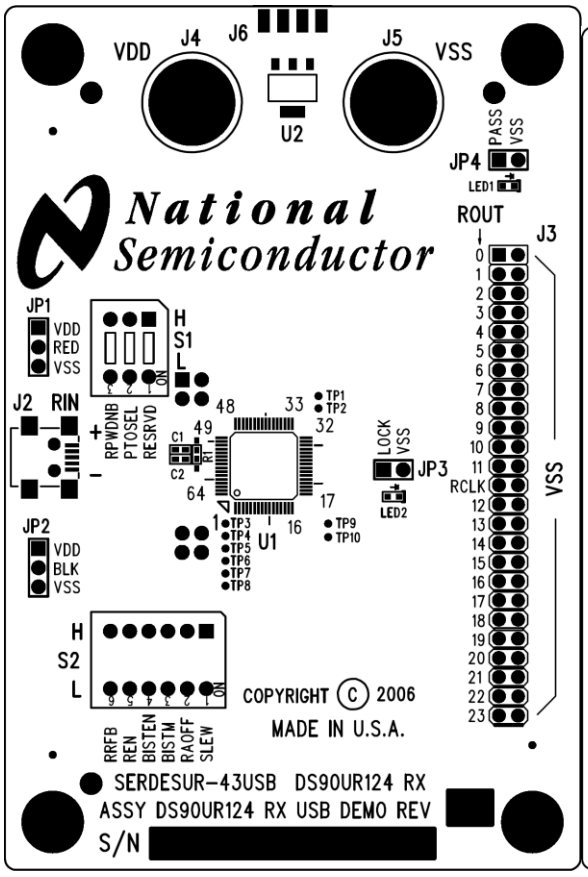
HOLE CHART				
CODE	SIZE	QTY	PLATED	TOL
+	0.011	18	YES	± .003
×	0.014	9	YES	± .003
□	0.024	2	YES	± .003
◇	0.036	6	YES	± .003
⧖	0.040	66	YES	± .003
⋈	0.063	1	YES	± .002
A	0.125	3	NO	+.003 –.000
B	0.078	1	NO	± .003
C	0.091	2	YES	± .003
D	0.094	1	NO	± .003
E	0.156	4	YES	± .004
F	0.265	2	YES	± .005



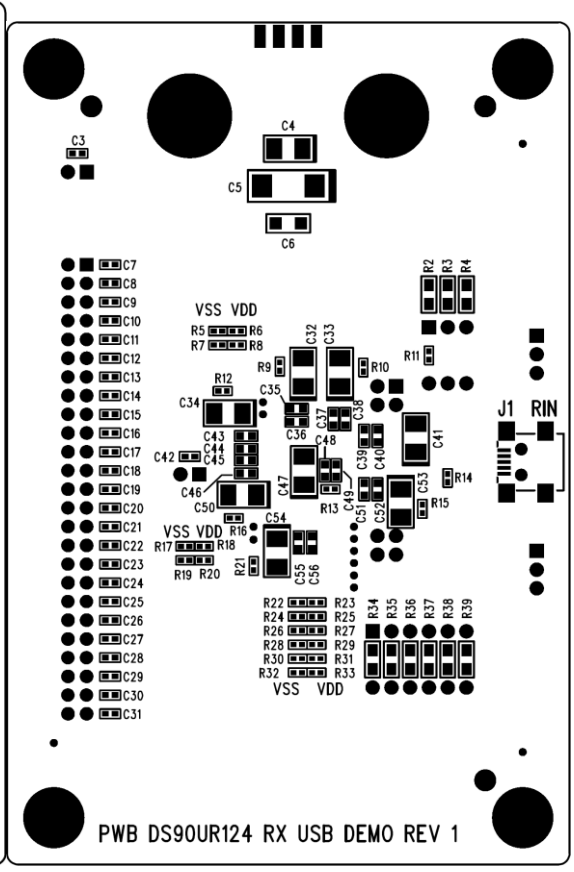
NOTES: UNLESS OTHERWISE SPECIFIED

1. PRIMARY COMPONENT SIDE IS SHOWN.
2. HOLES MARKED " A " ARE TOOLING HOLES, UNPLATED, AND SHALL BE "ONCE" DRILLED.
3. FABRICATE USING MASTER FILM DS99R421 XLATOR APPS DEMO BD REV 1. USE GERBER FILE A517B0A.PHO FOR BOARD ROUTE.
4. ACCEPTABILITY SHALL BE BASED ON IPC–A–600, CLASS 2
5. MATERIAL: BASE MATERIAL IS POLYCLAD FR–370HR OR EQUIV (Tg >=170 DEG C) (Td >=350 DEG C), COLOR GREEN, 0.062 +/–.006 INCH NOM. THICKNESS COPPER CLADDING SHALL BE 1 OZ.
6. PLATING: ALL HOLES AND CONDUCTIVE SURFACES SHALL BE PLATED WITH A MIN. OF .001 INCH COPPER. SURFACE PLATING TO BE ELECTROLESS NICKEL / IMMERSION GOLD (ENIG).
7. FABRICATION TOLERANCES:
   END PRODUCT CONDUCTOR WIDTHS AND LAND DIAMETERS SHALL NOT VARY MORE THAN .002 INCH FROM THE 1:1 DIMENSIONS OF THE MASTER PATTERN. THE CONDUCTIVE PATTERN SHALL BE POSITIONED SO THAT THE LOCATION OF ANY LAND SHALL BE WITHIN .002 INCH DIAMETER TO THE TRUE POSITION OF THE HOLE IT CIRCUMSCRIBES THE MINIMUM ANNULAR RING SHALL BE .002 INCH. BOW AND TWIST SHALL NOT EXCEED .07 INCH PER INCH.
8. SOLDERMASK BOTH SIDES PER IPC–SM–840, TYPE A, CLASS B. COLOR–GREEN. THERE SHALL BE NO SOLDERMASK ON ANY LAND.
9. SILKSCREEN THE LEGEND ON BOTH SIDES USING NON CONDUCTIVE EPOXY INK, COLOR–WHITE. THERE SHALL BE NO INK ON ANY LAND.
10. THE .008 TRACES (LAYER 1) TO BE 50 OHM SINGLE ENDED IMPEDANCE THE .007 TRACES (LAYER 1) TO BE 100 OHM DIFFERENTIAL IMPEDANCE, AND THE DIELECTRIC REFERENCED IN BOARD STACK DETAIL IS SUGESTED. HOWEVER, TRACE WIDTHS AND OR DIELECTRIC THICKNESS MAY BE MICRO–MODIFIED IN ORDER TO FABRICATE BOARDS TO THE REQUIRED IMPEDANCE NOMINALS TO A TOLERANCE OF +/– 5%.
11. THE PCB SHALL BE E.U. ROHS COMPLIANT.

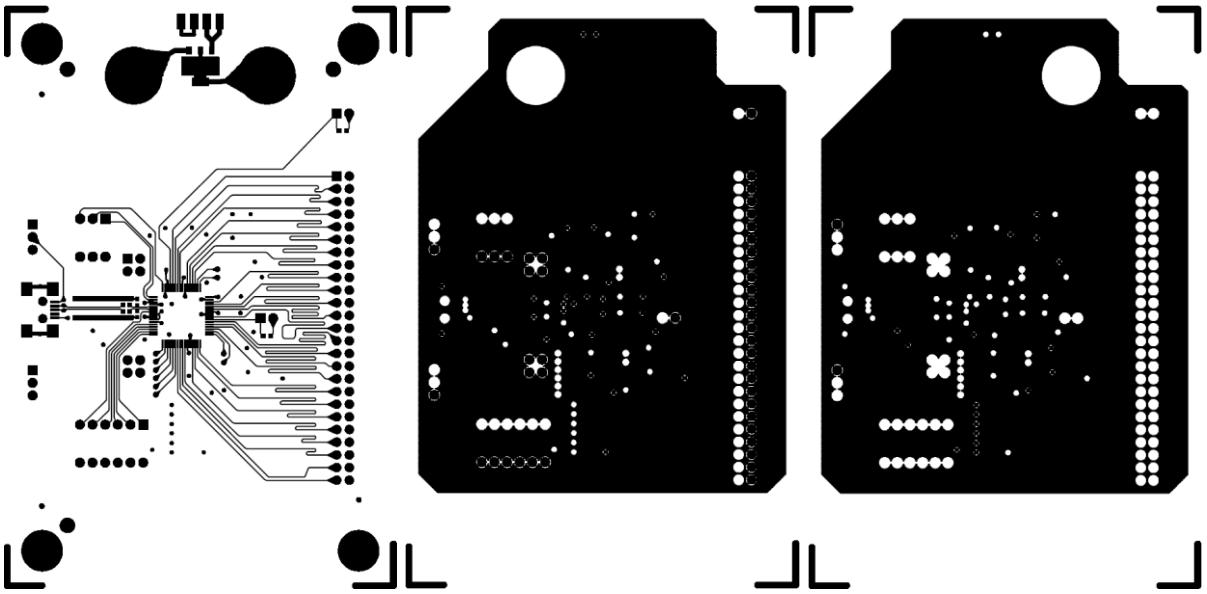
Deserializer (Rx) PCB Layout:



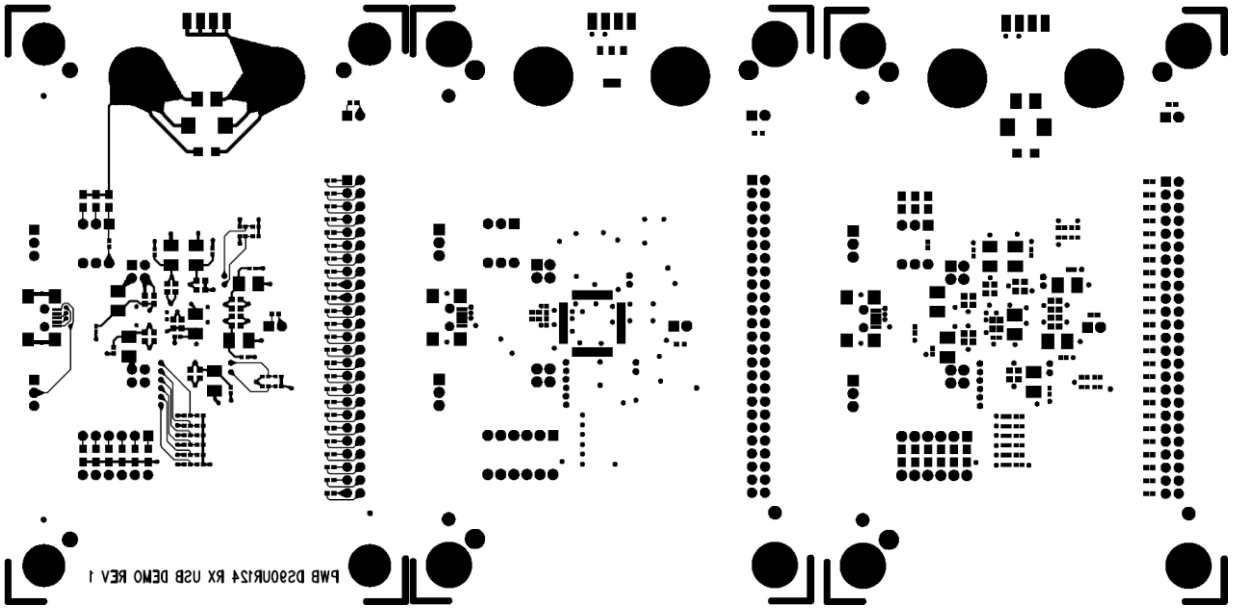
TOP VIEW



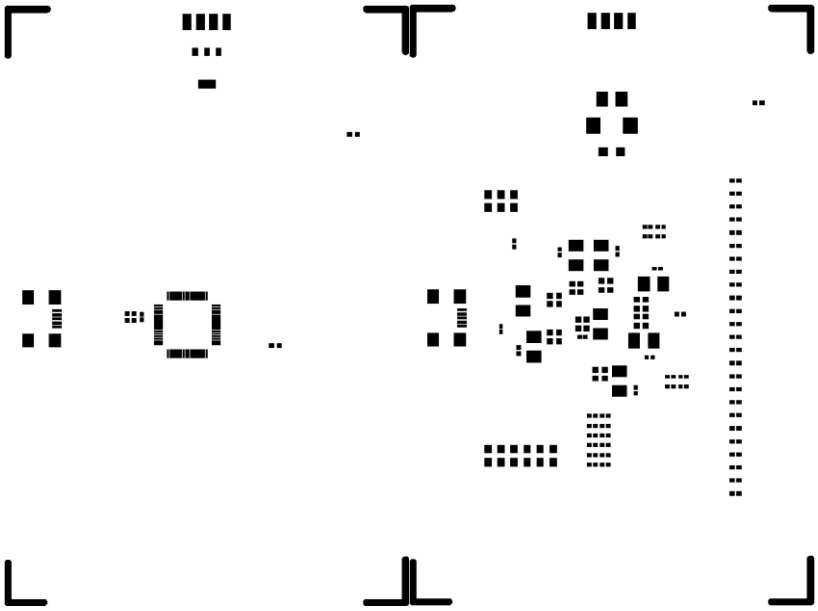
BOTTOMSIDE VIEW



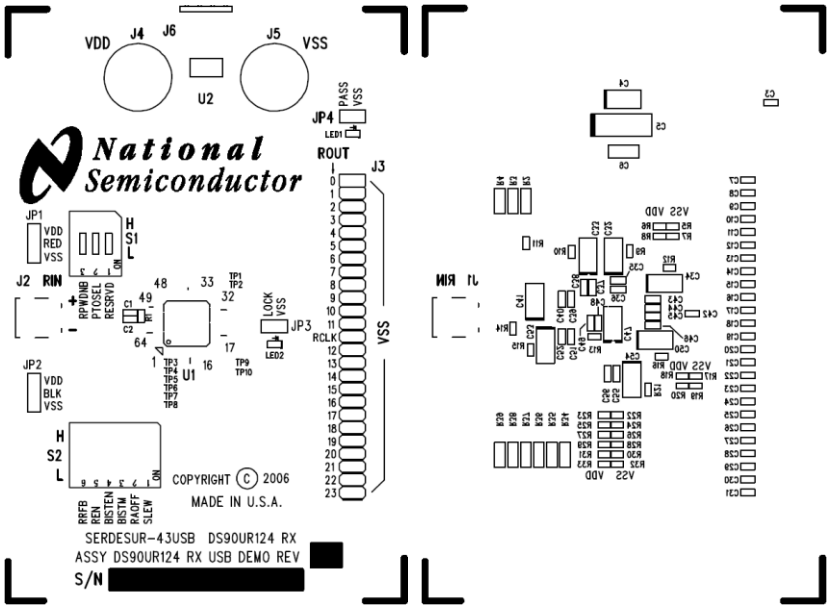
PRIMARY COMPONENT SIDE – LAYER 1 GROUND PLANE (VSS) – LAYER 2 POWER PLANE (VDD) – LAYER 3



SECONDARY COMP SIDE – LAYER 4 PRIMARY COMP SIDE – SOLDER MASK (LAYER 1) SECONDARY COMP SIDE – SOLDER MASK (LAYER 4)

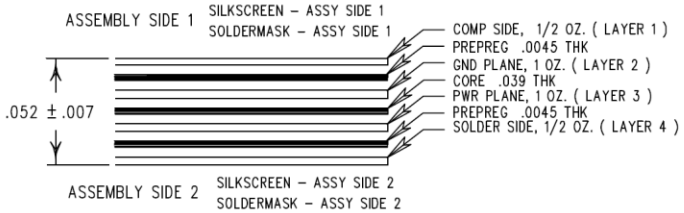


PRIMARY COMP SIDE – SOLDER PASTE (LAYER 1) SECONDARY COMP SIDE – SOLDER PASTE (LAYER 4)

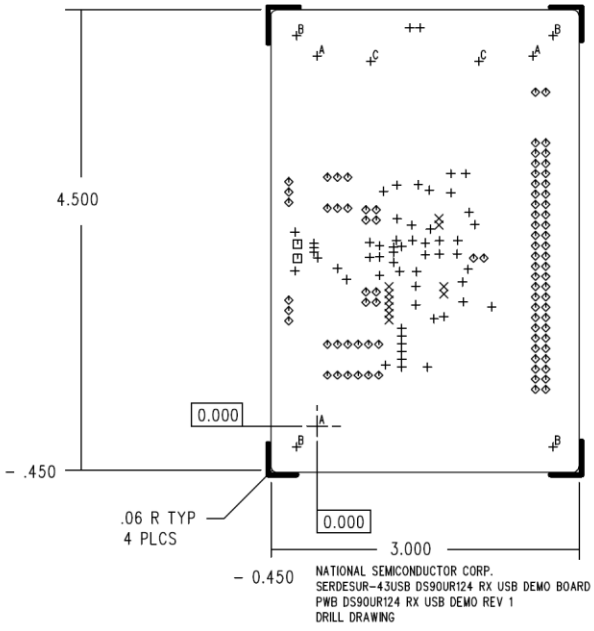


PRIMARY COMP SIDE – SILKSCREEN (LAYER 1) SILKSCREEN COMP SIDE – SILKSCREEN (LAYER 4)

Deserializer (Rx) PCB Stackup:



HOLE CHART				
CODE	SIZE	QTY	PLATED	TOL
+	0.011	57	YES	± .003
×	0.016	10	YES	± .003
□	0.035	2	YES	± .003
◇	0.043	86	YES	± .003
A	0.125	3	NO	+.003 –.000
B	0.156	4	YES	± .005
C	0.265	2	YES	± .005



NOTES: UNLESS OTHERWISE SPECIFIED

1. PRIMARY COMPONENT SIDE IS SHOWN.
2. HOLES MARKED " A " ARE TOOLING HOLES, UNPLATED, AND SHALL BE "ONCE" DRILLED.
3. FABRICATE USING MASTER FILM DS90UR124 RX USB DEMO REV 1. USE BOARD OUTLINE FILE A472B0A.PHO FOR BOARD ROUTE.
4. ACCEPTABILITY SHALL BE BASED ON IPC-A-600, CLASS 2
5. MATERIAL: BASE MATERIAL IS NEMAL-1 GRADE FR-406, COLOR GREEN, 0.052 INCH NOM. THICKNESS. COPPER CLADDING SHALL BE 1/2 OZ. OUTSIDE LAYERS AND 1 OZ INSIDE LAYERS.
6. PLATING: ALL HOLES AND CONDUCTIVE SURFACES SHALL BE PLATED WITH A MIN OF .001 INCH CU. SURFACE FINISH: GOLD FLASH, .000005 MIN.
7. FABRICATION TOLERANCES:
   END PRODUCT CONDUCTOR WIDTHS AND LAND DIAMETERS SHALL NOT VARY MORE THAN .003 INCH FROM THE 1:1 DIMENSIONS OF THE MASTER PATTERN. THE CONDUCTIVE PATTERN SHALL BE POSITIONED SO THAT THE LOCATION OF ANY LAND SHALL BE WITHIN .010 INCH DIAMETER TO THE TRUE POSITION OF THE HOLE IT CIRCUMSCRIBES THE MINIMUM ANNULAR RING SHALL BE .002 INCH. BOW AND TWIST SHALL NOT EXCEED .010 INCH PER INCH.
8. SOLDERMASK BOTH SIDES PER IPC-SM-840, TYPE A, CLASS B. COLOR-GREEN. THERE SHALL BE NO SOLDERMASK ON ANY LAND.
9. SILKSCREEN THE LEGEND ON BOTH SIDES USING NON CONDUCTIVE EPOXY INK, COLOR-WHITE. THERE SHALL BE NO INK ON ANY LAND.
10. THE .008 (LAYER 1) TRACES TO BE 50 OHM SINGLE ENDED IMPEDANCE AND THE .007 TRACES (LAYER 1) TO BE 100 OHM DIFFERENTIAL IMPEDANCE AND THE DIELECTRIC REFERENCED IN BOARD STACK DETAIL IS SUGGESTED. HOWEVER, TRACE WIDTHS AND OR DIELECTRIC THICKNESS MAY BE MICRO-MODIFIED IN ORDER TO FABRICATE BOARDS TO THE REQUIRED IMPEDANCE NOMINALS TO A TOLERANCE OF +/– 5%.
11. BOARD TO BE FABRICATED IN COMPLIANCY TO ROHS REQUIREMENTS.

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