

Schematic Checklist for HD3SS3212 and HD3SS3220

ABSTRACT

This schematic checklist provides a brief explanation of the HD3SS3212 and HD3SS3220 device pin and the recommended configuration of the device pins for default operation. The HD3SS3212 is a generic SuperSpeed differential passive 2:1 MUX that can work for any SuperSpeed interface applications (USB3, PCIe, SATA). The HD3SS3220 is not only a SuperSpeed 2:1 MUX, but also the USB Type-C™ DRP port controller. The device provides Channel Configuration(CC) logic and 5-V VCONN sourcing for ecosystems implementing USB Type-C. The HD3SS3212 and HD3SS3220 are similar device, so this checklist applies to both devices. Use this information to check the connectivity for each device on a system schematic.

This document is intended to aid design at the system level for general applications but should not be the only resource used. In addition to this list, customers are advised to use the information in the HD3SS3212 and HD3SS3220 data sheet, EVM User's Guide and associated documents to gain a full understanding of device functionality.

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1 Schematic Checklist for HD3SS3212 and HD3SS3220

Table 1. Schematic Checklist⁽¹⁾⁽²⁾⁽³⁾

| Pin Name | HD3SS3220 Pin Number | HD3SS3212 Pin Number | Pin Description | Recommendation |
|---------------|----------------------|----------------------|--|---|
| TXP (A0P) | 6 | 3 | Host, device SuperSpeed TX positive | No AC cap needed if TX1, TX2 has AC cap |
| TXN (A0N) | 7 | 4 | Host, device SuperSpeed TX negative | No AC cap needed if TX1, TX2 has AC cap |
| RXP (A1P) | 9 | 7 | Host, device SuperSpeed RX positive | Biased by host controller |
| RXN (A1N) | 10 | 8 | Host, device SuperSpeed RX negative | Biased by host controller |
| TXP1 (B0P) | 17 | 19 | USB Type-C port SuperSpeed TXP1 positive | Need 100-nf AC cap |
| TXN1 (B0N) | 16 | 18 | USB Type-C port SuperSpeed TXN1 negative | Need 100-nf AC cap |
| RXP1 (B1P) | 15 | 17 | USB Type-C port SuperSpeed RXP1 positive | Biased by host controller |
| RXN1 (B1N) | 14 | 16 | USB Type-C port SuperSpeed RXN1 negative | Biased by host controller |
| TXP2 (C0P) | 21 | 15 | USB Type-C port SuperSpeed TXP2 negative | Need 100-nf AC cap |
| TXN2 (C0N) | 20 | 14 | USB Type-C port SuperSpeed TXN2 negative | Need 100-nf AC cap |
| RXP2 (C1P) | 19 | 13 | USB Type-C port SuperSpeed RXP2 negative | Biased by host controller |
| RXN2 (C1N) | 18 | 12 | USB Type-C port SuperSpeed RXN2 negative | Biased by host controller |
| ENz_Mux (OEn) | 12 | 2 | Active low MUX enable | Adding a Cap to GND |
| SEL | | 9 | Port select pin, L: A to B H: A to C | |

- (1) When using the 3.3-V supply for I²C pullup, the customer must ensure that the VDD is 3 V, and above. Otherwise, the I²C may backpower the device.
- (2) When VDD5 is off, the HD3SS3220 non-failsafe pins (DIR, VBUS_DET, ADDR, OUT[3:1] pins) could back-drive the HD3SS3220 device if not handled properly. When necessary to pull these pins up, it is recommended to pull up DIR, ADDR, and INT_N, OUT3 to the VDD5 supply of the device. The VBUS_DET must be pulled up to VBUS through a 900-kΩ resistor.
- (3) The HD3SS3220 device requires a common mode biasing of 0 V to 2 V. If the host receiver has bias voltage outside this range, appropriate additional AC coupling caps and biasing of HD3SS3220 RX pairs is needed.

Table 1. Schematic Checklist⁽¹⁾⁽²⁾⁽³⁾ (continued)

| Pin Name | HD3SS3220 Pin Number | HD3SS3212 Pin Number | Pin Description | Recommendation |
|---------------|-------------------------|-------------------------|---|--|
| ENn_CC | 29 | | Enable CC controller, active low | |
| CC1 | 2 | | USB Type-C configuration channel 1 | |
| CC2 | 1 | | USB Type-C configuration channel 2 | |
| CURRENT_MODE | 3 | | Tri-level input to indicate current advertisement in DFP, UFP does not matter | Pullup resistor varied due to different current mode |
| PORT | 4 | | Tri-level input to indicate port mode | DFP: pullup to VDD; UFP: pulldown to GND; DRP: NC |
| VBUS_DET | 5 | | 5–28 Vbus input pin | 900-kΩ external resistor between Vbus and VBUS_DET |
| ADDR | 22 | | Tri-level input pin to indicate I2C or GPIO mode | H: pullup to VDD, I2C address 0x67; L: pulldown to GND, I2C address 0x47; NC: GPIO |
| ID | 27 | | Open drain output, low when CC pin detect device attached in DFP mode | 200-kΩ pullup to VDD5 |
| VCONN_FAULT_N | 24 | | Open drain output, low when VCONN overcurrent detected | 200-kΩ pullup to VDD5 |
| INT_OUT3 | 23 | | In I2C, its INT open drain output, active low; in GPIO, OUT3 is used as audio accessory detection | 200-kΩ pullup to VDD5 |
| DIR | 11 | | USB Type-C plug orientation | 200-kΩ pullup to VCC33 |
| SDA_OUT1 | 25 | | In I2C: this pin is used as I2C communication data signal; In GPIO, this pin is used as current mode detection | 4.7-kΩ pullup to IO supply (1.8 V or 3.3 V) |
| SCL_OUT2 | 26 | | In I2C: this pin is used as I2C communication clock signal; In GPIO, this pin is used as current mode detection | 4.7-kΩ pullup to IO supply(1.8 V or 3.3 V) |
| VCC33 (VCC) | 8 | 6 | 3.3-V supply | Decoupling capacitor near the pin |
| VDD5 | 30 | | 5-V supply | Should be > 5 V |
| GND | 13, 28 | 5, 11, 20 | Ground | |
| Thermal Pad | | | | Must be connected to GND |

2 References

1. Texas Instruments, [HD3SS3220 USB Type-C™ DRP Port Controller With SuperSpeed 2:1 MUX Data Sheet](#)
2. Texas Instruments, [HD3SS3212x Two-Channel Differential 2:1/1:2 USB3.1 MUX/DEMUX Data Sheet](#)
3. Texas Instruments, [HD3SS3220 DFP Dongle Evaluation Module User's Guide](#)
4. Texas Instruments, [HD3SS3212 Evaluation Module User's Guide](#)

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