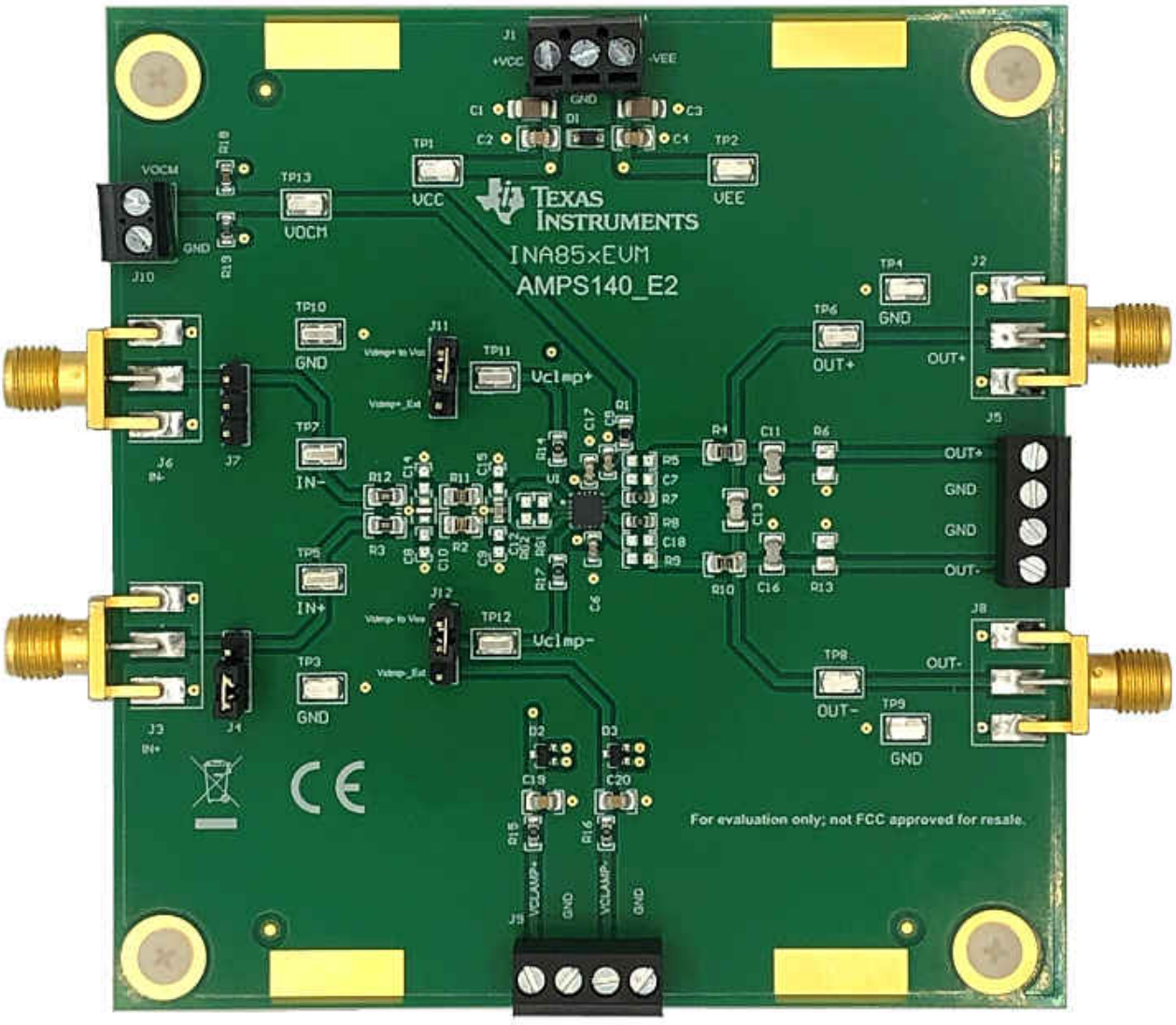
*User's Guide*

# *INA851 Evaluation Module*


**ABSTRACT**


This user's guide contains information and support documentation for the INA851 evaluation module (EVM). Included are the circuit description, jumper settings, required connections, printed circuit board (PCB) layout, schematic, and bill of materials of the INA851EVM. Throughout this document, the terms evaluation board, evaluation module, and EVM are synonymous with the INA851EVM.

# Table of Contents



## List of Figures



## List of Tables



## Trademarks

# 1 Overview

The INA851 is a high-precision instrumentation amplifier with differential outputs that is optimized to drive high-performance analog-to-digital converters (ADCs) with fully differential inputs. A single external resistor sets any gain from 0.2 V/V to 10,000 V/V. The device features super-beta input transistors from Texas Instruments, which provide ultra-low input offset voltage, offset drift, input bias current, input voltage noise, and current noise. For a full list of electrical characteristics for the INA851, see the *INA851 Precision, Fully Differential Output, Instrumentation Amplifier* data sheet.

## 1.1 Related Documentation

The following document provides information regarding Texas Instruments integrated circuits used in the assembly of the INA851EVM. This user's guide is available from the TI website under literature number SBOU273. Any letter appended to the literature number corresponds to the document revision that is current at the time of the writing of this document. Newer revisions may be available from the TI website at , or call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center at (972) 644-5580. When ordering, identify the document by both title and literature number.

**Table 1-1. Related Documentation**

| Device | Literature Number |
|---|---|
| INA851 | SBOS999 |

## 1.2 Electrostatic Discharge Caution

**CAUTION**

Many of the components on the INA851EVM are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap at an approved ESD workstation.

## 1.3 Hot Surface Warning

**WARNING**

Device may become hot under high-current conditions. Take care when handling the EVM.

## 2 EVM Circuit Description

This EVM provides access to the features and measures the performance of the INA851. By default, the INA851EVM instrumentation amplifier is configured in a gain of 1 V/V. The evaluation board provides optional footprints for gain resistors RG1 and RG2 to modify the input-stage instrumentation-amplifier gain. Optional footprints R5 and R9 can be populated with 0-Ω jumpers to set the output stage gain to 0.2 V/V. The INA851 incorporates features that simplify interfacing to a fully-differential ADC. The VOCM connector sets the output common-mode voltage. If the VOCM connector is not driven, the output common-mode voltage defaults to the INA851 midsupply value. Clamp pins are provided to limit the INA851 output voltage level, which can be applied to the ADC inputs. The output clamp pins, VCLAMP+ and VCLAMP–, are accessible using connector J9. Selectable jumpers J11 and J12 set the output clamp voltage level to the INA851 supplies (default), or to external voltages using connector J9. A simplified block diagram of the INA851EVM is displayed in Figure 2-1. For a full schematic of the INA851EVM, see Figure 7-1.

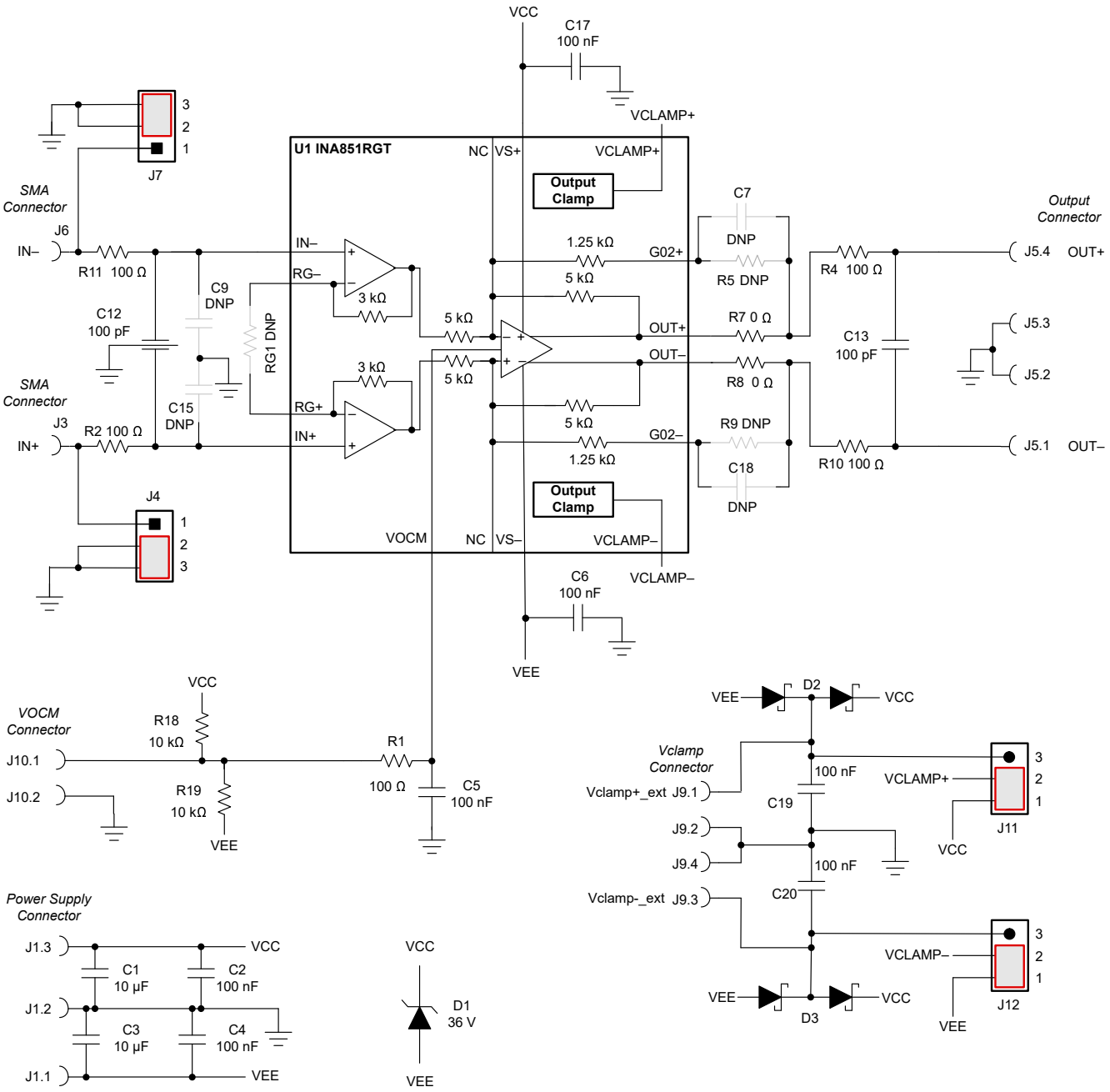



**Figure 2-1. INA851EVM Simplified Schematic**

## 3 Jumper Settings

Figure 3-1 details the default jumper settings of the INA851EVM. Table 3-1 explains the configuration for these jumpers.

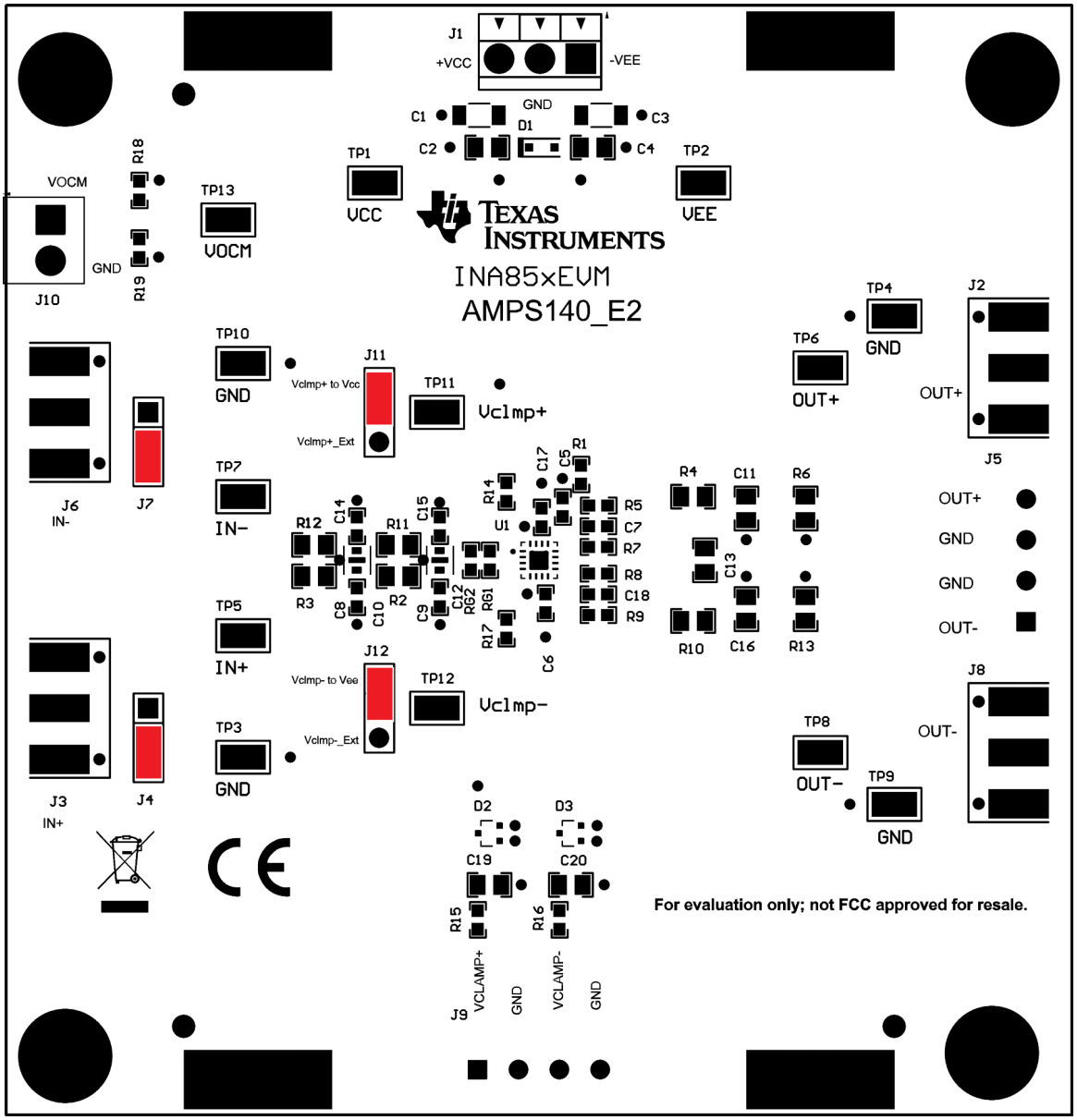



**Figure 3-1. INA851EVM Default Jumper Settings**

**Table 3-1. Default Jumper Configuration**

| Jumper | Function | Default Position | Description |
|---|---|---|---|
| J4 | Positive (noninverting) input IN+ | Shunt 2-3 | Shunt 2-3: Input signal to SMA connector J3<br>Shunt 1-2 connects IN+ to GND |
| J7 | Negative (inverting) input IN– | Shunt 2-3 | Shunt 2-3: Input signal to SMA connector J6<br>Shunt 1-2 connects IN– to GND |
| J11 | VCLAMP+ Connection | Shunt 1-2 | Shunt 1-2: Sets level of output VCLAMP+ to +VCC supply<br>Shunt 2-3 connects VCLAMP+ to external connector J9 pin 3 |
| J12 | VCLAMP– Connection | Shunt 1-2 | Shunt 1-2: Sets level of output VCLAMP-to-VEE supply<br>Shunt 2-3 connects VCLAMP– to external connector J9 pin 1 |

# 4 Power-Supply Connections

The power-supply connections for the INA851EVM are provided through connector J1 at the top of the EVM. The positive power-supply connection is labeled +VCC, the negative power-supply connection is labeled –VEE, and the ground connection is labeled GND. To connect power to the INA851EVM, insert wires into each terminal of J1 and then tighten the screws to make the connection. Table 4-1 summarizes the pin definition for supply connector J1, and the allowed voltage range for each supply connection.

**Table 4-1. INA851EVM Supply-Range Specifications**

| Pin Number | Supply Connection | Voltage Range |
|---|---|---|
| J1.3 | Positive supply (+VCC) | Single supply, $V_S$ = (+VCC): 8 V to 36 V<br>Dual supply, $V_S$ = (+VCC) – (–VEE): 4 V to 18 V |
| J1.2 | Ground | 0 V |
| J1.1 | Negative supply (–VEE) | Single supply, $V_S$ = (+VCC): 0 V (GND)<br>Dual supply, $V_S$ = (+VCC) – (–VEE): –4 V to –18 V |

Figure 4-1 shows the INA851EVM voltage supply connections.

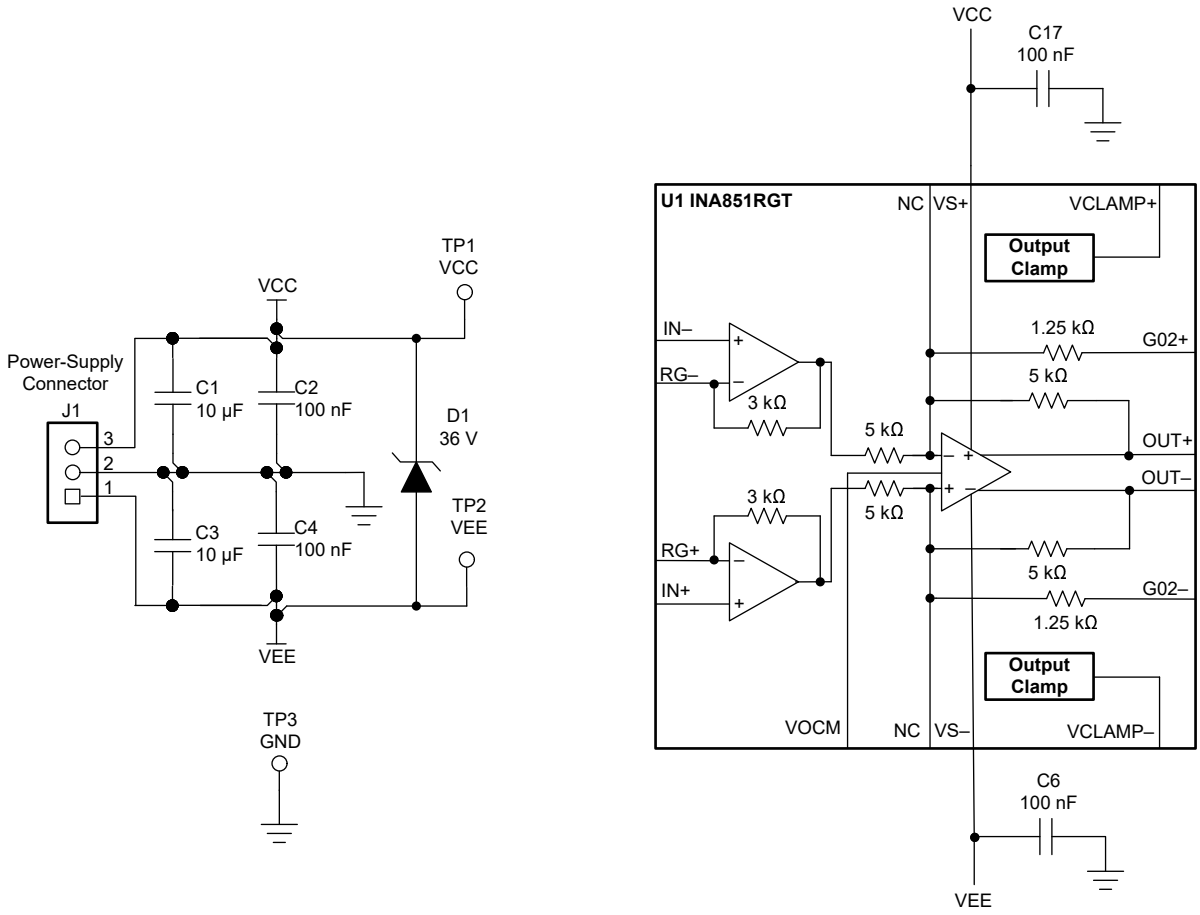



**Figure 4-1. INA851EVM Voltage Supply Connections**

## 5 Input and Output Connections

The instrumentation amplifier input signal connections for the INA851EVM are provided through the use of SMA connectors J3, J6, and test points TP5, TP7 located at the left of the EVM. The VOCM input is provided through screw terminal connector J10, located on the left of the board.

By default, the output clamp voltage levels VCLAMP+ and VCLAMP– are set to the INA851 positive (+VCC) and negative (–VEE) supplies, respectively. The VCLAMP+ pin is connected to +VCC through jumper J11 1-2, and the VCLAMP– pin is connected to –VEE through J12 1-2. Screw terminal connector J9 provides access to the output clamp pins. To set the voltage level of the clamps with an external supply, shunt jumper J11 2-3 to access the VCLAMP+ using connector J9.1. In a similar fashion, shunt jumper J12 2-3 to access the VCLAMP– pin using connector J9.3.

The differential output amplifier connections are provided through screw terminal connector J5, SMA connectors J2 and J8, and test points TP6 and TP8, located at the right side of the EVM. A simplified diagram of the INA851EVM input and output connections is displayed in Figure 5-1.

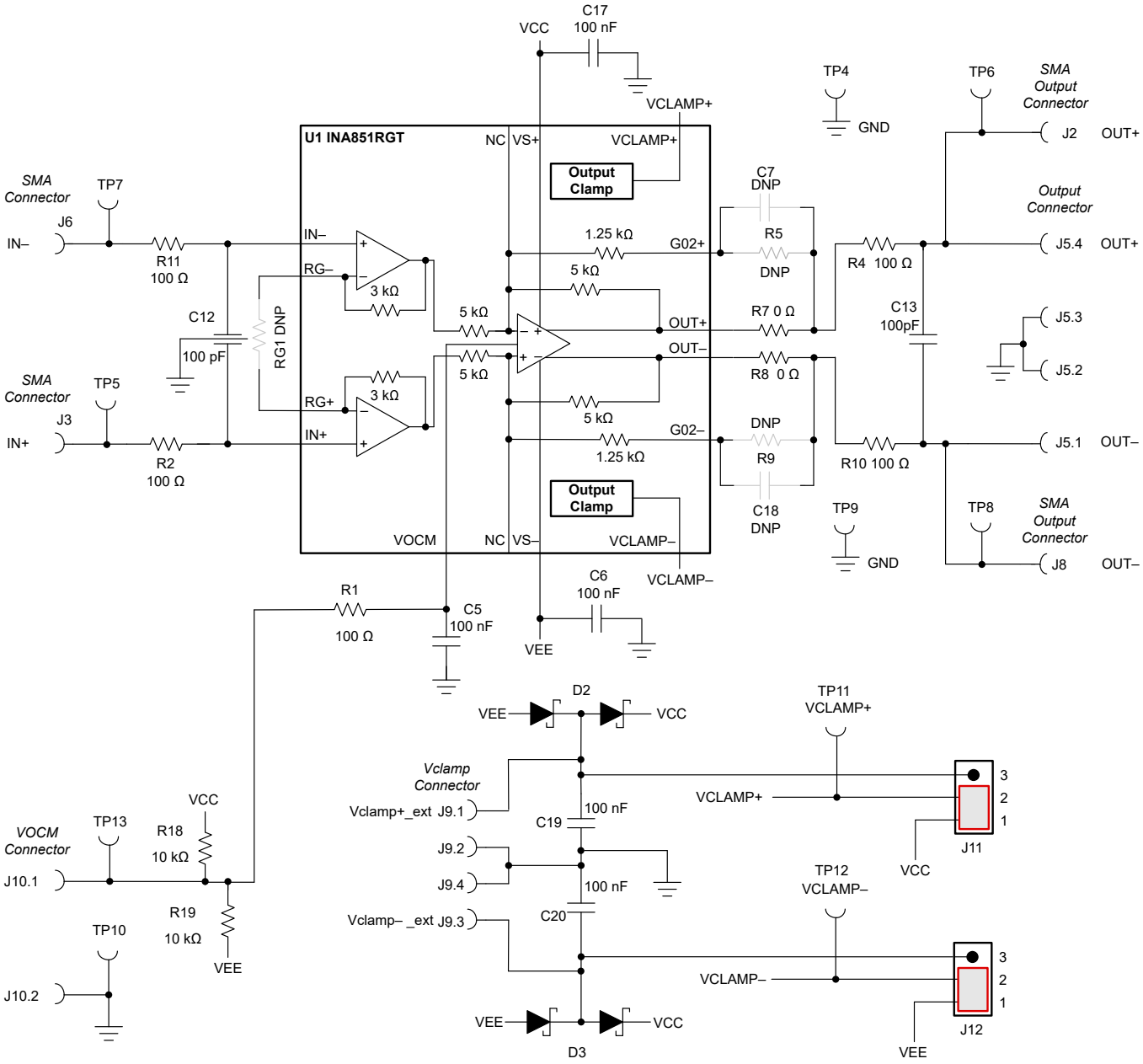



**Figure 5-1. INA851EVM Input and Output Connections**

Table 5-1 summarizes the input and output connectors and corresponding test points.

**Table 5-1. INA851EVM Input and Output Connections**

| Connector Designator | Signal | Comment | Test Point |
|---|---|---|---|
| J3 | IN+ | SMA | TP5 |
| J6 | IN– | SMA | TP7 |
| J2 | OUT+ | SMA | TP6 |
| J8 | OUT– | SMA | TP8 |
| J5.4 | OUT+ | Screw terminal | TP6 |
| J5.3 | GND | Screw terminal | TP4 |
| J5.2 | GND | Screw terminal | TP9 |
| J5.1 | OUT– | Screw terminal | TP8 |
| J10.1 | VOCM | Screw terminal | TP13 |
| J10.2 | GND | Screw terminal | N/A |
| J9.1 | VCLAMP+ external | Screw terminal | N/A |
| J9.2 | GND | Screw terminal | N/A |
| J9.3 | VCLAMP– external | Screw terminal | N/A |
| J9.4 | GND | Screw terminal | N/A |

# 6 Modifications

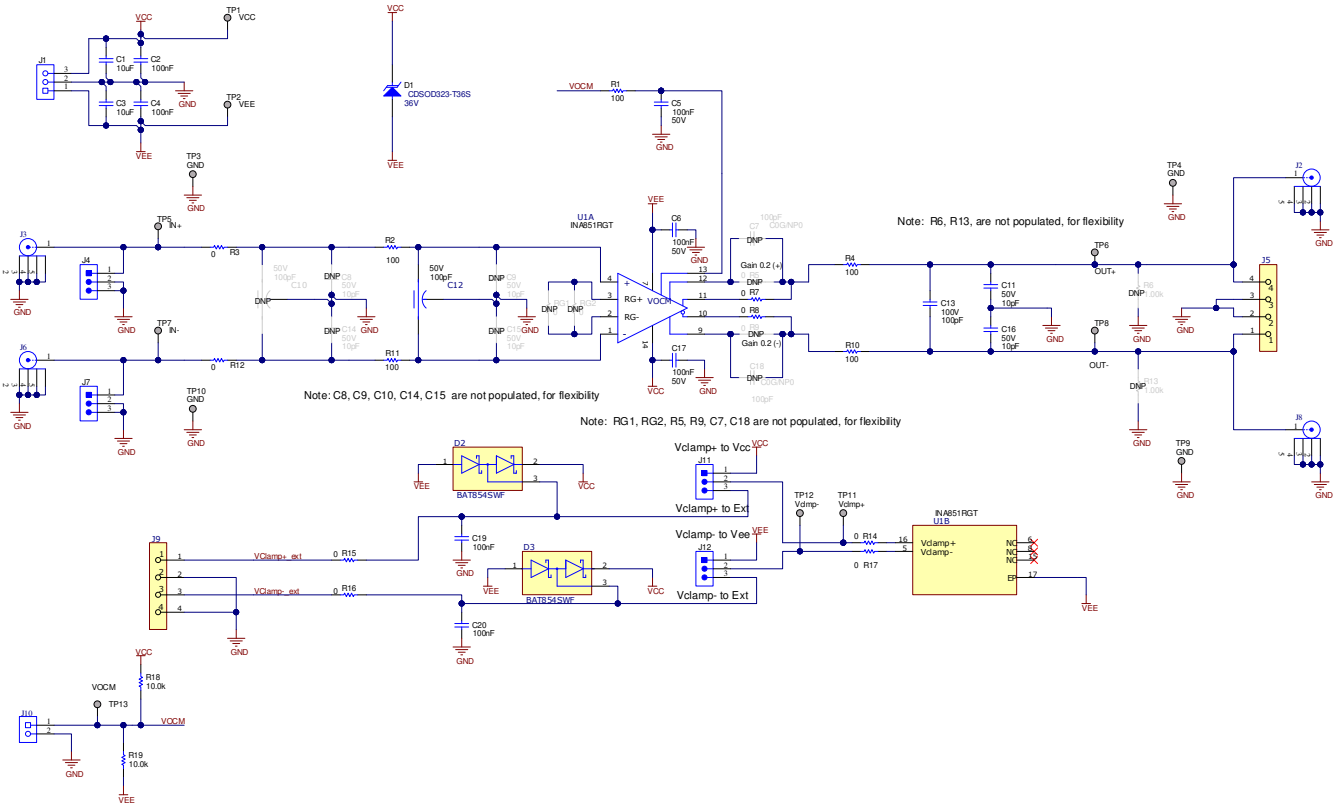
By default, the INA851EVM is populated with the INA851 device configured in gain of 1 V/V. However, for flexibility, the PCB layout has additional unpopulated, passive component footprints for gain resistors RG1 and RG2 to set the front-end amplifier gain. Optional footprints for jumper resistors R5 and R6 are provided to set the output stage to gain of 0.2 V/V. In addition, the evaluation board provides footprints R3, R12, C10, C8, and C14 for optional input low-pass filters, and footprints for load resistors R6 and R13. These additional component footprints in the layout allow the user to customize the evaluation circuit. For a full schematic of the INA851EVM, see Figure 7-1.

# 7 Schematic, PCB Layout, and Bill of Materials

This section contains the schematic, PCB layout, and bill of materials for the INA851EVM.

## 7.1 Schematic

Figure 7-1 illustrates the EVM schematic.




Note: DNP components are not populated.

**Figure 7-1. INA851EVM Schematic**

## 7.2 PCB Layout

The INA851EVM is a four-layer PCB design. Figure 7-2 to Figure 7-6 show the PCB layer illustrations. The top layer consists of all signal path traces, and is poured with a solid ground plane. A symmetrical board layout is used at the differential inputs and outputs to keep good performance matching and improve common-mode noise rejection. Route traces as symmetrically as possible for both positive and negative pathways. Gain resistors RG1 and RG2 are placed on the top layer in close proximity to the device to reduce parasitic capacitance. Capacitor C5 is placed in close proximity to VOCM to avoid injecting common-mode noise. Decoupling capacitors C6, and C17 are positioned on the top layer as close as possible to the power-supply pins of the device. The second internal layer is a dedicated solid GND plane. Independent vias are placed at the ground connection of every component to provide a low-impedance path to ground. The third internal layer and bottom layer route the power supplies and the VCLAMP+ and VCLAMP– connections.

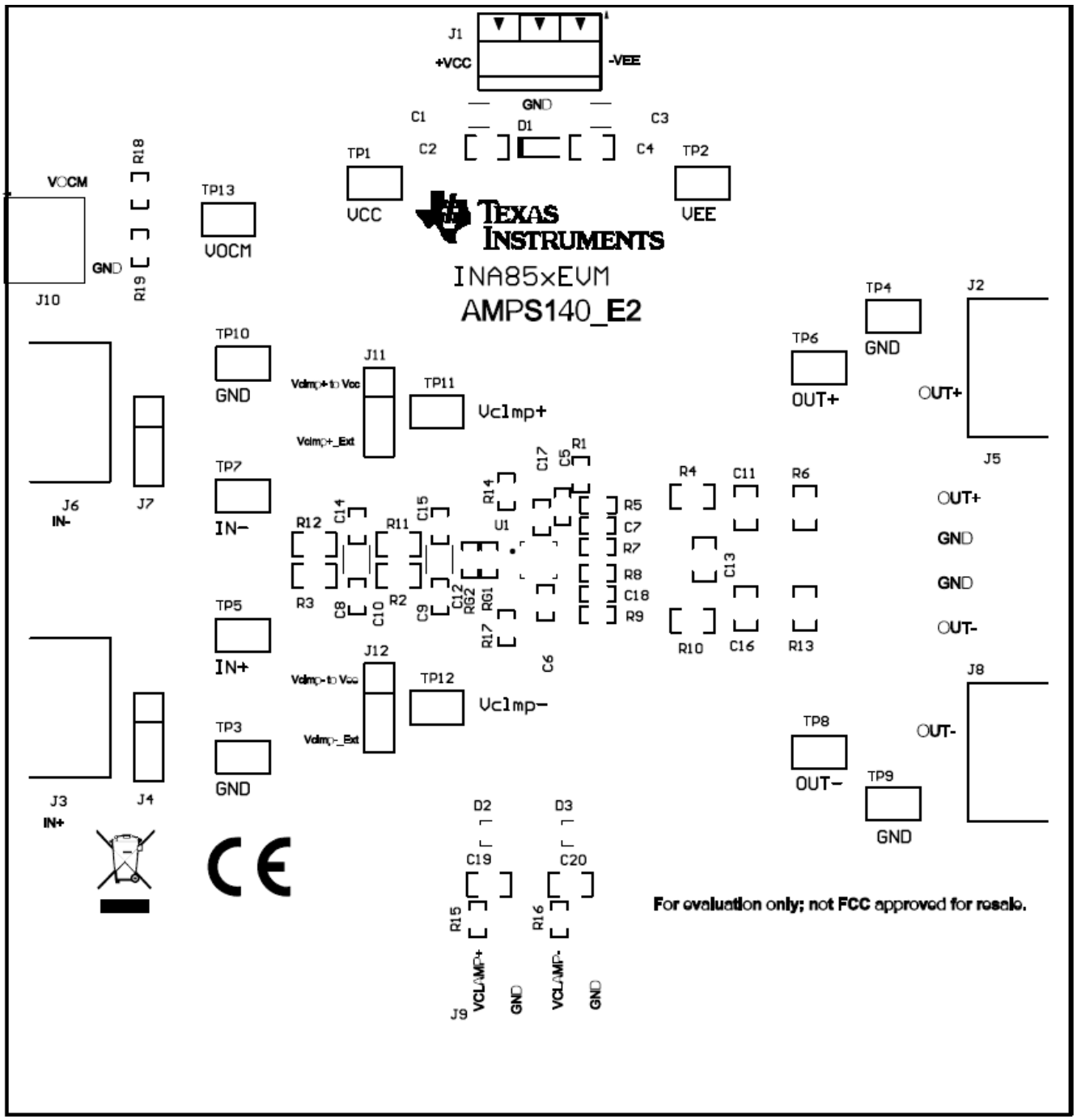



**Figure 7-2. Top Overlay PCB Layout**

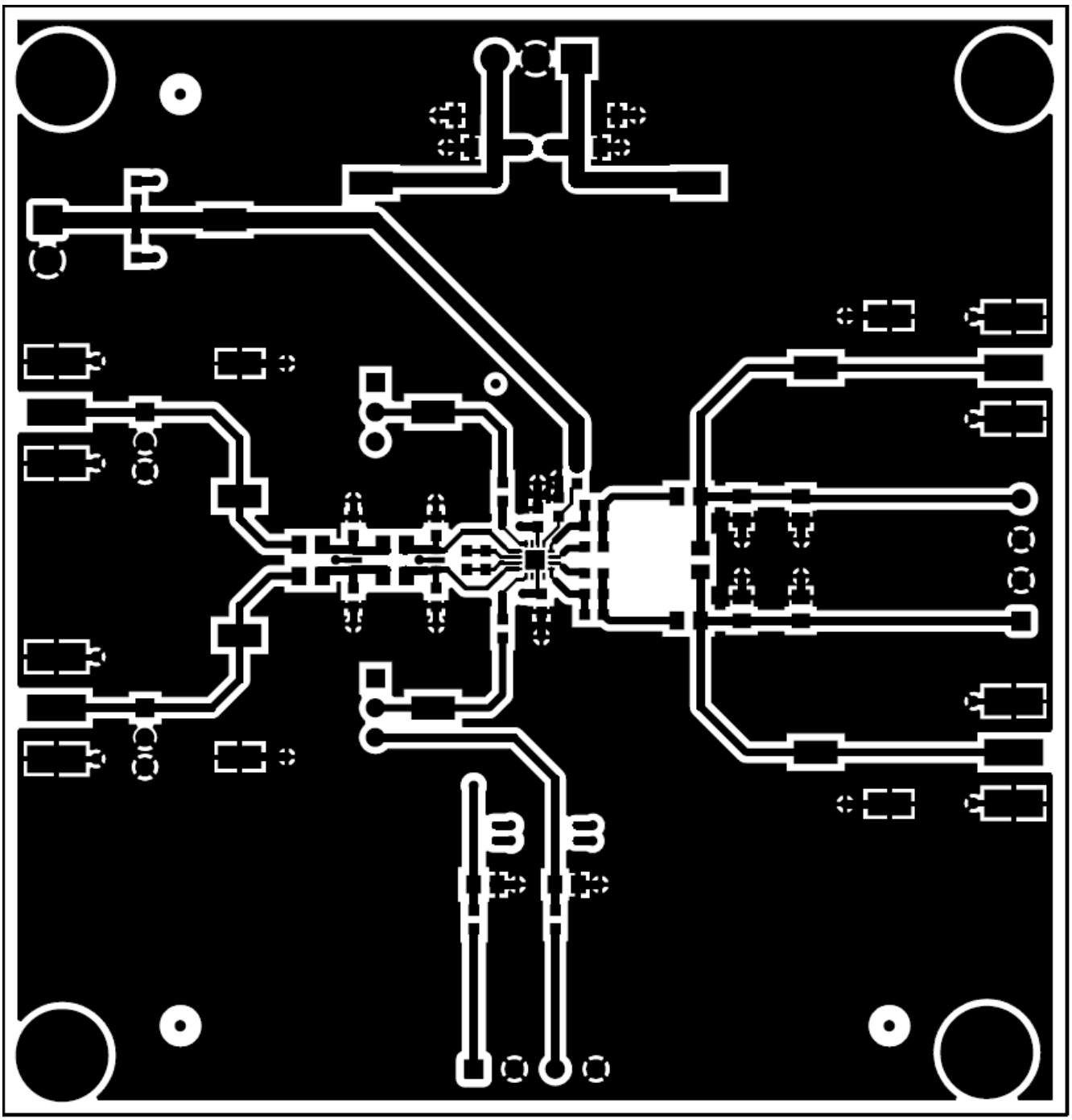


**Figure 7-3. Top Layer PCB Layout**

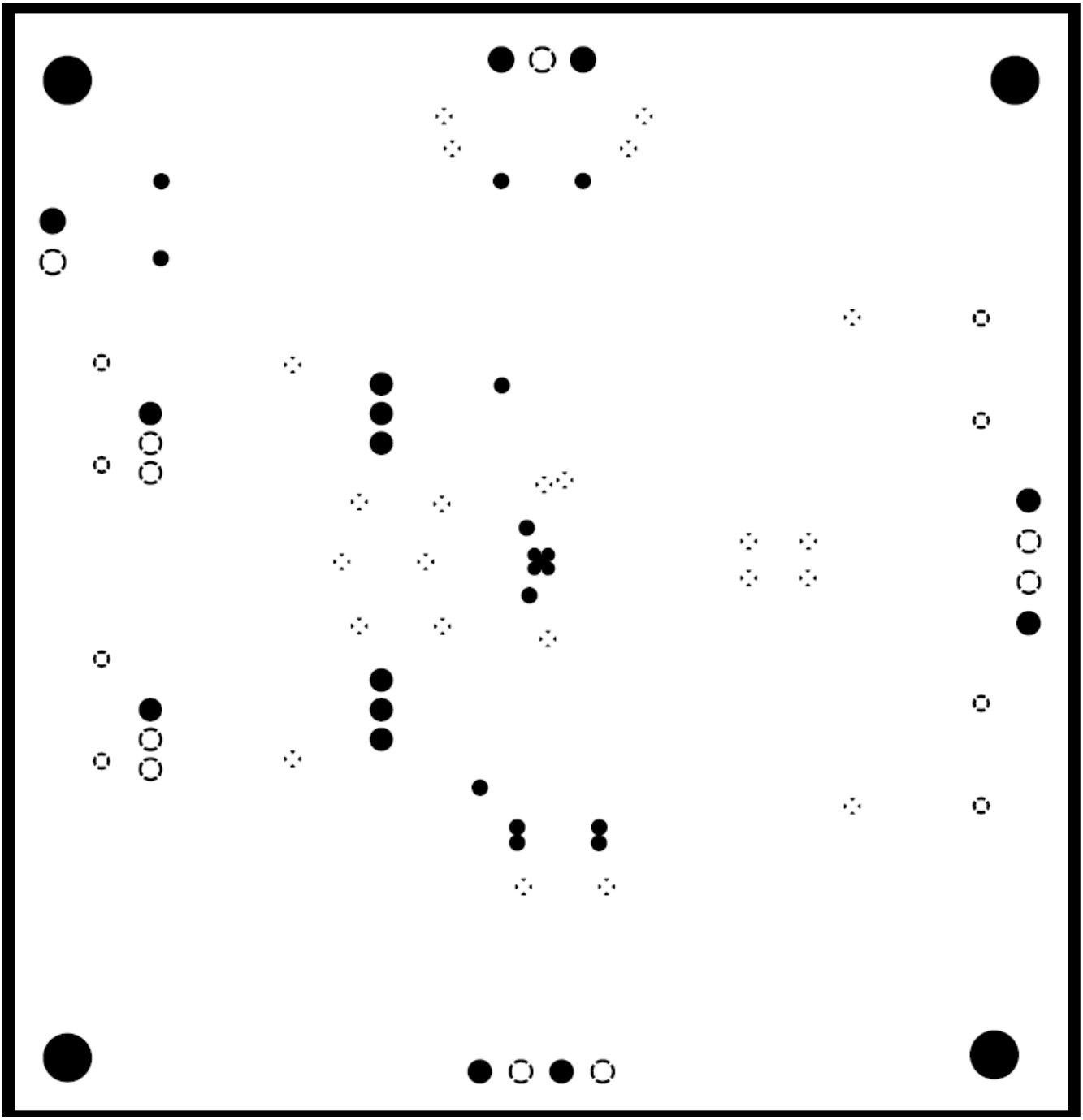


**Figure 7-4. Ground Layer PCB Layout**

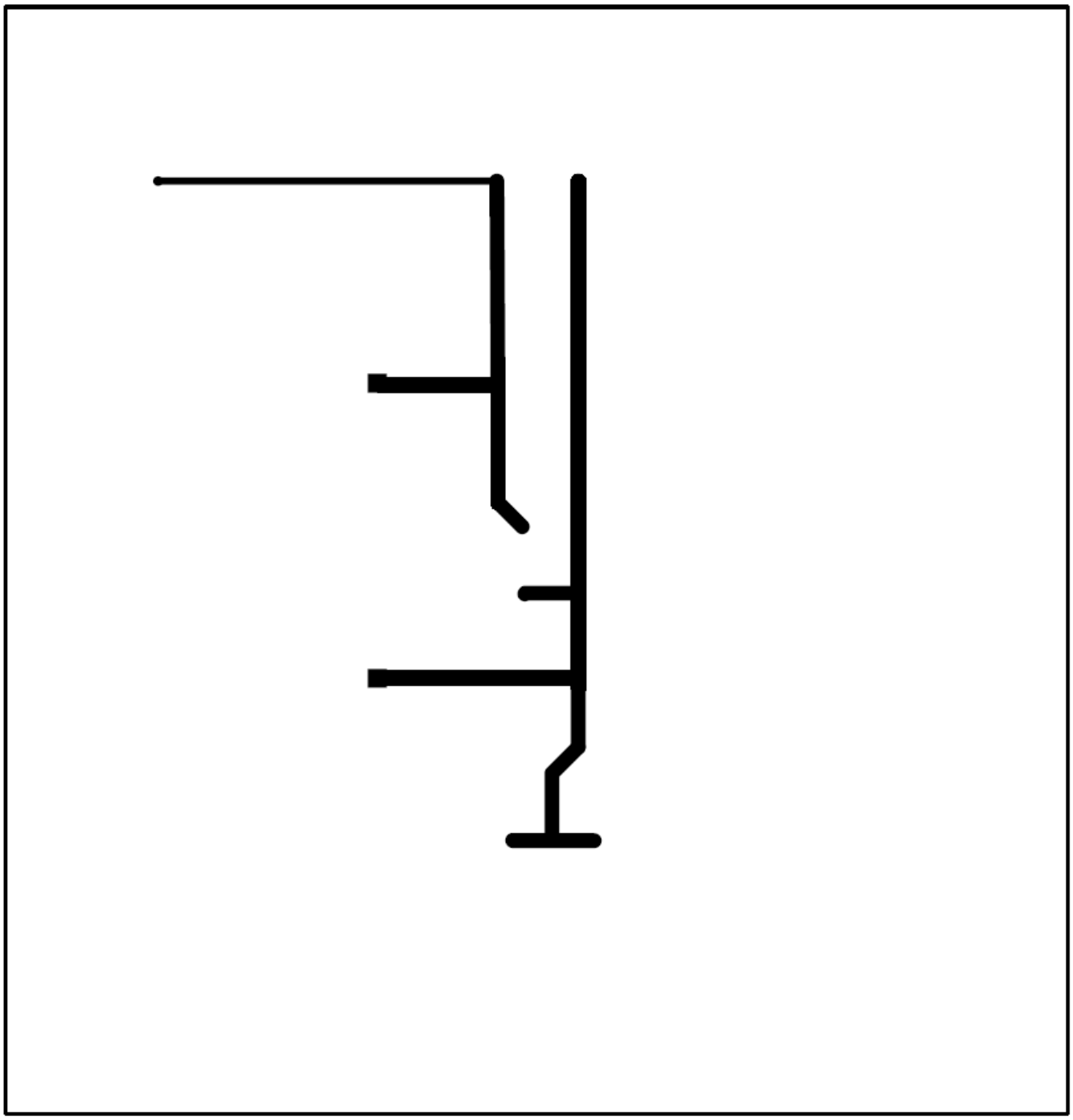


**Figure 7-5. Power Layer PCB Layout**

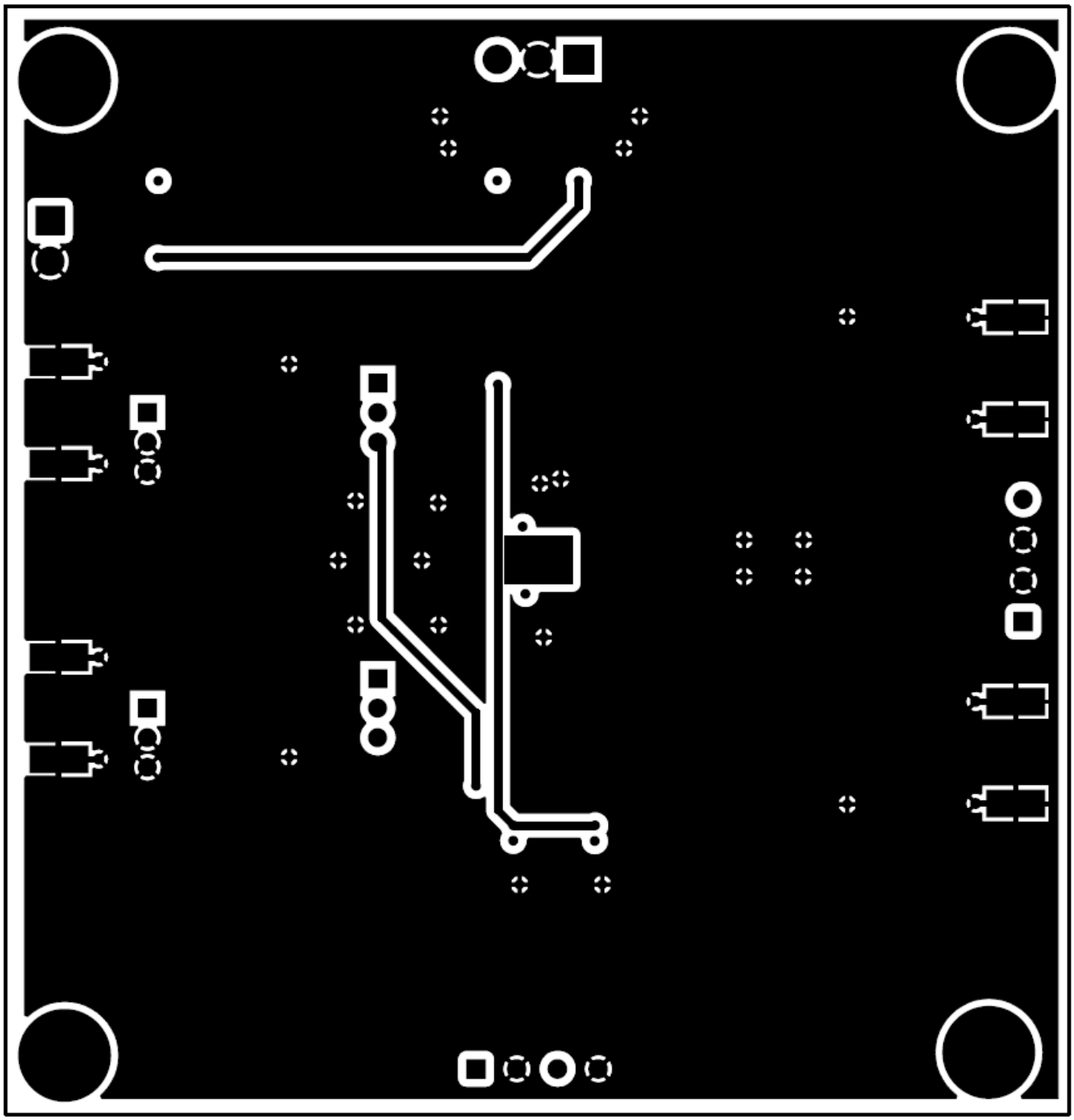


**Figure 7-6. Bottom Layer PCB Layout**

## 7.3 Bill of Materials

Table 7-1 lists the INA851EVM bill of materials (BOM).

**Table 7-1. INA851EVM Bill of Materials**

| Designator | Quantity | Value | Description | Package Reference | Part Number | Manufacturer |
|---|---|---|---|---|---|---|
| !PCB1 | 1 | | Printed Circuit Board | | AMPS140 | Any |
| C1, C3 | 2 | 10uF | CAP, CERM, 10 uF, 35 V, +/- 10%, X7R, 1206 | 1206 | C3216X7R1V106K160AC | TDK |
| C2, C4, C19, C20 | 4 | 0.1uF | CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0805 | 0805 | 08055C104KAT2A | AVX |
| C5, C6, C17 | 3 | 0.1uF | CAP, CERM, 0.1 uF, 50 V, +/- 5%, X7R, 0603 | 0603 | C0603C104J5RACTU | Kemet |
| C11, C16 | 2 | 10pF | CAP, CERM, 10 pF, 50 V, +/- 5%, C0G/NP0, 0805 | 0805 | 08055A100JAT2A | AVX |
| C12 | 1 | 100pF | 100 pF ±20% 50V Ceramic Capacitor C0G, NP0 0603 (1608 Metric) | 0603 | 500X14N101MV4T | Johanson Dielectrics |
| C13 | 1 | 100pF | CAP, CERM, 100 pF, 100 V, +/- 5%, C0G/NP0, 0805 | 0805 | C0805C101J1GACTU | Kemet |
| D1 | 1 | 39V | Zener Diode 39 V 200 mW ±5% Surface Mount SOD-323 | SOD-323 | BZX384C39-E3-08 | Vishay Semiconductor |
| D2, D3 | 2 | | Diode Array 1 Pair Series Connection Schottky 40 V 200mA (DC) Surface Mount SC-70, SOT-323 | SOT-323 | BAT854SWF | Nexperia |
| H1, H2, H3, H4 | 4 | | Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead | Screw | NY PMS 440 0025 PH | B&F Fastener Supply |
| H5, H6, H7, H8 | 4 | | Standoff, Hex, 0.5"L #4-40 Nylon | Standoff | 1902C | Keystone |
| J1 | 1 | | Terminal Block, 3.5mm Pitch, 3x1, TH | 10.5x8.2x6.5mm | ED555/3DS | On-Shore Technology |
| J2, J3, J6, J8 | 4 | | Connector, End launch SMA, 50 ohm, SMT | End Launch SMA | 142-0701-801 | Cinch Connectivity |
| J4, J7, J11, J12 | 4 | | Header, 100mil, 3x1, Gold, TH | PBC03SAAN | PBC03SAAN | Sullins Connector Solutions |
| J5, J9 | 2 | | TERM BLOCK 3.5MM VERT 4POS PCB | HDR4 | OSTTE040161 | On Shore Technology |
| J10 | 1 | | Terminal Block, 3.5mm Pitch, 2x1, TH | 7.0x8.2x6.5mm | ED555/2DS | On-Shore Technology |
| R1 | 1 | 100 | RES, 100, 1%, 0.1 W, 0603 | 0603 | RC0603FR-07100RL | Yageo |
| R2, R4, R10, R11 | 4 | 100 | RES, 100, 0.1%, 0.125 W, 0805 | 0805 | RT0805BRD07100RL | Yageo America |
| R3, R12 | 2 | 0 | RES, 0, 5%, 0.125 W, AEC-Q200 Grade 0, 0805 | 0805 | ERJ-6GEY0R00V | Panasonic |
| R7, R8, R14, R15, R16, R17 | 6 | 0 | RES, 0, 5%, 0.1 W, 0603 | 0603 | RC0603JR-070RL | Yageo |
| R18, R19 | 2 | 10.0k | RES, 10.0 k, 1%, 0.1 W, 0603 | 0603 | ERJ-3EKF1002V | Panasonic |
| SH-J1, SH-J2, SH-J3 | 3 | 1x2 | Shunt, 100mil, Flash Gold, Black | Closed Top 100mil Shunt | SPC02SYAN | Sullins Connector Solutions |
| TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13 | 13 | | Test Point, Miniature, SMT | Test Point, Miniature, SMT | 5019 | Keystone |
| U1 | 1 | | Precision, Fully Differential Output, Instrumentation Amplifier | VQFN16 | INA851RGT | Texas Instruments |

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