

Understanding electromagnetic compliance tests in digital isolators



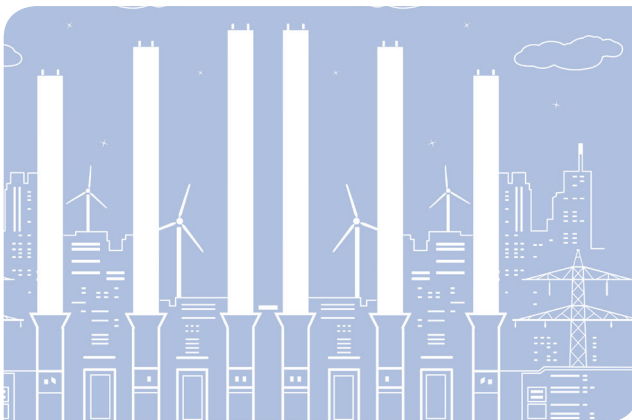
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Choosing the right digital isolator requires a clear understanding of electromagnetic compliance test methods and results, after accounting for common performance improvement techniques.

For a system designer working with high voltage and high-voltage isolation, one of the most important tasks is to choose the right digital isolator for the system. Electromagnetic compatibility (EMC) is a key consideration on which this choice hinges. An in-depth understanding of how the different EMC tests are performed help in making this decision correctly. It also helps in differentiating the isolator's true performance in the actual system versus the claimed performances on a far from practical test setup. This paper discusses EMC standards and test setups for the relevant EMC parameters.

In the exacting conditions of an industrial environment, the reliability and longevity of a communication link relies heavily on the individual system component's robust EMC. Digital isolators play a major part in ensuring continued, reliable performance of these systems – even during extremely harsh stresses like lightning strikes, high electrostatic discharges, and electromagnetically-coupled, high-energy transients from neighboring high-power systems, and so on. Hence, assessing the performance of these digital isolators during such stresses is a critical but challenging part of choosing the right isolator.

A clear understanding of the setup in which these tests are done is important to avoid common mistakes or pitfalls that can affect the results.



There are standards and regulations that must be met to ensure that the digital isolators aid the smooth functioning of the intended final system. In this document we describe some of these key isolation and EMC test and discuss the performance of reinforced digital isolators.

EMC test setup vs. a typical system

Performance in EMC tests can appear to be better, artificially, by using costly or impractical board level implementations.

Typical methods include:

- Adding large and expensive high-voltage capacitors across the isolation barrier.
- Complex PCB plane designs intended to increase capacitance between both sides of the isolation barrier.
- Performing tests on multiple custom boards, each optimized for one of the above tests. For example, using a small two-layer coupon card for radiated susceptibility tests and a large board with expansive planes for across the barrier ESD tests.

Though such methods can be considered for the final system design, they should not be employed when evaluating/comparing the performance of a digital isolator by itself. The above methods, in one way or the other, either block or divert the actual stress from reaching the isolators.

Such methods, instead of exposing the true performance of the isolator, are designed to protect it from the full force of the stress. This is where a careful review of test setups for EMC tests becomes critical for a system designer.

A good EMC test setup should:

- Employ simple PCB design practices that are already in common use
- Have basic components and blocks seen in most common digital isolator systems
- Not be architected to make a device pass a standard test, but to identify its inherent capability
- Not be changed from one test to another unless the standard requires it

EMC/EMI board

The ISO7842 EMC / electromagnetic interference (EMI) board shown in Figure 1, (block diagram) and Figure 2 (photograph) meets the above expectations. We used this board to evaluate EMC.

Electrostatic discharge immunity

Electrostatic discharge (ESD) is the transfer of charge between two objects at different potential and is caused by contact or an induced electric field. The transfer is characterized by a very high current in a short duration. The objects become charged by a mechanism called tribo-charging or tribo-electric charging. This happens whenever two dissimilar materials make contact and then are separated. The charging can be greatly increased when one of the materials is an insulator.

In many systems, board-level ESD protection circuits like TVS diodes are employed. But for digital isolators, ESD performance for strikes across the isolation barrier is a key metric as board-level ESD protection devices cannot be employed. This is because a major portion of the energy of an across the barrier strike appears as a common mode for an ESD protection device sitting on one side of the isolation barrier. JEDEC standard models such as human body model (HBM), charged device model (CDM) and

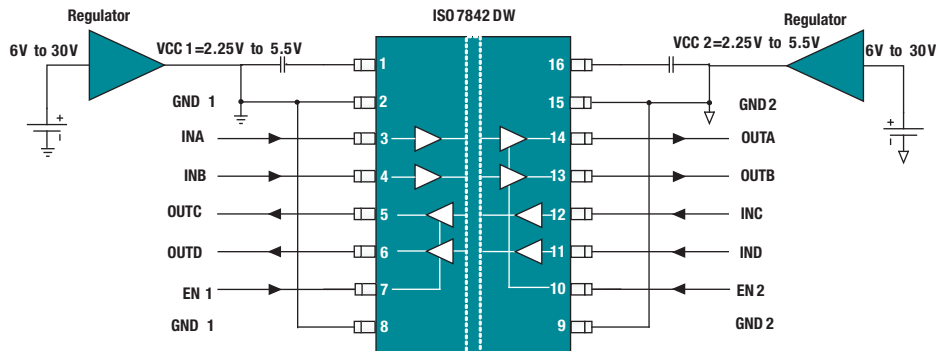


Figure 1. Block diagram of an EMC/EMI evaluation board

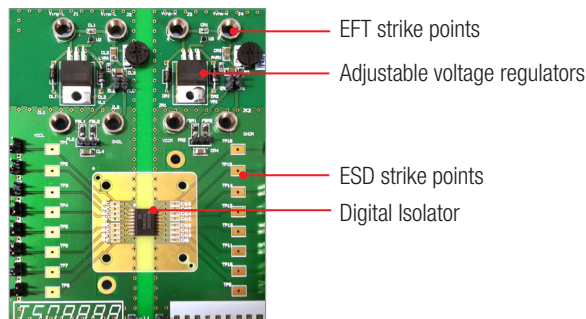


Figure 2. Block diagram of an EMC/EMI evaluation board

machine model (MM) are used to assess device-level ESD robustness, while the IEC 61000-4-2 standard defines the system-level ESD performance test. The graph in Figure 3 compares the stress seen by equipment under test (EUT) when subjected to ESD events as recommended in the above models.

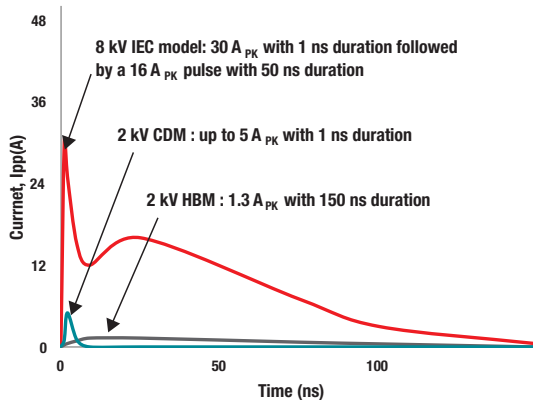


Figure 3. Comparison of stress due to different ESD models

IEC-61000-4-2 defines two discharge modes and four test levels of performance defined in Table 1 below.

Contact discharge		Air discharge	
Level	Test voltage kV	Level	Test voltage kV
1	2	1	2
2	4	2	4
3	6	3	8
4	8	4	15
X (1)	Special	X (1)	Special

Note 1: "X" is an open level. The level must be specified in the dedicated equipment specification. If higher voltages than those are specified, special test equipment may be required.

Table 1. IEC 61000-4-2 performance levels

Radiated susceptibility test

Radiated susceptibility is a measure of the system's ability to operate acceptably when subjected to an externally generated electromagnetic field. A radiated susceptibility test is also known as a radiated immunity test. A current is induced in a conductor in the presence of a changing electromagnetic field. The amplitude of the induced current and the voltages induced at the circuits at each end of the conductor are proportional to the inducing field strength.

The susceptibility threshold, or limit, of a system is the field strength that induces sufficiently high current to cause the system to no longer operate acceptably. Thus, at field levels below the susceptibility threshold, the device operates acceptably. At field levels above the susceptibility threshold, the device does not operate acceptably. This limit for a given system typically varies as a function of frequency.

Radiated susceptibility tests are performed on a device to determine whether the device is susceptible to electromagnetic fields having specified amplitude over a specified frequency range. If the device operates acceptably as the field is applied and swept over the specified frequency range, the device is considered to have passed. If not, it has failed. In many cases, a device that is adversely affected by the field returns to normal operation when the field is removed. Typically, radiated EMI occurs when the dimensions of the equipment being examined are of the similar magnitude as the wavelength of the interfering signal.

IEC-61000-4-3 is the relevant standard for this test. It is performed in a semi-anechoic chamber similar to the radiated emissions setup with only the signal chain reversed. The frequency range is swept from 80 to 1000 MHz. The modulation is 80 percent AM with a 1 kHz sine wave. The stress field levels up to which the system operates as expected is quoted as the system performance. The various test levels for 80 -1000 MHz as prescribed in the standard are shown in Table 2.

Level	Test field strength (V/m)
1	1
2	3
3	10
4	30
X (1)	Special

Note 1: "X" is an open level, The associated field strength may be any value. This level may be given in the product standard.

Table 2. IEC-61000-4-3 test levels

Electrical fast transient immunity

The test for electrical fast transients (EFT) or burst immunity, as defined by the IEC61000-4-4 standard, simulates the switching transients caused by the interruption of inductive loads, relay contact bounce, and so on. This test is performed on power, signal, and earth wires.

A burst is defined as a sequence of pulses of limited duration. In this case, a burst generator produces a sequence of test pulses with a decay time, down to 50 percent of the peak value, of less than 100 ns. The typical duration of a burst is 15 ms at a repetition rate of 5 kHz/100 kHz. The burst period, or the time from one burst start to the next, is 300 ms.

Significant characteristics of the test pulse are its short rise time, high repetition rate, and low energy content. This test requires the application of six burst frames of 10 seconds duration with 10 second pause intervals between frames (Figure 4).

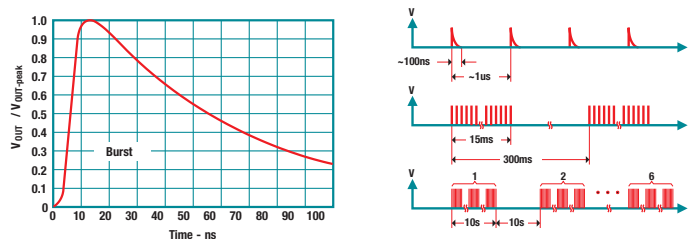


Figure 4. Voltage wave form of an EFT (burst) pulse and timing sequence of an entire test cycle

Table 3 shows the test levels specified in the IEC61000-4-4 standard.

Level	On power supply port PE		On I/O signal data and control ports	
	Voltage peak (kV)	Repetition rate (kHz)	Voltage peak (kV)	Repetition rate (kHz)
1	0	5 or 100	0	5 or 100
2	1	5 or 100	0	5 or 100
3	2	5 or 100	1	5 or 100
4	4	5 or 100	2	5 or 100
X (1)	Special	Special	Special	Special

Note 1: "X" is an open level. The level has to be specified in the dedicated equipment specification.

Table 3. IEC-61000-4-4 test levels

Conducted immunity

Conducted susceptibility or immunity is the ability of a system to operate acceptably when subjected to radio frequency voltage or current on interconnecting conductors. Typically such radio frequency noise is induced on electrical conductors from a variety of sources and coupling mechanisms. Load switching, electromagnetic fields and conducted emissions from equipment sharing the conductors are examples.

Generally, conducted susceptibility tests are intended to evaluate device response to low-mid frequency noise on the conductors, while radiated susceptibility tests are intended to test the response to mid-high frequency noise. Conducted susceptibility test signals are injected at a pre-determined point on the conductors. The injected signal may be voltage or a current. If the device operates acceptably as the signal is applied and

swept over the specified frequency range, the device is considered to have passed. Figure 5 shows setup for conducted susceptibility test. Conducted electromagnetic interferences occur when the dimensions of the equipment being examined are much less than the wavelength of the interfering signal. In this case, the interference is conducted to the device via an external cable.

The IEC-61000-4-6 standard describes the test conditions for the conducted immunity tests. There are two principal parameters defined in conducted RF tests: frequency range, and test level.

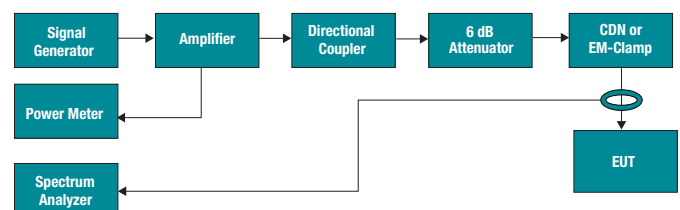


Figure 5. IEC-61000-4-6 test setup

A frequency range of 150 kHz minimum, 80 MHz typical, and 230 MHz maximum is given for general applications. The exact frequency range used for a test is defined in individual product standards and depends on the test object.

Frequency range is chosen depending on the cable size and EUT. Test level is a slightly ambiguous term when used in relation to actual tests. The levels given in the standards refer to the calibrated signal level into ideal impedance and with no modulation. What actually appears at the EUT during testing can be quite different, depending upon the EUT's impedance characteristics. Defined as volts root mean square (rms) into a 50 Ω matched load, the nominal test level chosen is entirely at the user's discretion, but should reflect the electromagnetic environment expected for normal operation of the equipment. The standards suggest levels of 1V, 3V and 10V.

Radiated emissions

Electromagnetic interference (EMI) is the disruption of proper operation of an electronic device, caused by an electromagnetic field generated by a different device. To prevent electronics from interfering with the operation of other devices, EMI is regulated by the government where the electronic device is being sold. There are several norms, for example, CISPR22 (EN 55022), FCC part 15. EMI is difficult to accurately predict, so it is important to minimize the known causes of EMI when planning your layout and design.

The international standard, EN 55022:2010, divides equipment, devices and apparatus into two classes:

1. Class A: equipment, device and apparatus that complies with EN 55022:2010 Class A emission requirements, but do not meet the EN 55022:2010 Class B emission requirements

2. Class B: equipment, device and apparatus intended for use in the domestic environment and meet EN 55022:2010 Class B emission requirements

Conducted emission requirements for mains / power supply ports and telecommunication ports must be satisfied in a frequency range of 150 kHz - 30 MHz. Radiated emission requirements must be satisfied in frequency ranges:

- 30 MHz-1 GHz, if internal oscillator frequency is up to 108 MHz
- 30 MHz-2 GHz, if internal oscillator frequency is up to 500 MHz
- 30 MHz-5 GHz, if internal oscillator frequency is up to 1 GHz
- 30 MHz-6 GHz, if internal oscillator frequency is higher than 1 GHz

Figure 6 shows a setup for radiated emissions test, and Table 4 shows the emissions limits as per CISPR22 for Class B devices.

Common-mode transient immunity

Frequency (MHz)	Limit (dBuV/m)
30 – 230	30
230 – 1000	37

Table 4. CISPR 22 emission limits for Class B devices (10 meters)

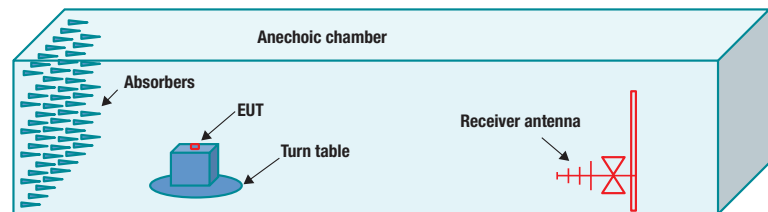


Figure 6. Radiated emissions measurement setup

Common-mode transient immunity (CMTI) is the maximum tolerable rate-of-rise (or fall) of a common-mode voltage. It is given in volts per second. Strictly speaking, CMTI is not an EMC specification. However, it is easy to understand intuitively that a device with a higher CMTI rating performs better in a noisy environment versus

a device with a lower CMTI rating. Hence, it's important to discuss CMTI in this context. VDE-0884-10 explains the method to test the CMTI. Typically the CMTI rating is a good indicator of the device's immunity-related EMC performance.

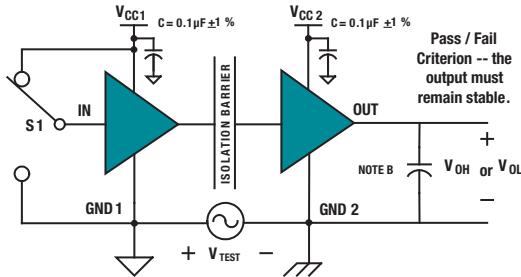


Figure 7. Common-mode transient immunity measurement setup

In digital isolators, CMTI is typically tested by applying a fast rising/falling pulse between the two sides of the isolation barrier. Figure 7 shows a typical test setup. When performing this test, extreme care should be taken to minimize the stray parasitic capacitance between both sides so that the stress is not diverted away from the isolator. Methods like expansive PCB planes or capacitance between the two sides of the isolation barrier should be avoided in this test set-up. Such methods should be restricted only to the final system design and not during the CMTI evaluation. If a vendor evaluation module (EVM) has such additional components, it is good to remove them for the CMTI tests.

Pass-fail criteria

There are four pass-fail criteria for assessing how well a device or equipment performs during and after a transient test.

1. Criterion A: allows no performance degradation during the application of noise transients, thus requiring normal operation during and after the test.
2. Criterion B: accepts some degradation in performance, such as unintentionally logic-state changes, which inevitably lead to a bit-error-rate (BER) increase. However, after the test, the system must be self-recoverable and return to normal operation.

3. Criterion C: accepts the loss of function, such as a latch-up event, but without device damage. After test, a manual re-start or toggling of the power supply is necessary to return the system to normal operation.
4. Criterion D: is the unrecoverable failure or permanent damage to the device and is not an unacceptable result.

In some cases like the ESD test, Criterion A is very difficult to measure on individual component level because in most cases the measurement circuitry itself gets affected during the event. So in those cases, a final system evaluation may be recommended.

Performance summary

To address these common system requirements TI offers the ISO78xx, a reinforced digital isolator family capable of galvanic isolation up to 8000 Vpk. These devices are certified to meet reinforced isolation requirements by VDE and CSA. These isolators provide high electromagnetic immunity and low emissions at low-power consumption, while isolating CMOS or LVCMOS digital I/Os. Table 5 shows the results of key EMC tests for the quad-channel ISO7842 reinforced digital isolator while following the test procedure as described by the relevant standards.

No	Test	Reference standard and specifications	Test results on ISO7842 and conditions
1	Electrostatic discharge immunity test	IEC61000-4-2	Level 4-8 kV contact across the isolation barrier; Criterion B
2	Radiated susceptibility test	IEC61000-4-3	10 Vrms/m 80 MHz to 3 GHz; Criterion A
3	Electrical fast transient immunity test	IEC61000-4-4	4 kV on both IO lines and power lines; Criterion B
4	Conducted immunity test	IEC61000-4-6	10 Vrms from 150 kHz to 80 MHz; Criterion A
5	Radiated emissions test	CISPR 22	30 MHz to 3 GHz with 20 dB Margin; Class B.
6	Common mode transient immunity	VDE-0884-10	100 kV/us typical and 50 kV/us minimum; Criterion A

Conclusions

Understanding the true performance of digital isolators under the harsh conditions of industrial environments is critical in choosing the right fit for any system design.

Expensive and impractical implementations of the evaluation board can sometimes result in good EMC results, but mask the inherent weakness of the digital isolator. For a true measure of the digital isolator, a basic system board design was used and the robust performance of the ISO78xx family of reinforced digital isolators in various IEC-61000-4-X and VDE standards was presented.

References

1. [ISO7842 product folder](#)
2. [ISO7841 product folder](#)
3. [ISO7821 product folder](#)
4. [Reinforced Isolation meets unmatched performance](#)
5. Anant S Kamath and Kannan Soundarapandian, [High-voltage reinforced isolation: Definitions and test methodologies](#), White Paper (slyy063), Texas Instruments, November 2014

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