

ISOUSB111 Full/Low Speed Isolated USB Repeater

1 Features

- Compliant to USB 2.0
- Supports low speed (1.5 Mbps) and full speed (12 Mbps) signaling
- Automatic speed and connection detection
- Supports L1 (sleep) and L2 (suspend) low-power states
- Supports automatic role reversal for USB On-The-Go (OTG) and Type-C® Dual Role Port (DRP) designs
- High CMTI: 100 kV/μs
- V_{BUS} voltage range: 4.25 V to 5.5 V
 - 3.3 V internal LDO
- Meets CISPR32 class B emissions limits
- Ambient temperature range: -40°C to +125°C
- 16-SOIC and 16-SSOP package options
- Safety-related certifications:
 - 7071-V_{PK} V_{IOTM} and 2121-V_{PK} V_{IORM} (Reinforced and Basic Options) per DIN EN IEC 60747-17 (VDE 0884-17)
 - 5000-V_{RMS} isolation for 1 minute per UL 1577
 - IEC 62368-1, IEC 60601-1 and IEC 61010-1 certifications
 - CQC, TUV and CSA certifications
 - 16-SOIC certifications complete; 16-SSOP certifications planned

2 Applications

- USB Hub, Host, Peripheral and Cable Isolation
- [Medical](#)
- [Factory automation](#)
- [Motor drives](#)
- [Grid infrastructure](#)
- [Power delivery](#)

Reinforced and Basic Isolation Options

FEATURE	ISOUSB111	ISOUSB111B
Protection Level	Reinforced	Basic
Surge Isolation Voltage	12800 V _{PK}	6000 V _{PK}
Isolation Rating	5000 V _{RMS}	3000 V _{RMS}
Isolation Working Voltage	1500 V _{RMS} / 2121 V _{PK}	1500 V _{RMS} / 2121 V _{PK}

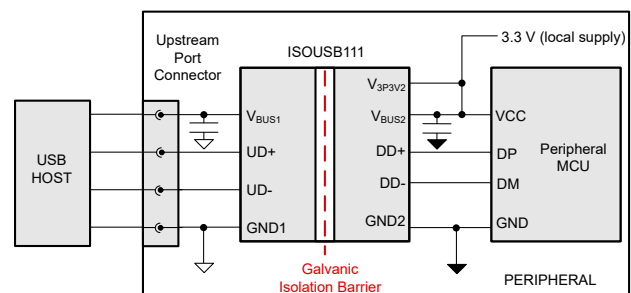
3 Description

ISOUSB111 is a galvanically-isolated USB 2.0 compliant repeater supporting low speed (1.5 Mbps) and full speed (12 Mbps) signaling rates. The device supports automatic connect and speed detection, reflection of pull-ups/pull-downs, and link power management allowing drop-in USB hub, host, peripheral and cable isolation. The device also supports automatic role reversal - if after disconnect, a new connect is detected on the Upstream facing port, then the Upstream and Downstream port definitions are reversed. This feature enables the device to support USB On-The-Go (OTG) and Type-C Dual Role Port (DRP) implementations. This device uses a silicon dioxide (SiO₂) insulation barrier with a withstand voltage of up to 5000 V_{RMS} and a working voltage of 1500 V_{RMS}. Used in conjunction with isolated power supplies, the device protects against high voltage, and prevents noise currents from the bus from entering the local ground. The ISOUSB111 device is available for both basic and reinforced isolation (see [Reinforced and Basic Isolation Options](#)). It supports a wide ambient temperature range of -40°C to +125°C. The device is available in the standard SOIC-16 (16-DW) package and a smaller SSOP-16 (16-DWX) package.

Device Information

PART NUMBER ⁽¹⁾	PACKAGE	BODY SIZE (NOM)
ISOUSB111	SOIC (16) DW	10.30 mm × 7.50 mm
	SSOP (16) DWX	5.85 mm × 7.50 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



Application Diagram



Table of Contents

1 Features	1	8 Detailed Description	16
2 Applications	1	8.1 Overview.....	16
3 Description	1	8.2 Functional Block Diagram.....	16
4 Revision History	2	8.3 Feature Description.....	16
5 Pin Configuration and Functions	3	8.4 Device Functional Modes.....	18
6 Specifications	5	9 Power Supply Recommendations	19
6.1 Absolute Maximum Ratings.....	5	10 Application and Implementation	20
6.2 ESD Ratings.....	5	10.1 Typical Application.....	20
6.3 Recommended Operating Conditions.....	5	11 Layout	24
6.4 Thermal Information.....	6	11.1 Layout Guidelines.....	24
6.5 Power Ratings.....	6	12 Device and Documentation Support	26
6.6 Insulation Specifications.....	7	12.1 Documentation Support.....	26
6.7 Safety-Related Certifications.....	8	12.2 Receiving Notification of Documentation Updates.....	26
6.8 Safety Limiting Values.....	8	12.3 Support Resources.....	26
6.9 Electrical Characteristics.....	9	12.4 Trademarks.....	26
6.10 Switching Characteristics.....	11	12.5 Electrostatic Discharge Caution.....	26
6.11 Insulation Characteristics Curves.....	13	12.6 Glossary.....	26
6.12 Typical Characteristics.....	14	13 Mechanical, Packaging, and Orderable Information	26
7 Parameter Measurement Information	15	13.1 Tape and Reel Information.....	33
7.1 Test Circuits.....	15		

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2022) to Revision B (July 2022)	Page
• Updated device status to Production Data.....	1
Changes from Revision * (November 2021) to Revision A (April 2022)	Page
• T _A Max value updated to 125°C.....	5

5 Pin Configuration and Functions

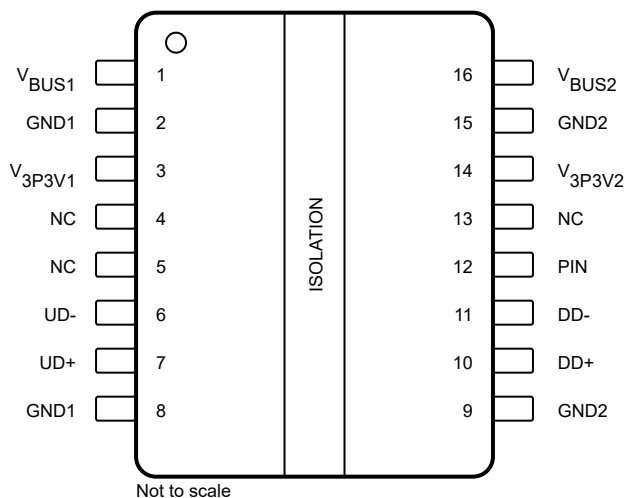


Figure 5-1. DW Package 16-Pin SOIC Top View

Pin Functions—16 DW

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V _{BUS1}	—	Input Power Supply for Side 1. If a 4.25 V to 5.5 V (example USB power bus) supply is available connect it to V _{BUS1} . In this case an internal LDO generates V _{3P3V1} . Else, connect V _{BUS1} and V _{3P3V1} to an external 3.3 V power supply.
2	GND1	—	Ground 1. Ground reference for Isolator Side 1.
3	V _{3P3V1}	—	Power Supply for Side 1. If a 4.25 V to 5.5 V supply is connected to V _{BUS1} connect a bypass capacitor between V _{3P3V1} and GND1. In this case an internal LDO generates V _{3P3V1} . Else, connect V _{BUS1} and V _{3P3V1} to an external 3.3 V power supply.
4	NC	—	Preferably leave floating or connect to V _{3P3V1} . It is also OK to connect to GND1.
5	NC	—	Preferably leave floating or connect to V _{3P3V1} . It is also OK to connect to GND1.
6	UD-	I/O	Upstream facing port D-.
7	UD+	I/O	Upstream facing port D+.
8	GND1	—	Ground 1. Ground reference for Isolator Side 1.
9	GND2	—	Ground 2. Ground reference for Isolator Side 2.
10	DD+	I/O	Downstream facing port D+.
11	DD-	I/O	Downstream facing port D-.
12	PIN	I	Upstream pull-up enable. If this pin is low, pull-up on DD+ and DD- is not recognized.
13	NC	—	Preferably leave floating or connect to V _{3P3V2} . It is also OK to connect to GND2.
14	V _{3P3V2}	—	Power Supply for Side 2. If a 4.25 V to 5.5 V supply is connected to V _{BUS2} connect a bypass capacitor between V _{3P3V2} and GND1. In this case an internal LDO generates V _{3P3V2} . Else, connect V _{BUS2} and V _{3P3V2} to an external 3.3 V power supply.
15	GND2	—	Ground 2. Ground reference for Isolator Side 2.
16	V _{BUS2}	—	Input Power Supply for Side 2. If a 4.25 V to 5.5 V (example USB power bus) supply is available connect it to V _{BUS2} . In this case an internal LDO generates V _{3P3V2} . Else, connect V _{BUS2} and V _{3P3V2} to an external 3.3 V power supply.

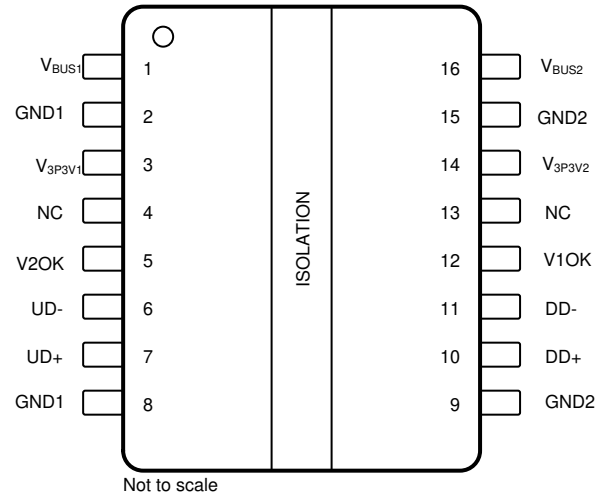


Figure 5-2. DWX Package 16-Pin SSOP Top View

Table 5-1. Pin Functions—16 DWX

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V _{BUS1}	—	Input Power Supply for Side 1. If a 4.25 V to 5.5 V (example USB power bus) supply is available connect it to V _{BUS1} . In this case an internal LDO generates V _{3P3V1} . Else, connect V _{BUS1} and V _{3P3V1} to an external 3.3 V power supply.
2	GND1	—	Ground 1. Ground reference for Isolator Side 1.
3	V _{3P3V1}	—	Power Supply for Side 1. If a 4.25 V to 5.5 V supply is connected to V _{BUS1} connect a bypass capacitor between V _{3P3V1} and GND1. In this case an internal LDO generates V _{3P3V1} . Else, connect V _{BUS1} and V _{3P3V1} to an external 3.3 V power supply.
4	NC	—	Leave floating or connect to V _{3P3V1} .
5	V2OK	O	High level on this pin indicates that side 2 is powered up.
6	UD-	I/O	Upstream facing port D-.
7	UD+	I/O	Upstream facing port D+.
8	GND1	—	Ground 1. Ground reference for Isolator Side 1.
9	GND2	—	Ground 2. Ground reference for Isolator Side 2.
10	DD+	I/O	Downstream facing port D+.
11	DD-	I/O	Downstream facing port D-.
12	V1OK	—	High level on this pin indicates that side 1 is powered up.
13	NC	—	Leave floating or connect to V _{3P3V2} .
14	V _{3P3V2}	—	Power Supply for Side 2. If a 4.25 V to 5.5 V supply is connected to V _{BUS2} connect a bypass capacitor between V _{3P3V2} and GND1. In this case an internal LDO generates V _{3P3V2} . Else, connect V _{BUS2} and V _{3P3V2} to an external 3.3 V power supply.
15	GND2	—	Ground 2. Ground reference for Isolator Side 2.
16	V _{BUS2}	—	Input Power Supply for Side 2. If a 4.25 V to 5.5 V (example USB power bus) supply is available connect it to V _{BUS2} . In this case an internal LDO generates V _{3P3V2} . Else, connect V _{BUS2} and V _{3P3V2} to an external 3.3 V power supply.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

		MIN	MAX	UNIT
V _{BUS1} , V _{BUS2}	V _{BUS} supply voltage	-0.3	6	V
V _{3P3V1} , V _{3P3V2}	3.3-V input supply voltage	-0.3	4.25	V
V _{DPDM}	Voltage on bus pins (UD+, UD-, DD+, DD-) 1000 total number of short events and cumulative duration of 1000 hrs.	-0.3	6	V
V _{IO}	IO voltage range (PIN, V*OK)	-0.3	V _{3P3Vx} +0.3 ⁽³⁾	V
I _O	Output current on output pins (V*OK)	-10	10	mA
T _J	Junction temperature		150	°C
T _{STG}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
- (3) Maximum voltage must not exceed 4.25 V

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾	±2000	V
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{BUSx}	V _{BUS} input voltage (inclusive of any ripple)	4.25	5	5.5	V
V _{3P3Vx}	3.3-V input supply voltage (inclusive of any ripple)	3.0	3.3	3.6	V
T _A	Operating free-air temperature	-40		125	°C
T _J	Junction temperature	-55		150	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		ISUSB111		UNIT
		DW (SOIC)	DWX (SSOP)	
		16 PINS	16 PINS	
R _{ΘJA}	Junction-to-ambient thermal resistance	53.4	60.6	°C/W
R _{ΘJC(top)}	Junction-to-case (top) thermal resistance	19.6	22.5	°C/W
R _{ΘJB}	Junction-to-board thermal resistance	22.3	27	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	2.4	2	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	21.6	26.1	°C/W
R _{ΘJC(bot)}	Junction-to-case (bottom) thermal resistance	-	-	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISUSB111						
P _D	Maximum power dissipation (both sides)	V _{BUS1} = V _{BUS2} = 5.5 V, T _J = 150°C, C _L = 50 pF each on DD- and DD+, Input a 6-MHz 50% duty cycle differential 3.3-V square wave on UD- and UD+			157	mW
P _{D1}	Maximum power dissipation (side-1)				72	mW
P _{D2}	Maximum power dissipation (side-2)				85	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFICATIONS		UNIT
			DW-16	DWX-16	
IEC 60664-1					
CLR	External clearance ⁽¹⁾	Side 1 to side 2 distance through air	>8	>8	mm
CPG	External Creepage ⁽¹⁾	Side 1 to side 2 distance across package surface	>8	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>21	>21	μm
CTI	Comparative tracking index	IEC 60112; UL 746A	>600	>600	V
	Material Group	According to IEC 60664-1	I	I	
	Overvoltage category	Rated mains voltage ≤ 600 V _{RMS}	I-IV	I-IV	
		Rated mains voltage ≤ 1000 V _{RMS}	I-III	I-III	
DIN EN IEC 60747-17 (VDE 0884-17) ⁽²⁾					
V _{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	2121	V _{PK}
V _{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDb) test;	1500	1500	V _{RMS}
		DC voltage	2121	2121	V _{DC}
V _{IOTM}	Maximum transient isolation voltage, ISOUSB111	V _{TEST} = V _{IOTM} , t = 60 s (qualification); V _{TEST} = 1.2 × V _{IOTM} , t = 1 s (100% production)	7071	7071	V _{PK}
	Maximum transient isolation voltage, ISOUSB111B		4242	4242	V _{PK}
V _{IMP}	Maximum impulse voltage, ISOUSB111 ⁽³⁾	Tested in air, 1.2/50-us waveform per IEC 62368-1	9800	9800	V _{PK}
	Maximum impulse voltage, ISOUSB111B ⁽³⁾		4615	4615	V _{PK}
V _{IOSM}	Maximum surge isolation voltage, ISOUSB111 ⁽⁴⁾	Tested in oil (qualification test), 1.2/50-μs waveform per IEC 62368-1	12800	12800	V _{PK}
	Maximum surge isolation voltage, ISOUSB111B ⁽⁴⁾		6000	6000	V _{PK}
q _{pd}	Apparent charge ⁽⁵⁾	Method a: After I/O safety test subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10 s	≤ 5	≤ 5	pC
		Method a: After environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s; ISOUSB111: V _{pd(m)} = 1.6 × V _{IORM} , t _m = 10 s ISOUSB111B: V _{pd(m)} = 1.3 × V _{IORM} , t _m = 10 s	≤ 5	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test), V _{ini} = V _{IOTM} , t _{ini} = 1 s; ISOUSB111: V _{pd(m)} = 1.875 × V _{IORM} , t _m = 1 s ISOUSB111B: V _{pd(m)} = 1.5 × V _{IORM} , t _m = 1 s	≤ 5	≤ 5	
C _{IO}	Barrier capacitance, input to output ⁽⁶⁾	V _{IO} = 0.4 × sin (2 pft), f = 1 MHz	0.8	0.7	pF
R _{IO}	Insulation resistance, input to output ⁽⁶⁾	V _{IO} = 500 V, T _A = 25°C	> 10 ¹²	> 10 ¹²	W
		V _{IO} = 500 V, 100°C ≤ T _A ≤ 125°C	> 10 ¹¹	> 10 ¹¹	
		V _{IO} = 500 V at T _S = 150°C	> 10 ⁹	> 10 ⁹	
	Pollution degree		2	2	
	Climatic category		40/125/21	40/125/21	
UL 1577					
V _{ISO}	Withstand isolation voltage, ISOUSB111	V _{TEST} = V _{ISO} , t = 60 s (qualification); V _{TEST} = 1.2 × V _{ISO} , t = 1 s (100% production)	5000	5000	V _{RMS}
	Withstand isolation voltage, ISOUSB111B		3000	3000	V _{RMS}

- (1) Care must be taken during board design so that the mounting pads of the isolator on the printed-circuit board (PCB) do not reduce creepage and clearance. Inserting grooves, ribs or both can help increase creepage distance on the PCB.
- (2) ISOUSB111 is suitable for safe electrical insulation and ISOUSB111B is suitable for basic electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air to determine the surge immunity of the package.
- (4) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.
- (5) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (6) All pins on each side of the barrier tied together creating a two-pin device.

6.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 61010-1, IEC 62368-1 and IEC 60601-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB4943.1-2011	Certified according to EN 61010-1:2010/A1:2019 and EN 62368-1:2014
Maximum transient isolation voltage, ISOUSB111: 7071 V _{PK} ISOUSB111B: 4242 V _{PK} Maximum repetitive peak isolation voltage, 2121 V _{PK} ; Maximum surge isolation voltage, ISOUSB111: 12800 V _{PK} (Reinforced) ISOUSB111B: 6000 V _{PK} (Basic)	IEC 62368-1 2nd Ed., for pollution degree 2, material group I ISOUSB111: 800 V _{RMS} reinforced isolation ISOUSB111B: 1000 V _{RMS} basic isolation ----- CSA 60601- 1:14 and IEC 60601-1 Ed. 3+A1 ISOUSB111: 2 MOPP (Means of Patient Protection) 250 V _{RMS} (354 V _{PK}) maximum working voltage	Single protection, ISOUSB111: 5000 V _{RMS} ISOUSB111B: 3000 V _{RMS}	Reinforced insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V _{RMS} maximum working voltage	EN 61010-1:2010/A1:2019 ISOUSB111: 600 V _{RMS} reinforced isolation ISOUSB111B: 1000 V _{RMS} basic isolation ----- EN 62368-1:2014 ISOUSB111: 800 V _{RMS} reinforced isolation ISOUSB111B: 1000 V _{RMS} basic isolation
Reinforced certificate: 40040142 Basic certificate: 40047657	Master contract: 220991	File number: E181974	Certificate: CQC15001121716	Client ID: 77311

6.8 Safety Limiting Values

Safety limiting⁽¹⁾ intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 PACKAGE						
I _S	Safety input, output, or supply current	R _{θJA} = 53.4°C/W, V _I = 5.5 V, T _J = 150°C, T _A = 25°C, see Figure 6-1			425	mA
		R _{θJA} = 53.4°C/W, V _I = 3.6 V, T _J = 150°C, T _A = 25°C, see Figure 6-1			650	mA
P _S	Safety input, output, or total power	R _{θJA} = 53.4°C/W, T _J = 150°C, T _A = 25°C, see Figure 6-3			2340	mW
T _S	Maximum safety temperature				150	°C
DWX-16 PACKAGE						
I _S	Safety input, output, or supply current	R _{θJA} = 60.6°C/W, V _I = 5.5 V, T _J = 150°C, T _A = 25°C, see Figure 6-2			374	mA
		R _{θJA} = 60.6°C/W, V _I = 3.6 V, T _J = 150°C, T _A = 25°C, see Figure 6-2			572	mA
P _S	Safety input, output, or total power	R _{θJA} = 60.6°C/W, T _J = 150°C, T _A = 25°C, see Figure 6-4			2062	mW
T _S	Maximum safety temperature				150	°C

- (1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, R_{θJA}, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
T_J = T_A + R_{θJA} × P, where P is the power dissipated in the device.
T_{J(max)} = T_S = T_A + R_{θJA} × P_S, where T_{J(max)} is the maximum allowed junction temperature.
P_S = I_S × V_I, where V_I is the maximum input voltage.

6.9 Electrical Characteristics

Over recommended operating conditions (unless otherwise noted). All typical values are at $T_A = 25^\circ\text{C}$, $V_{\text{BUSx}} = 5\text{ V}$, $V_{3\text{P3Vx}} = 3.3\text{ V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CHARACTERISTICS						
I_{VBUSx} or I_{V3P3Vx}	V_{BUS} or $V_{3\text{P3V}}$ current consumption - Full Speed (FS) and Low Speed (LS) modes	Receive side FS Active (6 MHz signal rate), Figure 7-9, $C_L = 50\text{ pF}$		12	15.3	mA
		Transmit side FS Active (6 MHz signal rate), Figure 7-9, $C_L = 50\text{ pF}$		9.5	13	mA
		Receive side LS Active (750 kHz signal rate), Figure 7-10, $C_L = 450\text{ pF}$		11	13.5	mA
		Transmit side LS Active (750 kHz signal rate), Figure 7-10, $C_L = 450\text{ pF}$		9.5	13	mA
		FS/LS Idle State (US side or DS side)		7.4	11	mA
I_{VBUSx} or I_{V3P3Vx}	V_{BUS} or $V_{3\text{P3V}}$ current consumption - L1 Sleep mode	Upstream Facing side		7.5	9.8	mA
		Downstream Facing side		7.3	9.5	mA
I_{VBUSx} or I_{V3P3Vx}	V_{BUS} or $V_{3\text{P3V}}$ current consumption - L2 Suspend mode	Upstream Facing side		1.07	1.55	mA
		Downstream Facing side		5.6	7.5	mA
I_{VBUSx} or I_{V3P3Vx}	V_{BUS} or $V_{3\text{P3V}}$ current consumption - Not attached	Upstream Facing side		6.2	8.5	mA
		Downstream Facing side		6.2	8.9	mA
$\text{UV}^+_{(\text{VBUSx})}$ (1)	Under voltage threshold when supply voltage is rising, V_{BUS}				4.0	V
$\text{UV}^-_{(\text{VBUSx})}$ (1)	Under voltage threshold when supply voltage is falling, V_{BUS}		3.6			V
$\text{UVHYS}_{(\text{VBUSx})}$ (1)	Under voltage threshold hysteresis, V_{BUS}			0.08		V
$\text{UV}^+_{(\text{V3P3Vx})}$	Under voltage threshold when supply voltage is rising, $V_{3\text{P3V}}$				2.95	V
$\text{UV}^-_{(\text{V3P3Vx})}$	Under voltage threshold when supply voltage is falling, $V_{3\text{P3V}}$		1.95			V
$\text{UVHYS}_{(\text{V3P3Vx})}$	Under voltage threshold hysteresis, $V_{3\text{P3V}}$			0.11		V
DIGITAL INPUTS						
V_{IH}	High-level input voltage		$0.7 \times V_{3\text{P3Vx}}$			V
V_{IL}	Low-level input voltage			$0.3 \times V_{3\text{P3Vx}}$		V
V_{IHYS}	Input transition threshold hysteresis		0.3			V
I_{IH}	High-level input current				1	μA
I_{IL}	Low-level input current				10	μA
DIGITAL OUTPUTS (V10K, V20K)						
V_{OH}	High-level output voltage	$I_O = -3\text{ mA}$ for $3.0\text{ V} \leq V_{3\text{P3Vx}} \leq 3.6\text{ V}$	$V_{3\text{P3Vx}} - 0.2$			V
V_{OL}	Low-level output voltage	$I_O = 3\text{ mA}$ for $3.0\text{ V} \leq V_{3\text{P3Vx}} \leq 3.6\text{ V}$		0.2		V
UDx, DDx, INPUT CAPACITANCE AND TERMINATION						
$Z_{\text{INP_xDx}}$	Impedance to GND, no pull up/down	$V_{\text{in}} = 3.6\text{ V}$, $V_{3\text{P3Vx}} = 3.0\text{ V}$, $T_J < 125^\circ\text{C}$, USB 2.0 Spec Section 7.1.6	300			k Ω
$C_{\text{IO_xDx}}$	Capacitance to GND	Measured with VNA at 240MHz, Driver Hi-Z		10		pF
R_{PUI}	Bus Pull up Resistor on Upstream Facing Port (idle)	USB 2.0 Spec Section 7.1.5	0.9	1.1	1.575	k Ω
R_{PUR}	Bus Pull up Resistor on Upstream Facing Port (receiving)	USB 2.0 Spec Section 7.1.5	1.5	2.2	3	k Ω

Over recommended operating conditions (unless otherwise noted). All typical values are at $T_A = 25^\circ\text{C}$, $V_{\text{BUSx}} = 5\text{ V}$, $V_{3\text{P3Vx}} = 3.3\text{ V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PD}	Bus Pull-down Resistor on Downstream Facing Port	USB 2.0 Spec Section 7.1.5	14.25	19	24.8	k Ω
V_{TERM}	Termination voltage for Upstream facing port pullup (RPU)	USB 2.0 Spec Section 7.1.5, measured on D+ or D- with pull up enabled on upstream port with external load disconnected.	3		3.6	V
UDx, DDx, INPUT LEVELS LS/FS						
V_{IH}	High (driven)	USB 2.0 Spec Section 7.1.4 (measured at connector)	2			V
V_{IHZ}	High (floating)	USB 2.0 Spec Section 7.1.4 (Host downstream port pull down resistor enabled and Device pulled up to 3.0 V - 3.6 V).	2.7		3.6	V
V_{IL}	Low	USB 2.0 Spec Section 7.1.4			0.8	V
V_{DI}	Differential Input Sensitivity	$ (\text{xD}+) - (\text{xD}-) $; USB 2.0 Spec Figure 7-19; (measured at connector)	0.2			V
V_{CM}	Common Mode Range	Includes VDI range; USB 2.0 Spec Figure 7-19; (measured at connector)	0.8		2.5	V
UDx, DDx, OUTPUT LEVELS LS/FS						
V_{OL}	Low	USB 2.0 Spec Section 7.1.1, (measured at connector with RL of 0.9 k Ω to 3.6 V.)	0		0.3	V
V_{OH}	High (Driven)	USB 2.0 Spec Section 7.1.1 (measured at connector with RL of 14.25 k Ω to GND.)	2.8		3.6	V
V_{OSE1}	SE1	USB 2.0 Spec Section 7.1.1	0.8			V
Z_{FSTERM}	Driver Series Output Resistance	USB 2.0 Spec Section 7.1.1 and Figure 7-4, Measured during VOL or VOH	28		44	Ω
V_{CRS}	Output Signal Crossover Voltage	Measured as in USB 2.0 Spec Section 7.1.1 Figures 7-8, 7-9 and 7-10; Excluding the first transition from the Idle state	1.3		2	V
THERMAL SHUTDOWN						
TSD+	Thermal shutdown turn-on temperature		160	170	180	$^\circ\text{C}$
TSD-	Thermal shutdown turn-off temperature		150	160	170	$^\circ\text{C}$
TSD _{HYS}	Thermal shutdown hysteresis			10		$^\circ\text{C}$

- (1) If V_{BUSx} pins are externally connected to the corresponding $V_{3\text{P3Vx}}$ pins, then UVLO thresholds on V_{BUSx} are governed by $\text{UV}^+_{(\text{V3P3Vx})}$, $\text{UV}^-_{(\text{V3P3Vx})}$ and $\text{UVHYS}_{(\text{V3P3Vx})}$

6.10 Switching Characteristics

Over recommended operating conditions (unless otherwise noted). All typical values are at $T_A = 25^\circ\text{C}$, $V_{\text{BUSX}} = 5\text{ V}$, $V_{\text{3P3VX}} = 3.3\text{ V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER-UP TIMING						
T_{SUPRAMP}	Allowed power supply ramp-up times on V_{BUSX} and V_{3P3VX} external power supplies		0.005		100	ms
T_{PWRUP}	Time taken for the device to power up, and recognize USB signaling, after valid power supply is provided on both side 1 and side 2.	All external power supplies are ramped up together with 5 μs power up time.		3.6	8	ms
UDx, DDx, FS Driver Switching Characteristics						
T_{FR}	Rise Time (10% - 90%)	USB 2.0 Spec Figure 7-8, Figure 7-9, $C_L = 50\text{ pF}$	4		20	ns
T_{FF}	Fall Time (10% - 90%)	USB 2.0 Spec Figure 7-8, Figure 7-9, $C_L = 50\text{ pF}$	4		20	ns
T_{FRFM}	Differential Rise and Fall Time Matching ($T_{\text{FR}}/T_{\text{FM}}$)	USB 2.0 Spec 7.1.2, Excluding the first transition from the Idle state, Figure 7-9, $C_L = 50\text{ pF}$	90		111.1	%
UDx, DDx, LS Driver Switching Characteristics						
T_{LR}	Rise Time (10% - 90%)	USB 2.0 Spec Figures 7-8 and 7-10, with C_L range 50 pF to 600 pF.	75		300	ns
T_{LF}	Fall Time (10% - 90%)	USB 2.0 Spec Figures 7-8 and 7-10, with C_L range 50 pF to 600 pF.	75		300	ns
T_{LRFM}	Rise and Fall Time Matching (TLR/TFM), Excluding first transition from idle state.	USB 2.0 Spec Figures 7-8 and 7-10, with C_L range 50 pF to 600 pF.	80		125	%
REPEATER TIMING - CONNECT, DISCONNECT, RESET, L1, L2						
T_{FILTCNN}	Debounce filter on FS or LS Connect Detection		45	70	80	μs
T_{DDIS}	Time to detect disconnect at the DS facing port in LS/FS L0 mode.		2		7	μs
T_{DETRST}	Time taken to detect reset on US port in LS/FS L0 mode		0		7	μs
T_{2SUSP}	Time taken by the US side to detect suspend mode (L2) and draw less than 2.5 mA current when bus is continuously in idle state.		3		10	ms
$t_{\text{DRESUMEL1}}$	Maximum time to detect resume on the US and reflect/drive resume on the DS port from sleep/L1 state.				1	μs
$t_{\text{DRESUMEL2}}$	Maximum time to detect resume on the US and reflect/drive resume on the DS port from suspend/L2 state.				130	μs
t_{DWAKEL1}	Maximum time to detect and propagate remote wake when in sleep/L1 state.				5	μs
t_{DWAKEL2}	Maximum pulse width of remote wake that is guaranteed to be detected when in suspend/L2 state.				900	μs
t_{DRSMPROP}	Minimum duration of resume driven upstream and downstream after detecting remote wake when in suspend/L2 state.		1			ms
CMTI	Common mode transient immunity	PK-PK common mode noise, $V_{\text{CMPKPK}} = 1200\text{ V}$ during USB data transmission, see Figure 7-2	75	100		kV/ μs

Over recommended operating conditions (unless otherwise noted). All typical values are at $T_A = 25^\circ\text{C}$, $V_{\text{BUSX}} = 5\text{ V}$, $V_{3\text{P3VX}} = 3.3\text{ V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REPEATER TIMING - LS, FS						
T_{LSDD}	Low-speed Differential Data Propagation Delay	USB 2.0 spec section 7.1.14. Figure 7-52(C).			358	ns
T_{LSOP}	LS Data bit-width distortion after SOP	USB 2.0 spec section 7.1.14. Figure 7-52(C).	-40		25	ns
T_{LSJP}	LS repeater additive jitter - paired transition	USB 2.0 spec section 7.1.14. Figure 7-52(C).	-5		5	ns
T_{LSJN}	LS repeater additive jitter - next transition	USB 2.0 spec section 7.1.14. Figure 7-52(C).	-7.0		7.0	ns
T_{LST}	Minimum width of SE0 interval during LS differential transition - filtered out by the repeater	USB 2.0 spec section 7.1.4.		210		ns
T_{LEOPD}	Repeater EOP delay relative to T_{LSDD}	USB 2.0 spec section 7.1.14. Figure 7-53(C).	0		200	ns
T_{LESK}	SE0 skew caused by the repeater during LS EOP	USB 2.0 spec section 7.1.14. Figure 7-53(C).	-100		100	ns
T_{FSDD}	Full-Speed Differential Data Propagation Delay	USB 2.0 spec section 7.1.14. Figure 7-52(C).			70	ns
T_{FSOP}	FS Data bit-width distortion after SOP	USB 2.0 spec section 7.1.14. Figure 7-52(C).	-10		10	ns
T_{FSJP}	FS repeater additive jitter - paired transition	USB 2.0 spec section 7.1.14. Figure 7-52(C).	-2		2	ns
T_{FSJN}	FS repeater additive jitter - next transition	USB 2.0 spec section 7.1.14. Figure 7-52(C).	-6.0		6.0	ns
T_{FST}	Minimum width of SE0 interval during FS differential transition - filtered out by the repeater	USB 2.0 spec section 7.1.4.		14		ns
T_{FEOPD}	Repeater EOP delay relative to T_{FSDD}	USB 2.0 spec section 7.1.14. Figure 7-53(C).	0		17	ns
T_{FESK}	SE0 skew caused by the repeater during FS EOP	USB 2.0 spec section 7.1.14. Figure 7-53(C).	-15		15	ns

6.11 Insulation Characteristics Curves

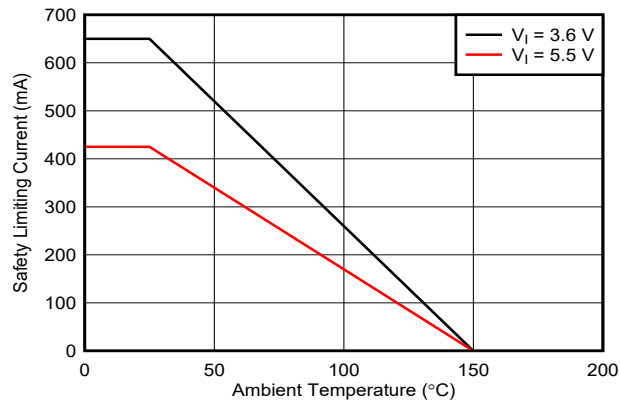


Figure 6-1. Thermal Derating Curve for Limiting Current per VDE for DW-16 Package

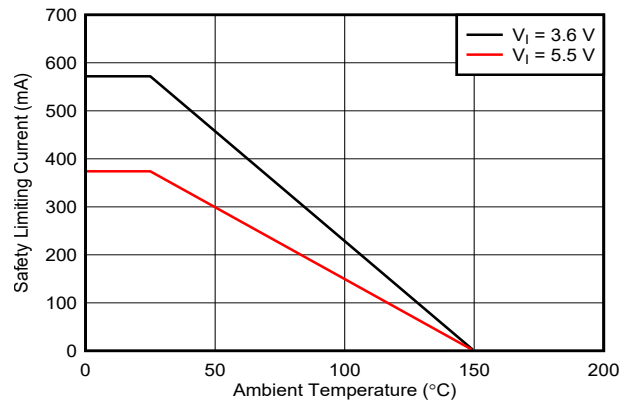


Figure 6-2. Thermal Derating Curve for Limiting Current per VDE for DWX-16 Package

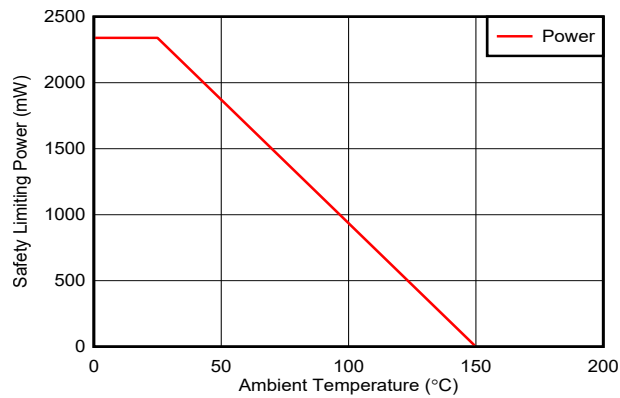


Figure 6-3. Thermal Derating Curve for Limiting Power per VDE for DW-16 Package

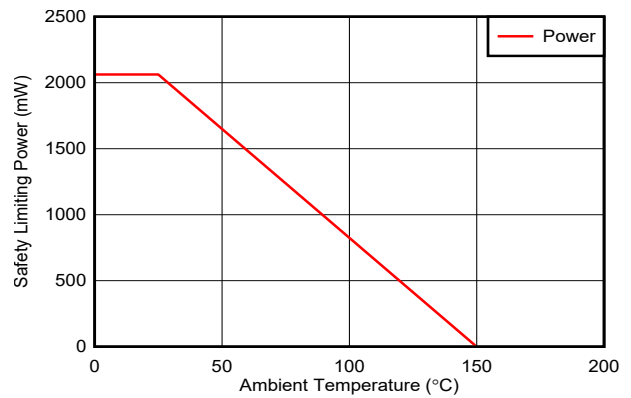


Figure 6-4. Thermal Derating Curve for Limiting Power per VDE for DWX-16 Package

6.12 Typical Characteristics

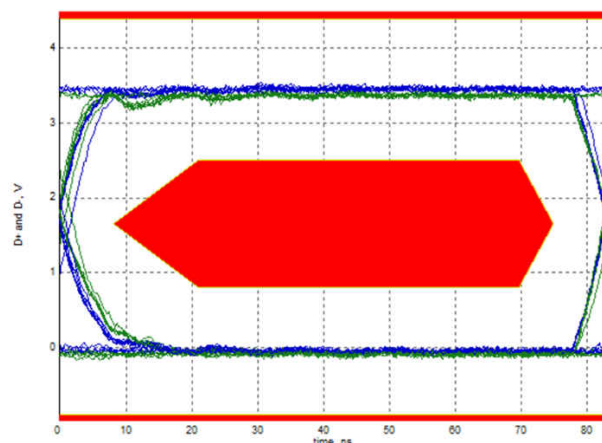


Figure 6-5. Typical Full-Speed (12 Mbps) Eye-Diagram through ISOUSB111

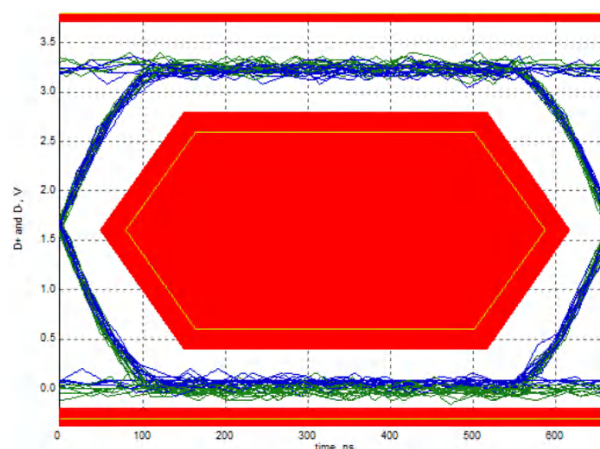


Figure 6-6. Typical Low-Speed (1.5 Mbps) Eye-Diagram through ISOUSB111

7 Parameter Measurement Information

7.1 Test Circuits

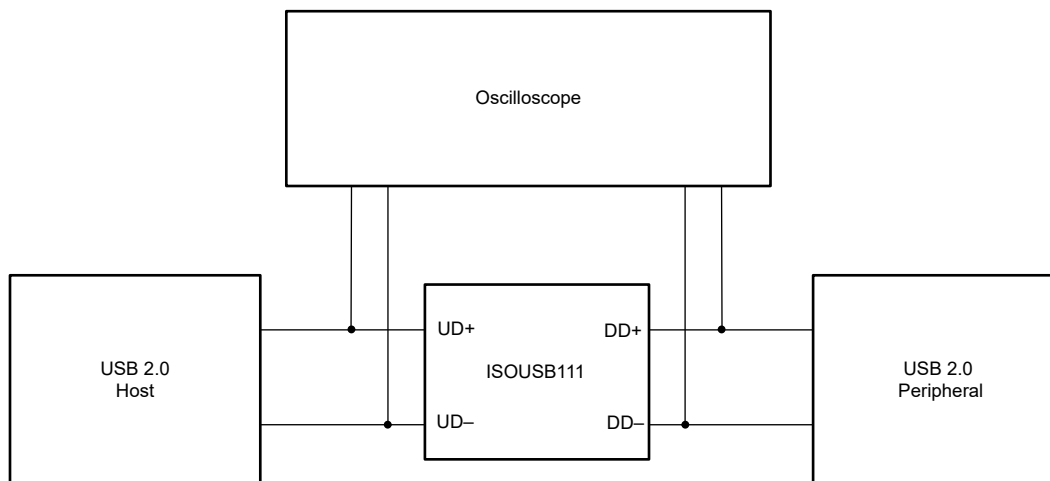


Figure 7-1. Upstream and Downstream Packet Parameter and Eye-Diagram Measurements

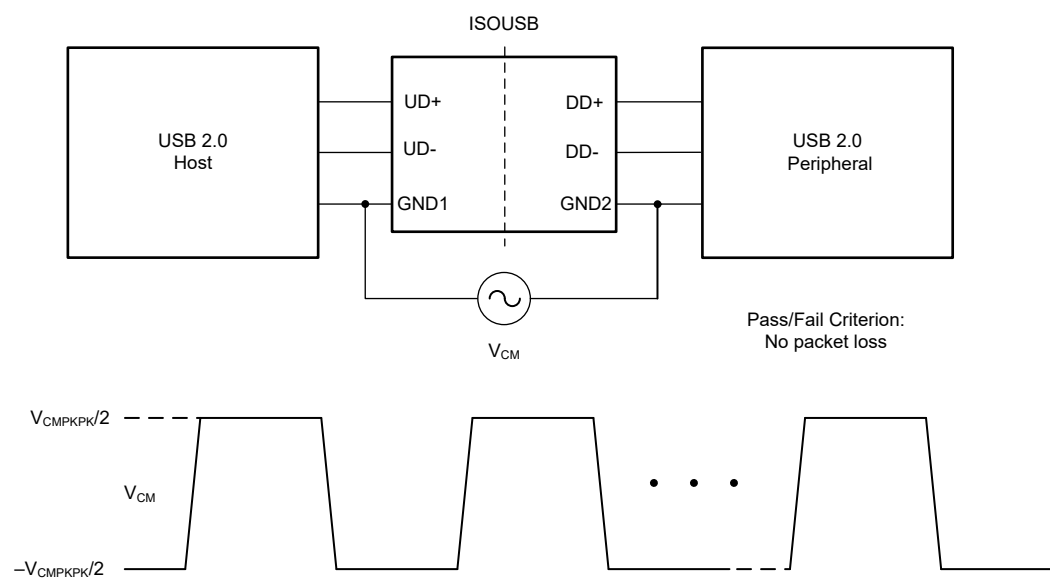


Figure 7-2. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

ISOUSB111 is a galvanically-isolated USB2.0 compliant repeater supporting Low Speed (1.5 Mbps) and Full Speed (12 Mbps) signaling rates. The device supports automatic speed and connection detection, reflection of pull-ups/pull-downs, and link power management allowing drop-in USB hub, host, peripheral and cable isolation. Most microcontrollers integrate the USB PHY, and so offer only D+ and D- bus lines as external pins. ISOUSB111 can isolate these pins from the USB bus without needing any other intervention from the microcontroller. The device also supports automatic role reversal - if after disconnect, if a new connect is detected on the Upstream facing port, then the Upstream and Downstream port definitions are reversed.

ISOUSB111 is available in basic and reinforced isolation options with isolation withstand voltage of 3000 V_{RMS} and 5000 V_{RMS} respectively, and with surge test voltage of 6 kV_{PK} and 12.8 kV_{PK} respectively. The device can operate completely off a 4.25 V to 5.5 V supply (USB VBUS power) or from local 3.3-V supply, if available, on both side 1 and side 2. This flexibility in supply voltages allows optimization for thermal performance based on power rails available in the system.

8.2 Functional Block Diagram

A simplified functional block diagram of ISOUSB111 is shown in [Figure 8-1](#). The device comprises the following:

1. Transmit and receive circuits and pull-up and pull-down resistors according to the USB standard.
2. Digital logic to handle bi-directional communication, and various state-transitions.
3. Internal LDOs to generate V_{3P3Vx} supplies from the V_{BUSx} supplies.
4. Galvanic isolation.

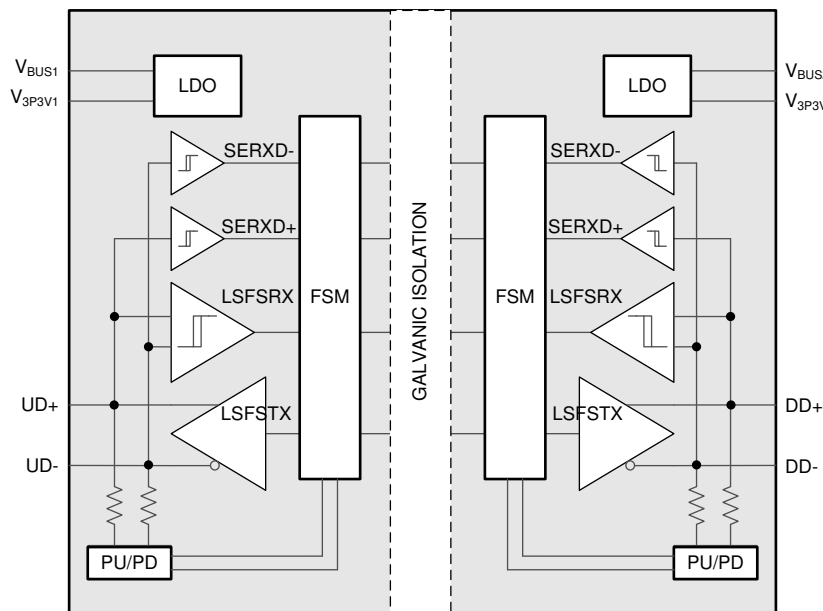


Figure 8-1. ISOUSB111 Simplified Functional Block Diagram

8.3 Feature Description

8.3.1 Power Supply Options

The ISOUSB111 can be powered by connecting a 4.25 V to 5.5 V supply on V_{BUSx} pins, in which case an internal LDO generates V_{3P3Vx} voltage. This option is suitable for the side facing the USB connector, where a 5-V VBUS supply is available. Alternatively, V_{BUSx} and V_{3P3Vx} pins can be shorted together and an external 3.3-V power supply can be connected to both. This second option is suitable for the side facing the microcontroller, where a 5-V supply may not be available.

8.3.2 Power Up

Until all power supplies on both sides of ISOUSB111 are above their respective UVLO thresholds, the device ignores any activity on the bus lines on both upstream and downstream side. Once the power supplies are above their UVLO thresholds, the device is ready to respond to activity on the bus lines.

8.3.3 Symmetric Operation, Dual-Role Port and Role-Reversal

ISOUSB111 supports symmetric operation. Normally, UD+ and UD- are upstream facing ports and connect to a host or hub. DD+ and DD- are downstream facing ports and connect to a peripheral. However, it is also possible to connect UD+ and UD- to a peripheral and DD+ and DD- to a host or hub. Whichever side sees a connect first (D+ or D- pulled up to 3.3V) becomes the downstream facing side. This feature enables implementation of dual-role port (for eg. Type-C dual-role port) and role-reversal (for eg. OTG Host Negotiation Protocol - HNP). Refer to [How to Implement an Isolated USB 2.0 High-Speed, Type-C® DRP](#) application note for details. In the rest of this document, DD+/DD- are treated as downstream facing ports, and UD+/UD- as upstream facing ports, but the various operations and features described are equally applicable if this assignment is swapped.

8.3.4 Connect and Speed Detection

When there is no peripheral device connected to the downstream side of ISOUSB111, internal 15 kΩ pull-down resistors on DD+ and DD- pins pull the bus lines to zero, creating an SE0 state. When either the DD+ or DD- lines is pulled up higher than the V_{IH} threshold, for a time period higher than $T_{FILTCNN}$, the ISOUSB111 device treats this as a connect. The ISOUSB111 device configures internal pull-up on the upstream side to match the pull-up detected on the downstream side. After connect is detected, the ISOUSB111 device waits for a reset to be asserted by the host/hub on the upstream side. Depending on whether DD+ or DD- is pulled up at the start of reset, the speed of the ISOUSB111 repeater is set. Once set, the speed of the repeater can only be changed after a power down or disconnect event.

8.3.5 Disconnect Detection

When in Full-speed (FS) and Low-speed (LS) modes, disconnection of a peripheral is indicated when the host/hub is not driving any signal on the upstream side, and when the downstream bus is in the SE0 state (Both DD+ and DD- are below the V_{IL} threshold) for a time period higher than T_{DDIS} . Upon disconnect detection in FS and LS modes, the ISOUSB111 device removes the pull-up resistor from the upstream side, thus allowing the upstream UD+ and UD- lines to discharge to zero. The ISOUSB111 then waits for the next connect event to occur.

8.3.6 Reset

The ISOUSB111 device detects Reset assertion (prolonged SE0 state) on its upstream facing side, and transmits the same to the downstream facing side.

8.3.7 LS/FS Message Traffic

The ISOUSB111 device monitors the state of the bus on both upstream and downstream sides. The direction of communication is set by which side transitions from the LS/FS idle state first (J to K transition). After that, data is transferred digitally across the barrier, and reconstructed on the other side. Data transmission continues till either an End-of-Packet (EOP) or a long idle is seen. At this point, the ISOUSB111 device tri-states its LS/FS transmitters, and waits for the next transition from the LS/FS idle state.

8.3.8 L2 Power Management State (Suspend) and Resume

The ISOUSB111 device supports Suspend low power state, also called L2 state in the USB 2.0 Link Power Management engineering change notice (ECN). Suspend mode is detected if the bus stays in the LS/FS idle state for more than 3 ms. When Suspend is detected from LS and FS idle state, the ISOUSB111 continues in the LS or FS idle state, at the same time reducing internal power consumption. The transition to the L2 low-power mode is completed within 10 ms.

Exit from L2 occurs through either Resume signaling from the host, on the upstream facing side of ISOUSB111, or Remote Wake signaling from the peripheral on the downstream facing side of ISOUSB111 followed by Resume signaling from the host/hub on the upstream facing side. Start of Resume or Wake are signaled by

a 'K' state by the host or the device respectively. The end of resume is signalled by the host by driving two low-speed bit times of SE0 followed by a 'J' state. ISOUSB111 is able to replicate the resume and wake signaling appropriately both upstream and downstream. After Resume/Wake signaling the device returns to LS or FS idle state depending on the state it was in before entering the L2 state.

8.3.9 L1 Power Management State (Sleep) and Resume

The ISOUSB111 device supports the additional L1 or Sleep low power state defined in the USB 2.0 Link Power Management ECN. When L1 entry is detected from the LS and FS idle state, the ISOUSB111 continues in the LS or FS idle state, at the same time reducing internal power consumption. The transition to the L1 low-power mode is completed within 50 μ s.

Exit from L1 occurs through either Resume signaling from the host, on the upstream facing side of ISOUSB111, or Remote Wake signaling from the peripheral on the downstream facing side of ISOUSB111 followed by Resume signaling from the host/hub on the upstream facing side. Start of Resume or Wake are signaled by a 'K' state by the host or the device respectively. The end of resume is signalled by the host by driving two low-speed bit times of SE0 followed by a 'J' state. ISOUSB111 is able to replicate the K signaling appropriately both upstream and downstream. After Resume/Wake signaling the device returns to LS or FS idle state depending on the state it was in before entering the L1 state.

8.4 Device Functional Modes

Table 8-1 lists the functional modes for the ISOUSB111 device.

Table 8-1. Function Table

SIDE 1 SUPPLY V_{BUS1} , V_{3P3V1} (1)	BUS1 (UD+, UD-)	SIDE 2 SUPPLY V_{PIN}	SIDE 2 SUPPLY V_{BUS2} , V_{3P3V2}	BUS2 (DD+, DD-)	COMMENTS
Powered	Active	H	Powered	Active	When both sides are powered, the state-of the bus is reflected correctly from upstream to downstream and vice-versa.
Powered	15-k Ω PD	L	Powered	15-k Ω PD	Disconnected state is presented on both upstream and downstream
Powered	15-k Ω PD	X	Unpowered	Z	If a side is not powered, the bus lines on that side are in high-impedance state.
Unpowered	Z	X	Powered	15-k Ω PD	
Unpowered	Z	X	Unpowered	Undetermined	

(1) Powered = ($V_{BUSx} \geq UV_{+(V_{BUSx})}$) || ($V_{BUSx} = V_{3P3Vx} \geq UV_{+(V_{3P3Vx})}$) ; Unpowered = ($V_{BUSx} < UV_{-(V_{BUSx})}$) & ($V_{3P3Vx} < UV_{-(V_{3P3Vx})}$) ; X = Irrelevant; H = High level; L = Low level; Z = High impedance

9 Power Supply Recommendations

0.1 μF capacitors are recommended to be placed very close to V_{3P3Vx} pins to GNDx. 1- μF capacitors are recommended to be placed placed very close to V_{BUSx} pins to GNDx.

These decoupling capacitor recommendations are irrespective of whether the 3.3 V supplies are provided externally or generated using internal LDOs.

Refer to the [Section 11.1.1](#) section for recommended placement of the decoupling capacitors. Small footprint capacitors (0402/0201) are recommended so that these may be placed very close to the supply pins and corresponding ground pins on the top layer without the use of vias.

While isolating a host/hub or bus-powered peripherals, isolated power is needed and can be generated with the help of a transformer driver such as TI's [SN6505B](#). For such applications, detailed power supply design, and transformer selection recommendations are available in the [SN6505 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies](#) data sheet.

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Typical Application

10.1.1 Isolated Host or Hub

Figure 10-1 shows an application for isolating a host or a hub using ISOUSB111. In this example, on the microcontroller side, V_{3P3V1} and V_{BUS1} are together connected to an external 3.3-V supply. On the connector side, the VBUS from the USB connector is connected to V_{BUS2} and the V_{3P3V2} supply is generated using the internal 3.3-V LDO.

Decoupling capacitors are placed next to ISOUSB111 according to the recommendations provided in the [Power Supply Recommendations](#) section. An isolated DC-DC converter (such as the SN6505) is to provide power to the VBUS using the 3.3-V local supply. Note that, for a host or hub, the USB standard requires a 120- μ F capacitor to be placed on the VBUS so as to be able provide in-rush current when a downstream peripheral is attached. In addition, a 100-nF capacitor is recommended close to the VBUS pin to handle transient currents.

ESD diodes with low capacitance and low dynamic resistance, such as PESD5V0C1USF, may be placed on D+ and D- lines. A ferrite bead, with dc resistance less than 100 m Ω , may be optionally placed between VBUS pin of the connector and the V_{BUS} pin of ISOUSB111, as shown in the figure, to suppress transients such as ESD.

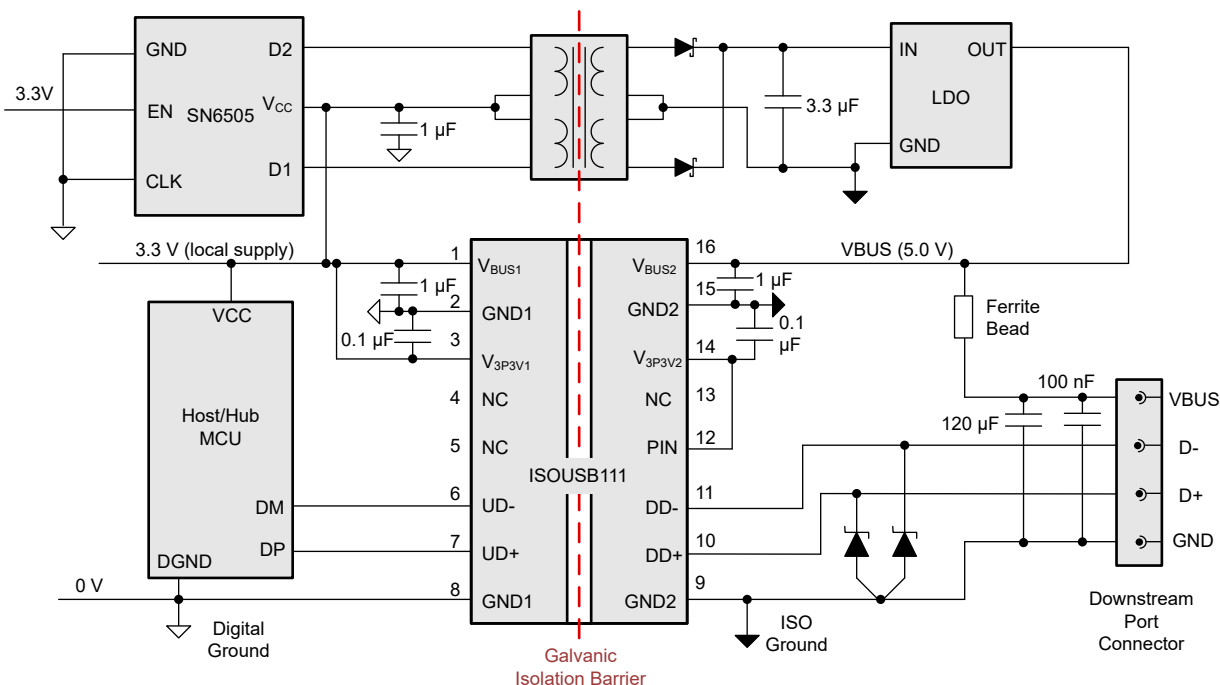


Figure 10-1. Isolated Host or Hub with ISOUSB111

10.1.2 Isolated Peripheral - Self-Powered

Figure 10-2 shows an application for isolating a self-powered peripheral using ISOUSB111. In this example, on the microcontroller side, V_{3P3V2} and V_{BUS2} are together connected to an external 3.3-V supply. On the connector side, the VBUS from the USB connector is connected to V_{BUS1} and the V_{3P3V1} supply is generated using the internal 3.3-V LDO.

Decoupling capacitors are placed next to ISOUSB111 according to the recommendations provided in the [Power Supply Recommendations](#) section. Note that the USB standard requires that, for a peripheral, the total capacitor value on VBUS must be less than 10- μ F. A 100-nF capacitor is recommended close to the VBUS pin to handle transient currents.

ESD diodes with low capacitance and low dynamic resistance, such as PESD5V0C1USF, may be placed on D+ and D- lines. A ferrite bead, with dc resistance less than 100 m Ω , may be optionally placed between VBUS pin of the connector and the V_{BUS} pin of ISOUSB111, as shown in the figure, to suppress transients such as ESD.

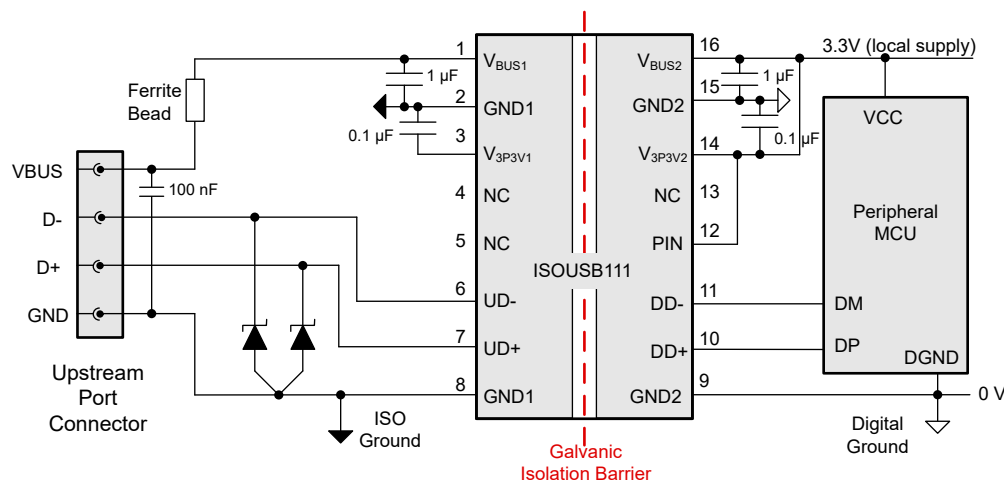


Figure 10-2. Isolated Self-Powered Peripheral with ISOUSB111

10.1.3 Isolated Peripheral - Bus-Powered

[Figure 10-3](#) shows an application for isolating a self-powered peripheral using ISOUSB111. In this example, an isolated DC-DC converter (for example: SN6505) is used to create a 3.3-V local supply while deriving power from the USB VBUS. On the microcontroller side, V_{3P3V2} and V_{BUS2} are together connected to an external 3.3-V supply. On the connector side, the VBUS from the USB connector is connected to V_{BUS1} and the V_{3P3V1} supply is generated using the internal 3.3-V LDO.

Decoupling capacitors are placed next to ISOUSB111 according to the recommendations provided in the [Power Supply Recommendations](#) section. Note that the USB standard requires that, for a peripheral, the total capacitor value on VBUS, including any decoupling capacitors reflected from the secondary side through the isolated DC-DC converter, must be less than 10- μ F. A 100-nF capacitor is recommended close to the VBUS pin to handle transient currents.

ESD diodes with low capacitance and low dynamic resistance, such as PESD5V0C1USF, may be placed on D+ and D- lines. A ferrite bead, with dc resistance less than 100 mΩ, may be optionally placed between VBUS pin of the connector and the V_{BUS} pin of ISOUSB111, as shown in the figure, to suppress transients such as ESD.

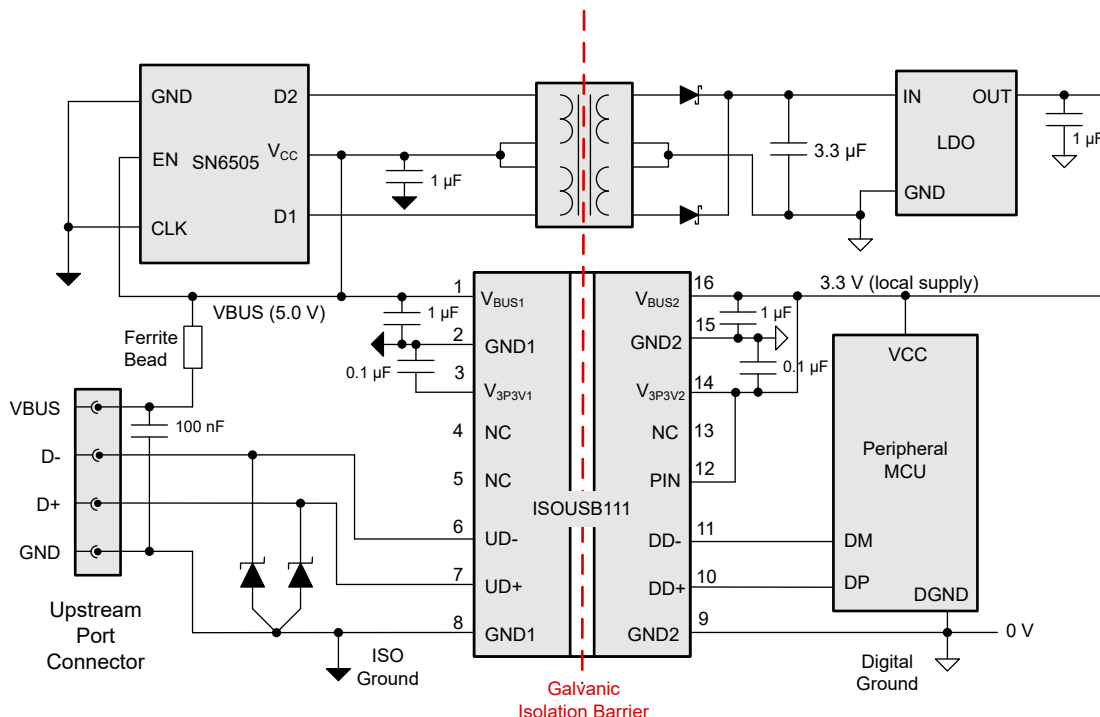


Figure 10-3. Isolated Bus-Powered Peripheral using ISOUSB111

10.1.4 Application Curve

10.1.4.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See [Figure 10-4](#) for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 50% for lifetime which translates into minimum required insulation lifetime of 30 years at a working voltage that's 20% higher than the specified value.

[Figure 10-5](#) shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 1500 V_{RMS} with a lifetime of 169 years. Other factors, such as package size, pollution degree, material group, etc. can further limit the working voltage of the component. The working voltage of DW-16 and DWX-16 packages is specified upto 1500 V_{RMS}. At the lower working voltages, the corresponding insulation lifetime is much longer than 169 years.

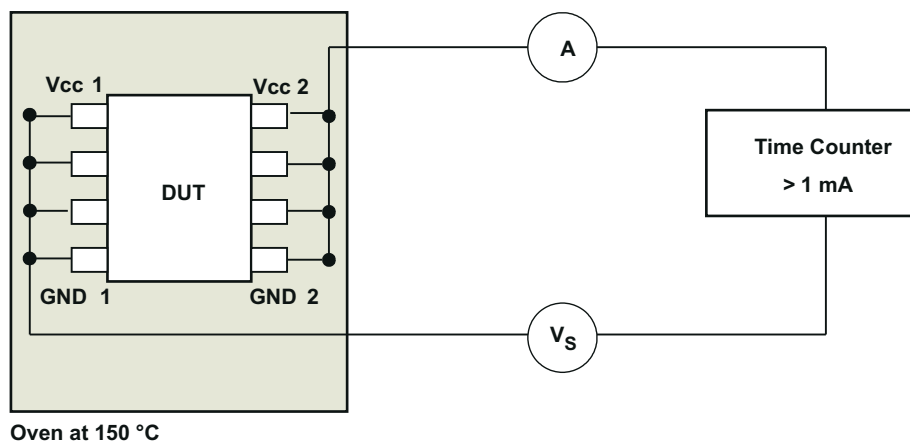


Figure 10-4. Test Setup for Insulation Lifetime Measurement

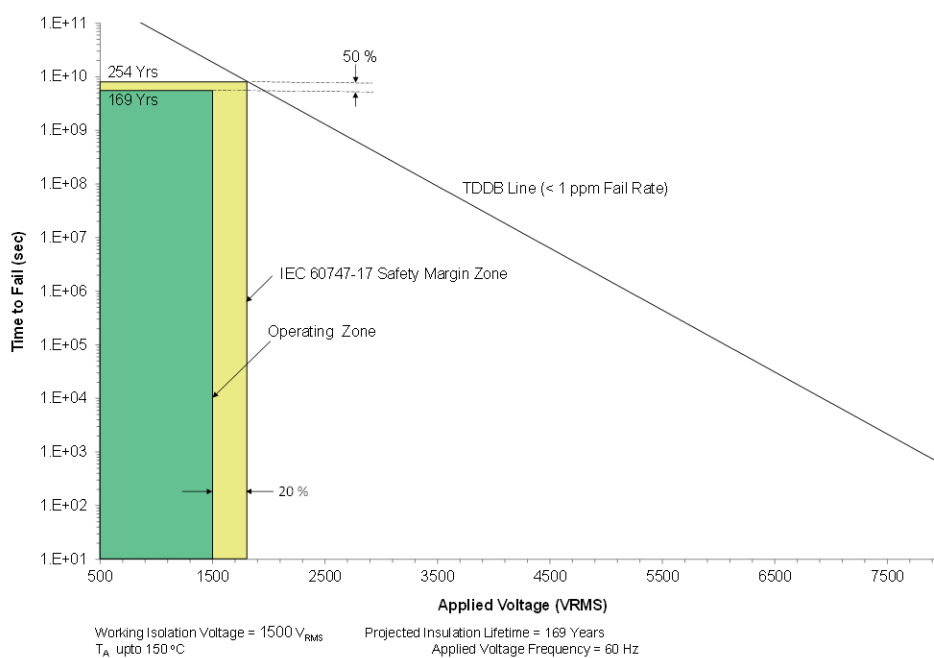


Figure 10-5. Insulation Lifetime Projection Data

11 Layout

11.1 Layout Guidelines

Two layers are sufficient to accomplish a low EMI PCB design.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- For best performance, it is recommended to minimize the length of D+/D- board traces from the MCU to ISOUSB111, and from ISOUSB111 to the connector. Vias and stubs on D+/D- lines must be avoided.
- Placing a solid ground plane just below the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow. D+ and D- traces must be designed for 90- Ω differential impedance and as close to 45- Ω single ended impedance as possible.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in².
- Decoupling capacitors must be placed on the top layer, and the routing between the capacitors and the corresponding to supply and ground pins must be completed in the top layer itself. There should not be any vias in the routing path between the decoupling capacitors and the corresponding supply and ground pins.
- ESD structures must be placed on the top layer, close to the connector, and right on the D+/D- traces without vias. Ground routing for the ESD structures must be made in the top layer if possible, else must have a strong connection to the ground plane with multiple vias.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

11.1.1 Layout Example

The layout example in this section shows the recommended placement for de-coupling capacitors and ESD protection diodes. A continuous ground plane is recommended below the D+/D- signal traces. Small footprint capacitors (0402/0201) are recommended so that these may be placed very close to the supply pins and corresponding ground pins and connected using the top layer. There should not be any vias in the routing path between the decoupling capacitors and the corresponding supply and ground pins. The ESD protection diodes should be placed close to the connector with a strong connection to the ground plane. The example shown is for an isolated host or hub, but similar considerations apply for isolated peripherals also. The 120- μ F capacitor on VBUS only applies to host or hub and should not be used for peripherals. A ferrite bead, with dc resistance less than 100 m Ω , may be optionally placed on the VBUS route, after the 100-nF (and 120- μ F) capacitors to prevent transients such as ESD from affecting the rest of the circuits.

For best performance, it is recommended to minimize the length of D+/D- board traces from the MCU to ISOUSB111, and from ISOUSB111 to the connector. Vias and stubs on D+/D- lines must be avoided.

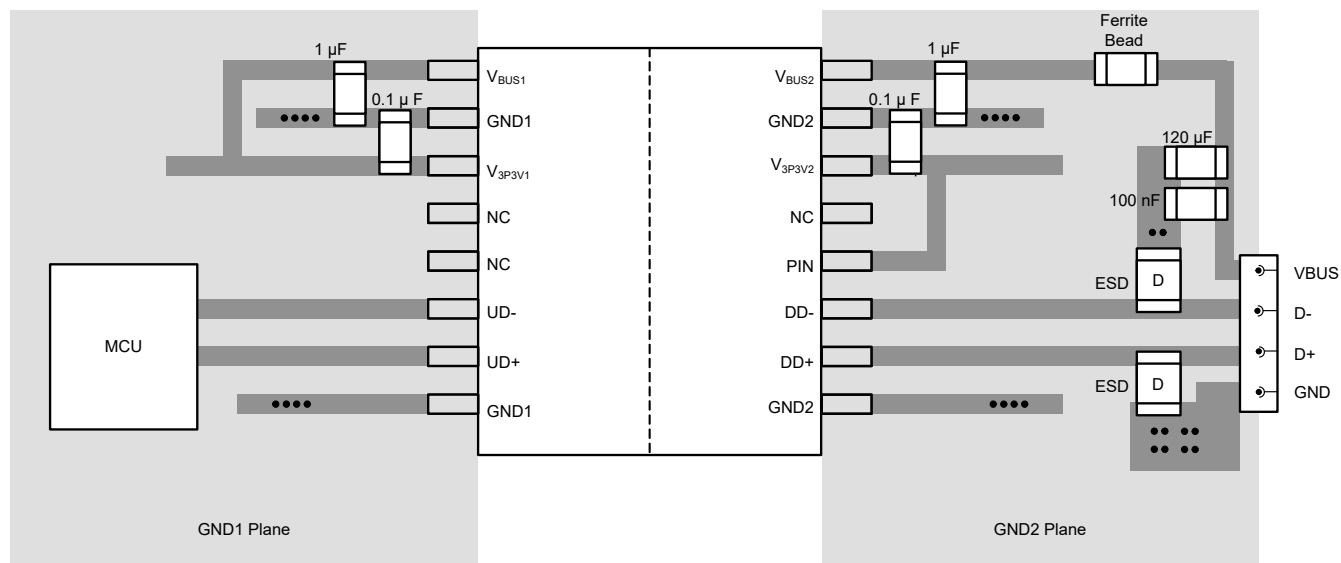


Figure 11-1. Layout Example for ISOUSB111

11.1.2 PCB Material

For digital circuit boards operating at less than 500 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over lower-cost alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Digital Isolator Design Guide](#)
- Texas Instruments, [Isolation Glossary](#)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

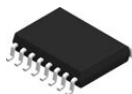
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

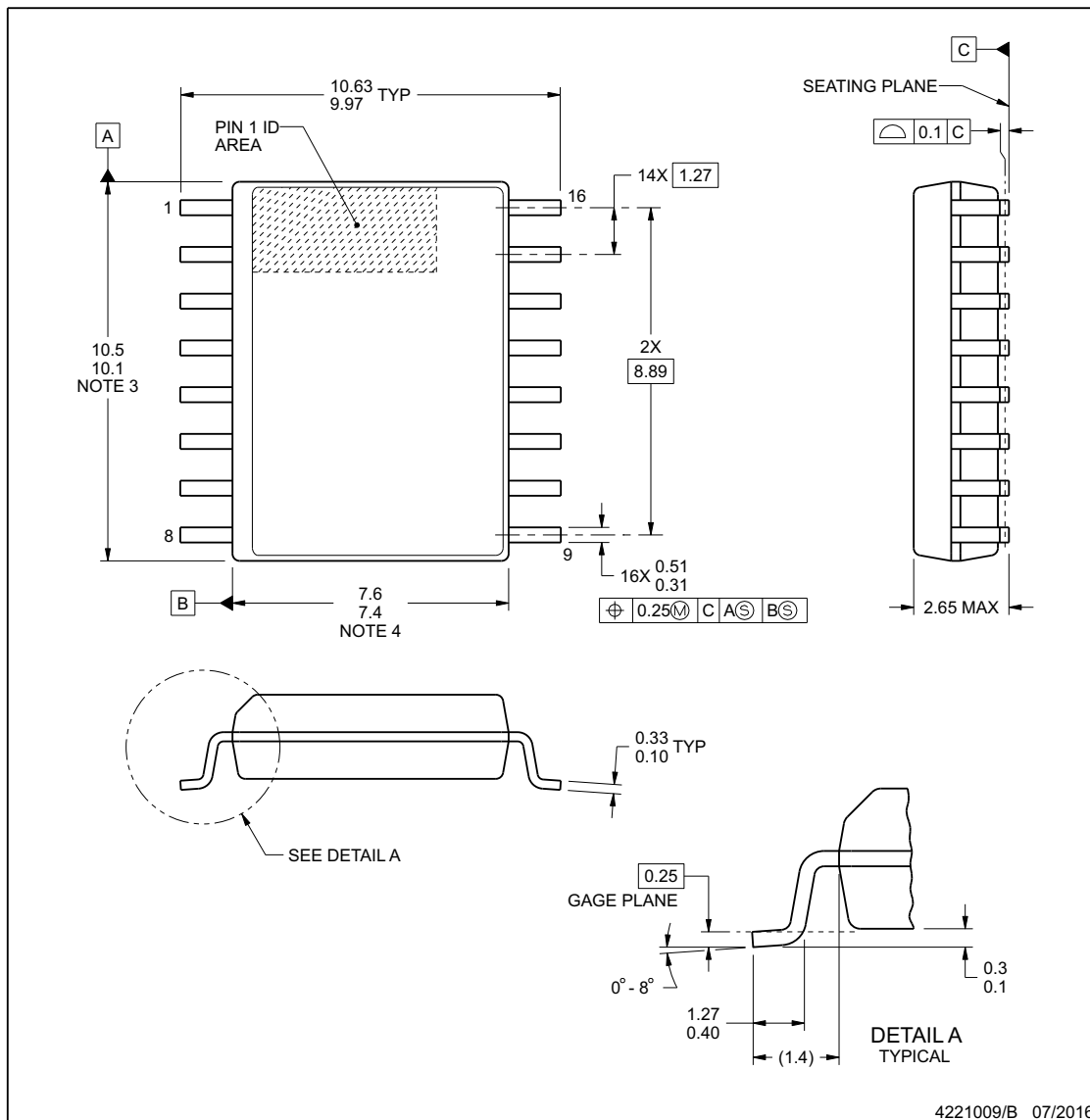
13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



PACKAGE OUTLINE
SOIC - 2.65 mm max height

SOIC

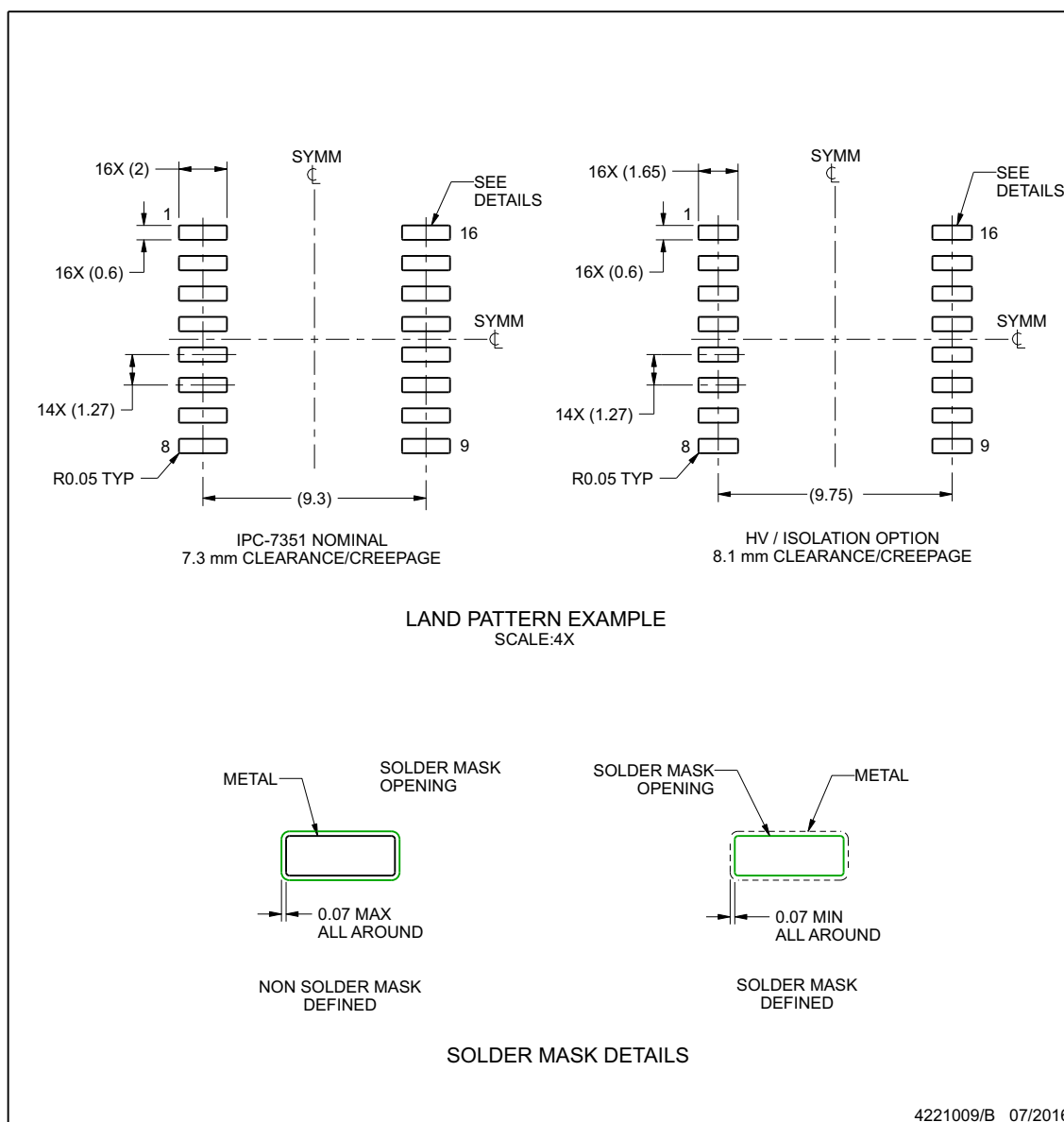


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT**DW0016B****SOIC - 2.65 mm max height**

SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

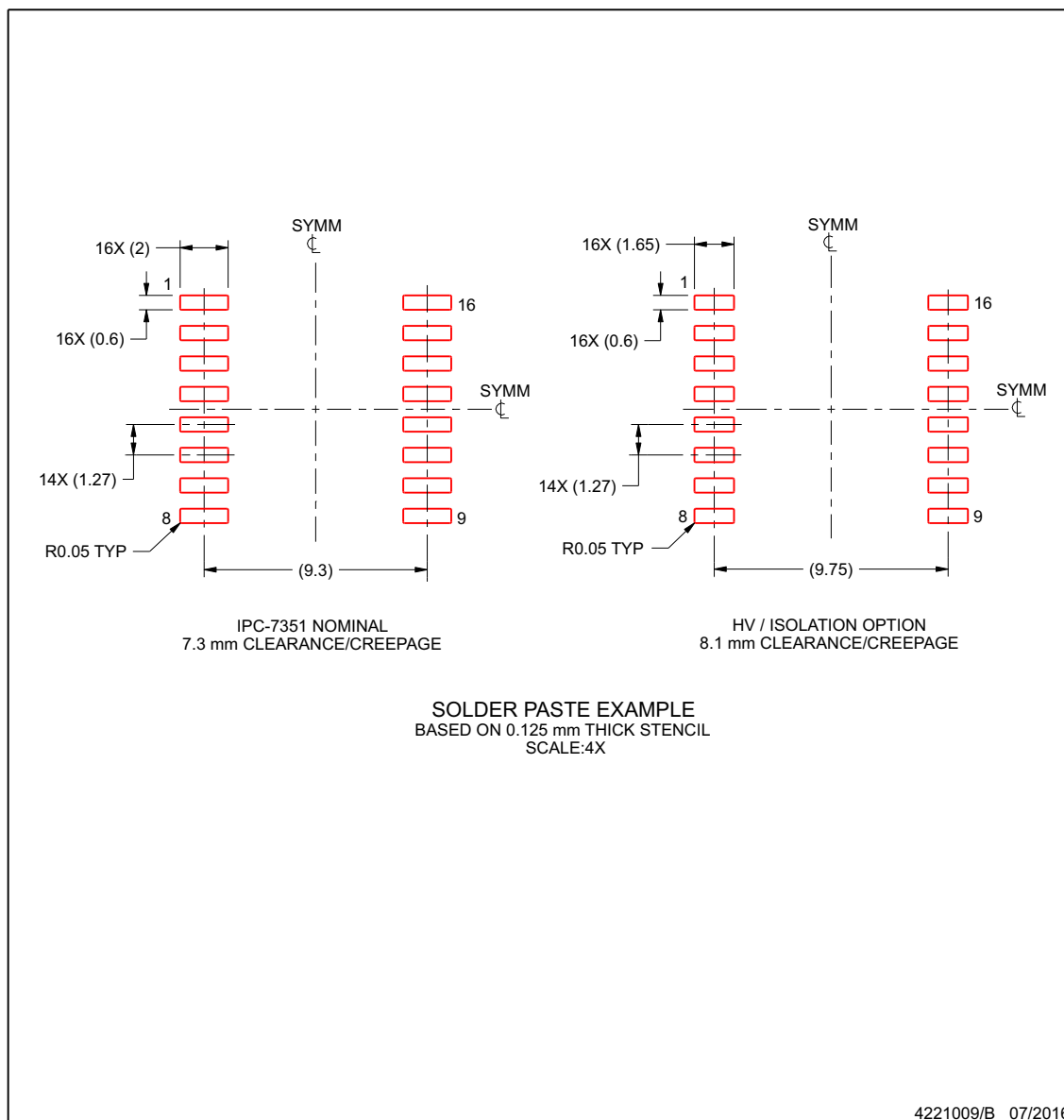
www.ti.com

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



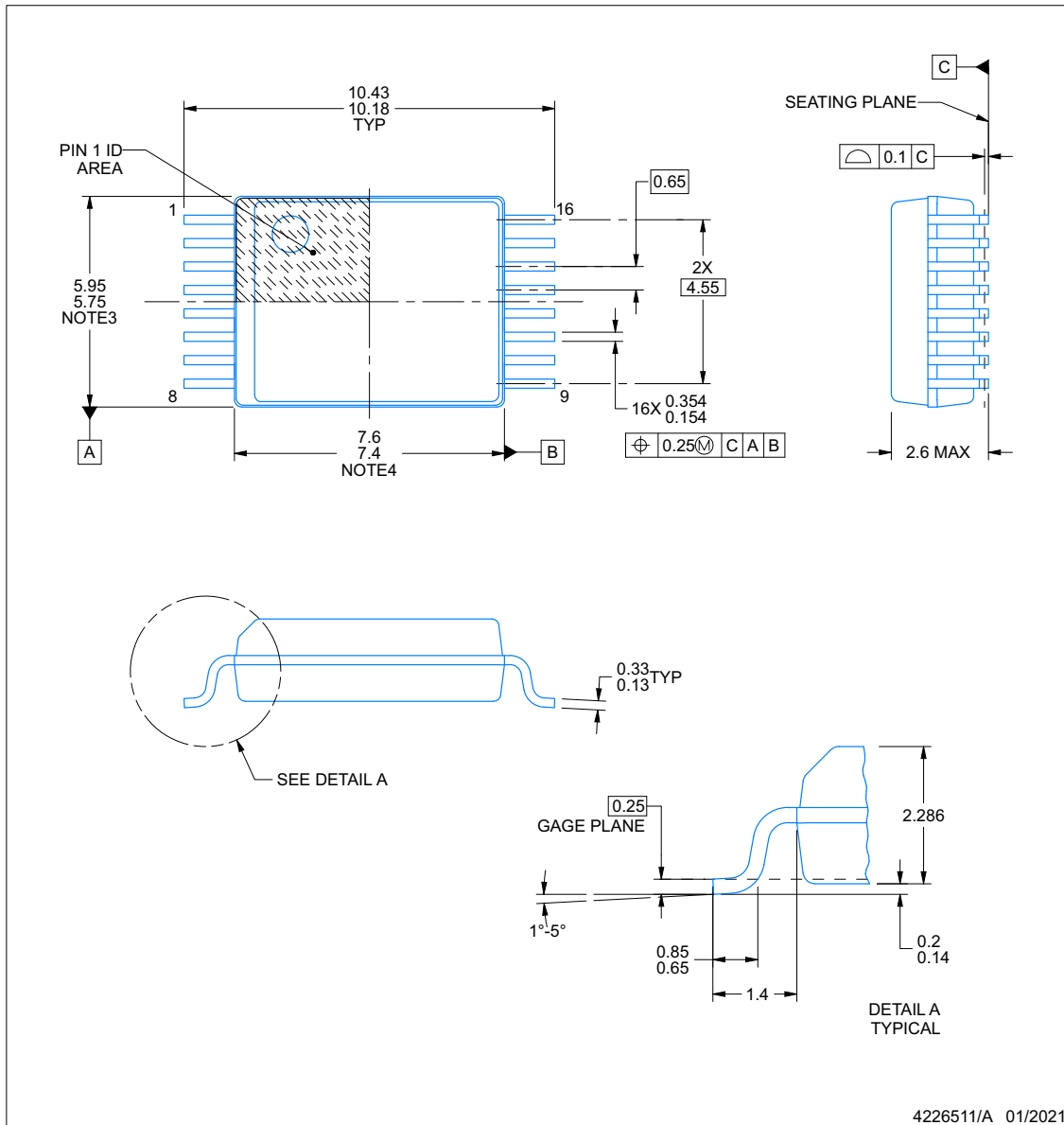
NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

www.ti.com

PACKAGE OUTLINE**DWX0016A****SSOP - 2.6 mm max height**

SMALL OUTLINE PACKAGE

**NOTES:**

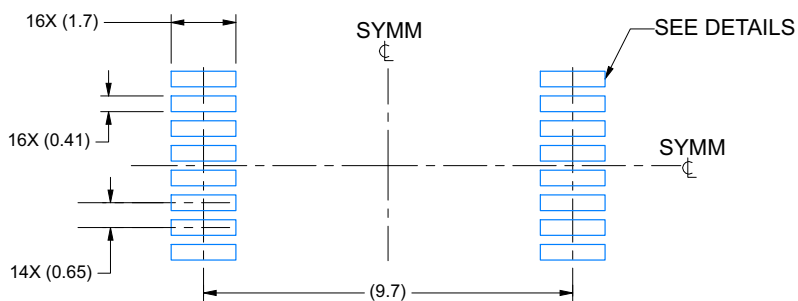
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Ref. JEDEC registration MS-013

EXAMPLE BOARD LAYOUT

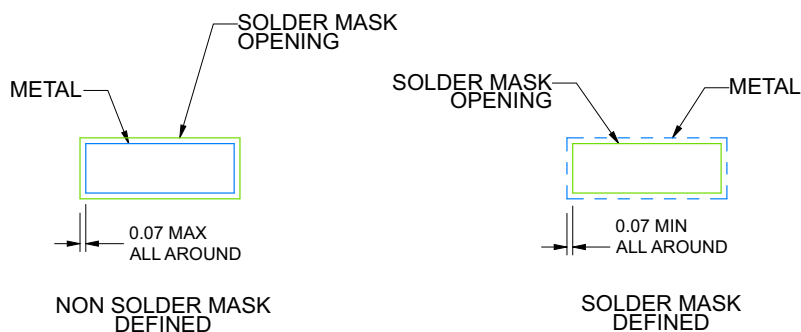
DWX0016A

SSOP - 2.6 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 6X



SOLDER MASK DETAILS

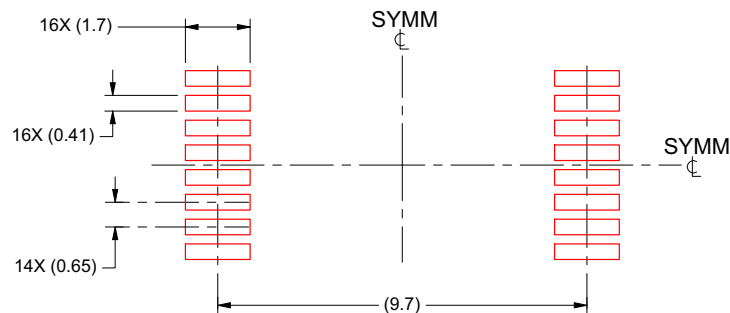
4226511/A 01/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN**DWX0016A****SSOP - 2.6 mm max height**

SMALL OUTLINE PACKAGE



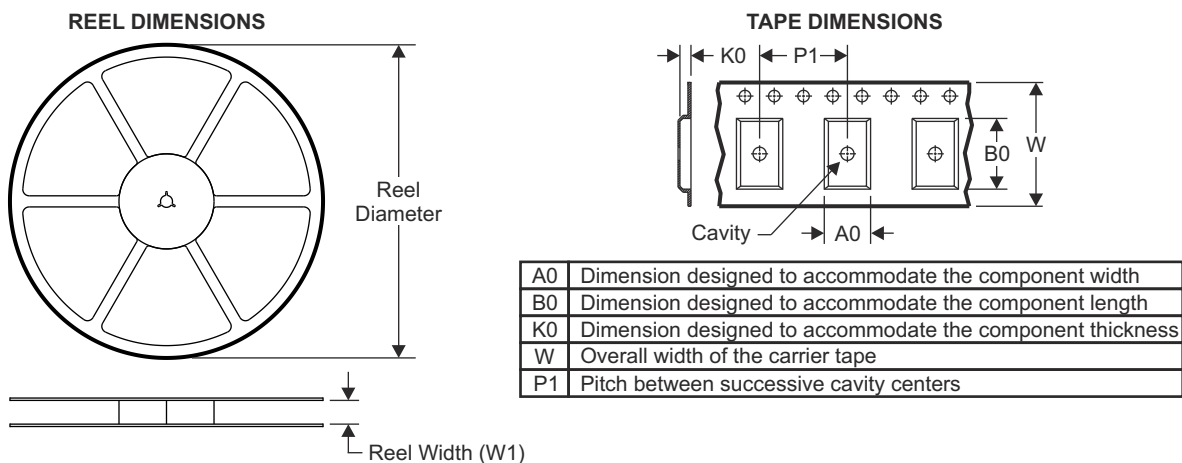
SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE: 6X

4226511/A 01/2021

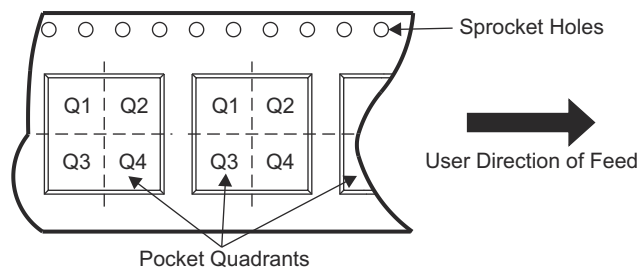
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

13.1 Tape and Reel Information

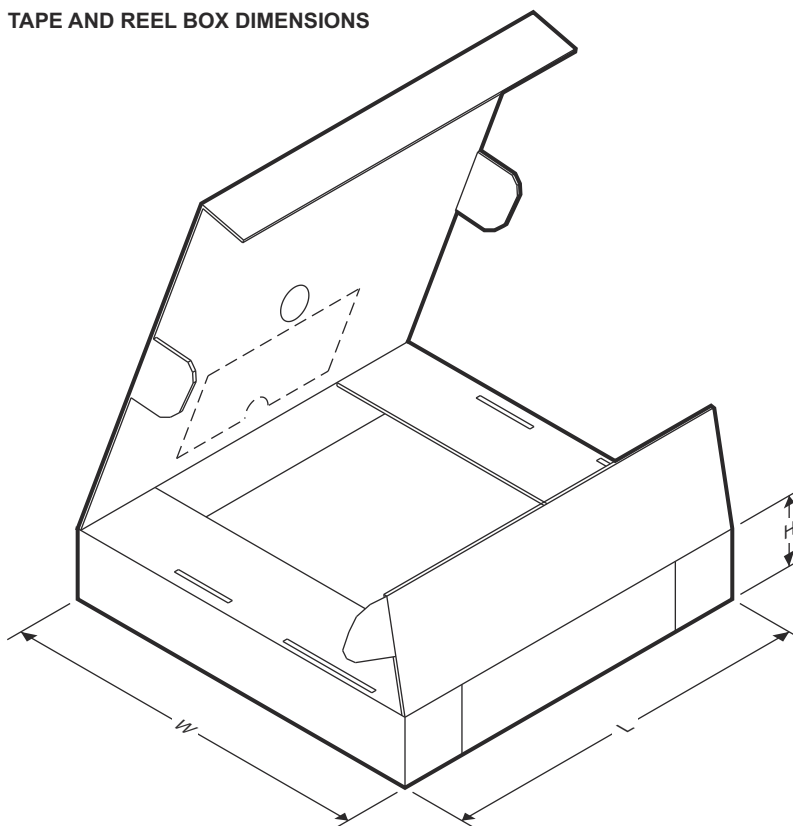


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISOUSB111DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISOUSB111DWXR	SSOP	DWX	16	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISOUSB111DWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISOUSB111DWXR	SSOP	DWX	16	1000	350.0	350.0	43.0

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISOUSB111DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOUSB111	Samples
XISOUSB111DWR	ACTIVE	SOIC	DW	16	2000	TBD	Call TI	Call TI	-40 to 125		Samples
XISOUSB111DWXR	ACTIVE	SSOP	DWX	16	1000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISOUSB111DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISOUSB111DWR	SOIC	DW	16	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated