LDC1312-Q1, LDC1314-Q1 Multi-Channel 12-Bit Inductance to Digital Converter (LDC) for Inductive Sensing

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1:–40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C5
- Easy-to-use – Minimal Configuration Required
- Measure up to 4 Sensors with One IC
- Multiple Channels Support Environmental and Aging Compensation
- Multi-Channel Remote Sensing Provides Lowest System Cost
- Pin-Compatible Medium and High-resolution Options
  - LDC1312-Q1/LDC1314-Q1: 2/4-ch 12-bit LDC
  - LDC1612-Q1/LDC1614-Q1: 2/4-ch 28-bit LDC
- Supports Wide Sensor Frequency Range of 1kHz to 10MHz
- Power Consumption:
  - 35 µA Low Power Sleep Mode
  - 200 nA Shutdown Mode
- 3.3V Operation
- Support Internal or External Reference Clock
- Immune to DC Magnetic Fields and Magnets

2 Applications

- Automotive Buttons and Knobs
- Linear and Rotational Encoders
- Slider Buttons
- Metal Detection in Industrial and Automotive
- Flow Meters

3 Description

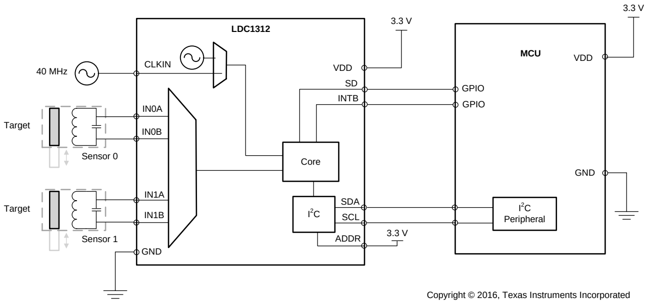
The LDC1312-Q1 and LDC1314-Q1 are 2- and 4-channel, 12-bit inductance to digital converters (LDCs) for inductive sensing solutions. With multiple channels and support for remote sensing, the LDC1312-Q1 and LDC1314-Q1 enable the performance and reliability benefits of inductive sensing to be realized at minimal cost and power. The products are easy to use, only requiring that the sensor frequency be within 1 kHz and 10 MHz to begin sensing. The wide 1 kHz to 10 MHz sensor frequency range also enables use of very small PCB coils, further reducing sensing solution cost and size.

Device Information[1]

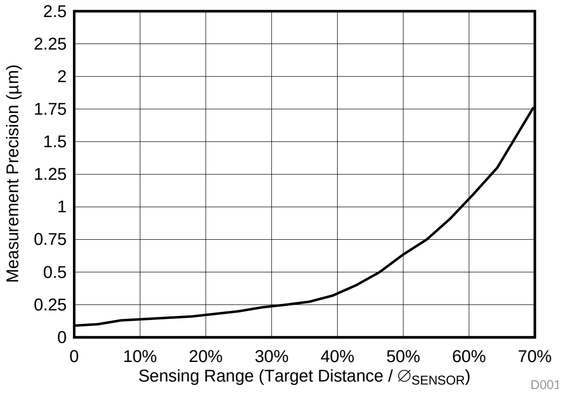
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LDC1312-Q1	WSON (12)	4.00 mm × 4.00 mm
LDC1314-Q1	WQFN (16)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Measurement Precision vs. Target Distance



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4 Revision History

DATE	REVISION	NOTES
April 2016	*	Initial release.

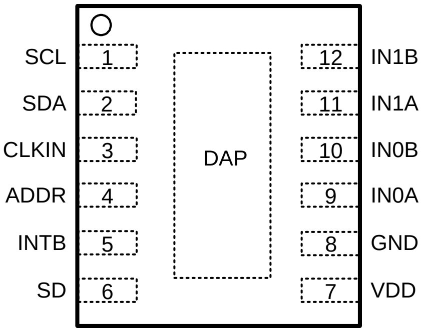
5 Description Continued

The LDC1312-Q1 and LDC1314-Q1 offer well-matched channels, which allow for differential and ratiometric measurements. This enables designers to use one channel to compensate their sensing for environmental and aging conditions such as temperature, humidity, and mechanical drift. Given their ease of use, low power, and low system cost these products enable designers to greatly improve on existing sensing solutions and to introduce brand new sensing capabilities to products in all markets, especially consumer and industrial applications. Inductive sensing offers better performance, reliability, and flexibility than competitive sensing technologies at lower system cost and power.

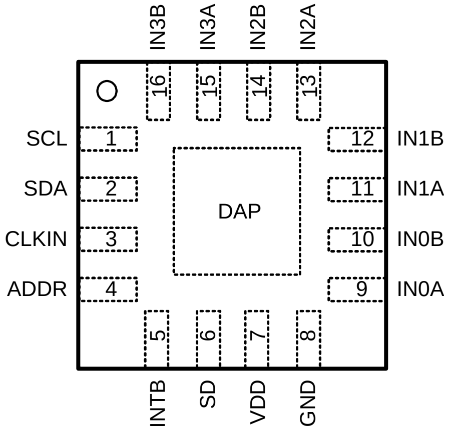
The LDC1312-Q1 and LDC1314-Q1 are easily configured via an I2C interface. The two-channel LDC1312-Q1 is available in a WSON-12 package and the four-channel LDC1314-Q1 is available in a WQFN-16 package.

6 Pin Configuration and Functions

**LDC1312-Q1 DNT
12 pin WSON
Top View**



**LDC1314-Q1 RGH
16 pin WQFN
Top View**



Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	SCL	I	I2C Clock input
2	SDA	I/O	I2C Data input/output
3	CLKIN	I	Master Clock input. Tie this pin to GND if internal oscillator is selected
4	ADDR	I	I2C Address selection pin: when ADDR=L, I2C address = 0x2A, when ADDR=H, I2C address = 0x2B.
5	INTB	O	Configurable Interrupt output pin
6	SD	I	Shutdown input
7	VDD	P	Power Supply
8	GND	G	Ground
9	IN0A	A	External LC sensor 0 connection
10	IN0B	A	External LC sensor 0 connection
11	IN1A	A	External LC sensor 1 connection
12	IN1B	A	External LC sensor 1 connection
13	IN2A	A	External LC sensor 2 connection (LDC1314 only)
14	IN2B	A	External LC sensor 2 connection (LDC1314 only)
15	IN3A	A	External LC sensor 3 connection (LDC1314 only)
16	IN3B	A	External LC sensor 3 connection (LDC1314 only)
DAP	DAP[2]	N/A	Connect to Ground

(1) I = Input, O = Output, P=Power, G=Ground, A=Analog
(2) There is an internal electrical connection between the exposed Die Attach Pad (DAP) and the GND pin of the device. Although the DAP can be left floating, for best performance the DAP should be connected to the same potential as the device's GND pin. Do not use the DAP as the primary ground for the device. The device GND pin must always be connected to ground.

7 Specifications

7.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
V_{DD}	Supply Voltage		5	V
Vi	Voltage on any pin	–0.3	VDD+0.3	V
IA	Input current on any INx pin	–8	8	mA
ID	Input current on any Digital pin	–5	5	mA
Tj	Junction Temperature	–55	150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

Unless otherwise specified, all limits ensured for T_A = 25°C, VDD = 3.3 V

		MIN	NOM	MAX	UNIT
VDD	Supply Voltage	2.7		3.6	V
T_A	Operating Temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC[1]		LDC1312	LDC1314	UNIT
		DNT (WSON)	RGH (WQFN)	
		12 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.7	35.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.2	36.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14	13.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.2	13.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.5	3.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics (1)

Unless otherwise specified, all limits ensured for T_A = 25°C, VDD = 3.3 V

PARAMETER		TEST CONDITIONS(2)	MIN(3)	TYP(4)	MAX(3)	UNIT
POWER						
V_{DD}	Supply Voltage	T_A = –40°C to +125°C	2.7		3.6	V
I_{DD}	Supply Current (not including sensor current)(5)	CLKIN = 10MHz (6)		2.1		mA
I_{DDSL}	Sleep Mode Supply Current(5)			35	60	µA
I_{SD}	Shutdown Mode Supply Current(5)			0.2	1	µA
SENSOR						
$I_{SENSORMAX}$	Sensor Maximum Current drive	HIGH_CURRENT_DRV = b0 DRIVE_CURRENT_CHx = 0xF800		1.5		mA
R_P	Sensor R_P		1		100	kΩ
$IHD_{SENSORMAX}$	High current sensor drive mode: Sensor Maximum Current	HIGH_CURRENT_DRV = b1 DRIVE_CURRENT_CH0 = 0xF800 Channel 0 only		6		mA
$R_{P\_HD\_MIN}$	Minimum sensor R_P			250		Ω
f_{SENSOR}	Sensor Resonance Frequency	T_A = –40°C to +125°C	0.001		10	MHz
$V_{SENSORMAX}$	Maximum oscillation amplitude (peak)			1.8		V
N_{BITS}	Number of bits	RESET_DEV.OUTPUT_GAIN=b00 RCOUNT ≥ 0x0400			12	bits
f_{CS}	Maximum Channel Sample Rate	single active channel continuous conversion, SCL=400kHz			13.3	kSPS
C_{IN}	Sensor Pin input capacitance			4		pF
MASTER CLOCK						
f_{CLKIN}	External Master Clock Input Frequency (CLKIN)	T_A = –40°C to +125°C	2		40	MHz
$CLKIN_{DUTY\_MIN}$	External Master Clock minimum acceptable duty cycle (CLKIN)			40%		
$CLKIN_{DUTY\_MAX}$	External Master Clock maximum acceptable duty cycle (CLKIN)			60%		
V_{CLKIN_LO}	CLKIN low voltage threshold				0.3×VDD	V
V_{CLKIN_HI}	CLKIN high voltage threshold		0.7×VDD			V
f_{INTCLK}	Internal Master Clock Frequency range		35	43.4	55	MHz
$T_{Cf\_int\_\mu}$	Internal Master Clock Temperature Coefficient mean			–13		ppm/°C

(1) Electrical Characteristics Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that TJ = TA. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

(2) Register values are represented as either binary (b is the prefix to the digits), or hexadecimal (0x is the prefix to the digits). Decimal values have no prefix.

(3) Limits are ensured by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(4) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

(5) I2C read/write communication and pullup resistors current through SCL, SDA not included.

(6) Sensor inductor: 2 layer, 32 turns/layer, 14mm diameter, PCB inductor with L=19.4 µH, R_P=5.7 kΩ at 2MHz Sensor capacitor: 330 pF 1% COG/NP0 Target: Aluminum, 1.5mm thickness Channel = Channel 0 (continuous mode) CLKIN = 40 MHz, CHx_FIN_DIVIDER = b0000, CHx_FREF_DIVIDER = b00 0000 0001 CH0_RCOUNT = 0xFFFF, SETTLECOUNT_CH0 = 0x0100 RP_OVERRIDE = b1, AUTO_AMP_DIS = b1, DRIVE_CURRENT_CH0 = 0x9800

7.6 Timing Characteristics

		MIN	NOM	MAX	UNIT
t_{WAKEUP}	Wake-up Time from SD high-low transition to I2C readback			2	ms
$t_{WD\text{-}TIMEOUT}$	Sensor recovery time (after watchdog timeout)		5.2		ms

7.7 Switching Characteristics - I2C

Unless otherwise specified, all limits ensured for T_A = 25°C, VDD = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE LEVELS						
V_{IH}	Input High Voltage		$0.7{\times}V_{DD}$			V
V_{IL}	Input Low Voltage				$0.3{\times}V_{DD}$	V
V_{OL}	Output Low Voltage (3mA sink current)				0.4	V
HYS	Hysteresis			$0.1{\times}V_{DD}$		V
I2C TIMING CHARACTERISTICS						
f_{SCL}	Clock Frequency		10		400	kHz
t_{LOW}	Clock Low Time		1.3			µs
t_{HIGH}	Clock High Time		0.6			µs
$t_{HD;STA}$	Hold Time (repeated) START condition	After this period, the first clock pulse is generated	0.6			µs
$t_{SU;STA}$	Set-up time for a repeated START condition		0.6			µs
$t_{HD;DAT}$	Data hold time		0			µs
$t_{SU;DAT}$	Data setup time		100			ns
$t_{SU;STO}$	Set-up time for STOP condition		0.6			µs
t_{BUF}	Bus free time between a STOP and START condition		1.3			µs
$t_{VD;DAT}$	Data valid time				0.9	µs
$t_{VD;ACK}$	Data valid acknowledge time				0.9	µs
t_{SP}	Pulse width of spikes that must be suppressed by the input filter(1)				50	ns

(1) This parameter is specified by design and/or characterization and is not tested in production.

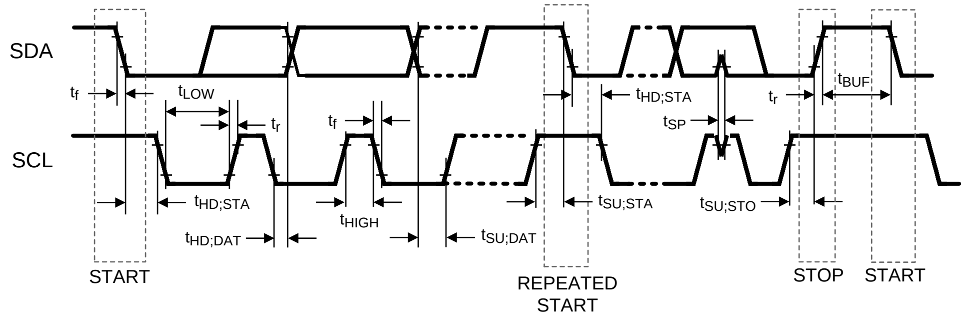
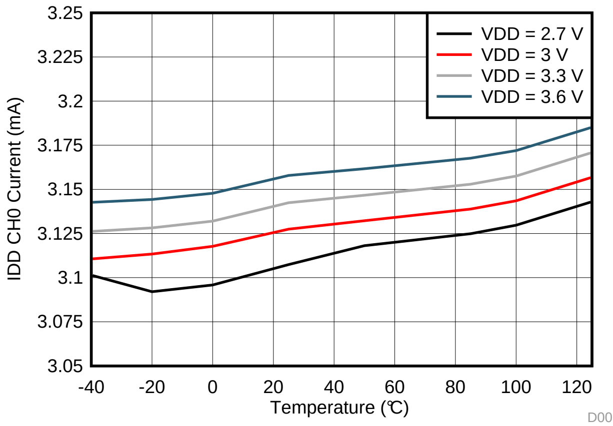


Figure 1. I2C Timing

7.8 Typical Characteristics

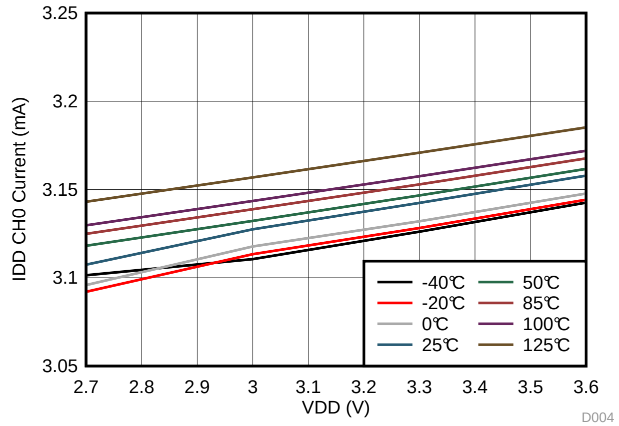
Common test conditions (unless specified otherwise): Sensor inductor: 2 layer, 32 turns/layer, 14 mm diameter, PCB inductor with L=19.4 µH, R_P=5.7 kΩ at 2 MHz; Sensor capacitor: 330 pF 1% COG/NP0; Target: Aluminum, 1.5mm thickness; Channel = Channel 0 (continuous mode); CLKIN = 40 MHz, CHx_FIN_DIVIDER = 0x1, CHx_FREF_DIVIDER = 0x001, CH0_RCOUNT = 0xFFFF, SETTLECOUNT_CH0 = 0x0100, RP_OVERRIDE = 1, AUTO_AMP_DIS = 1, DRIVE_CURRENT_CH0 = 0x9800



Includes 1.57 mA sensor coil current

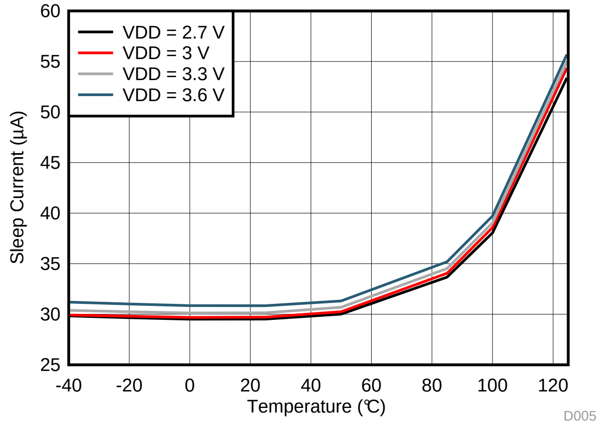
–40°C to +125°C

Figure 2. Active Mode I_{DD} vs. Temperature



Includes 1.57 mA sensor coil current

Figure 3. Active Mode I_{DD} vs. V_{DD}



–40°C to +125°C

Figure 4. Sleep Mode I_{DD} vs. Temperature

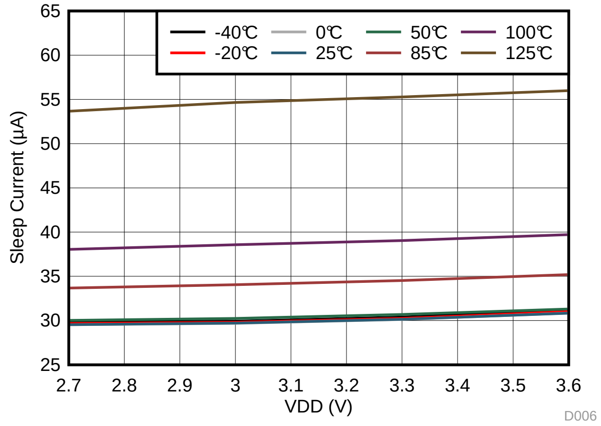
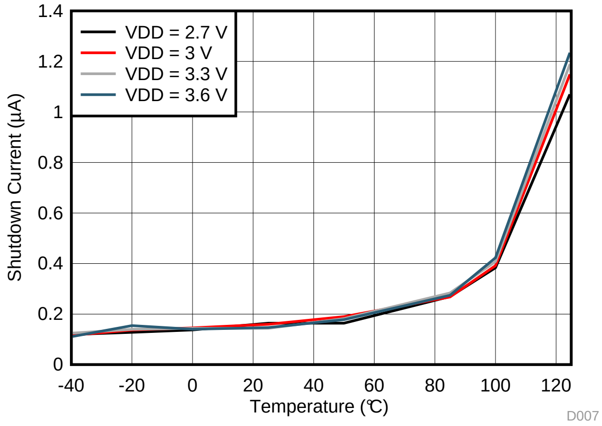


Figure 5. Sleep Mode I_{DD} vs. V_{DD}



–40°C to +125°C

Figure 6. Shutdown Mode I_{DD} vs. Temperature

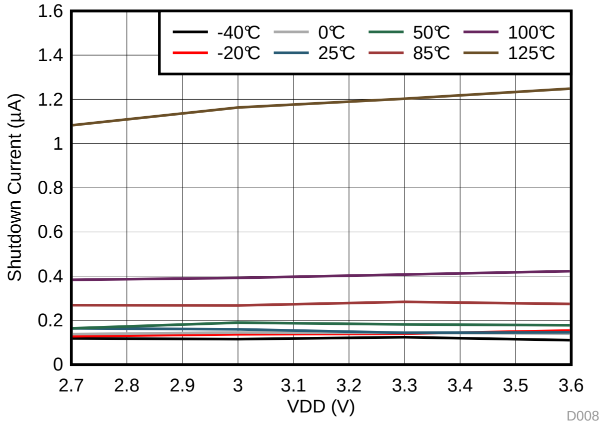
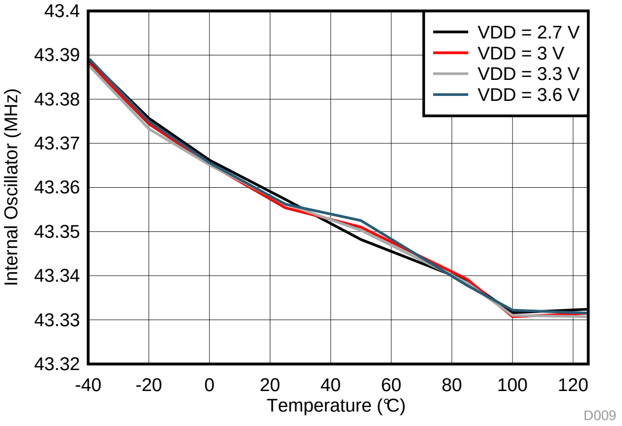


Figure 7. Shutdown Mode I_{DD} vs. V_{DD}

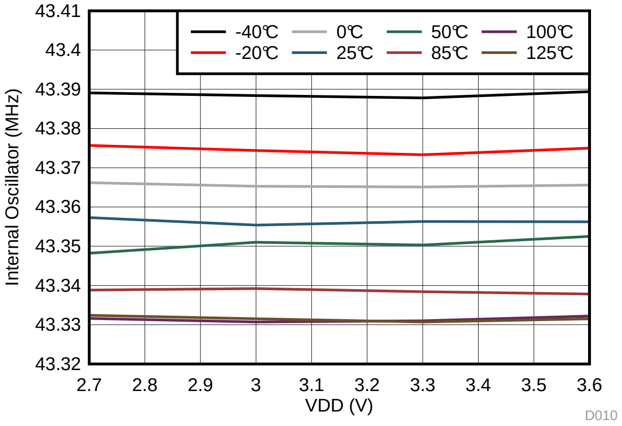
Typical Characteristics (continued)

Common test conditions (unless specified otherwise): Sensor inductor: 2 layer, 32 turns/layer, 14 mm diameter, PCB inductor with L=19.4 µH, R_P=5.7 kΩ at 2 MHz; Sensor capacitor: 330 pF 1% COG/NP0; Target: Aluminum, 1.5mm thickness; Channel = Channel 0 (continuous mode); CLKIN = 40 MHz, CHx_FIN_DIVIDER = 0x1, CHx_FREF_DIVIDER = 0x001, CH0_RCOUNT = 0xFFFF, SETTLECOUNT_CH0 = 0x0100, RP_OVERRIDE = 1, AUTO_AMP_DIS = 1, DRIVE_CURRENT_CH0 = 0x9800



–40°C to +125°C

Figure 8. Internal Oscillator Frequency vs. Temperature



Data based on 1 unit

Figure 9. Internal Oscillator Frequency vs. V_{DD}

8 Detailed Description

8.1 Overview

Conductive objects brought in contact with an AC electromagnetic (EM) field will induce field changes that can be detected using a sensor such as an inductor. Conveniently, an inductor, along with a capacitor, can be used to construct an L-C resonator, also known as an L-C tank, which can be used to produce an EM field. In the case of an L-C tank, the effect of the field disturbance is an apparent shift in the inductance of the sensor, which can be observed as a shift in the resonant frequency. Using this principle, the LDC1312/1314 is an inductance-to-digital converter (LDC) that measures the oscillation frequency of an LC resonator. The device outputs a digital value that is proportional to frequency. This frequency measurement can be converted to an equivalent inductance.

8.2 Functional Block Diagram

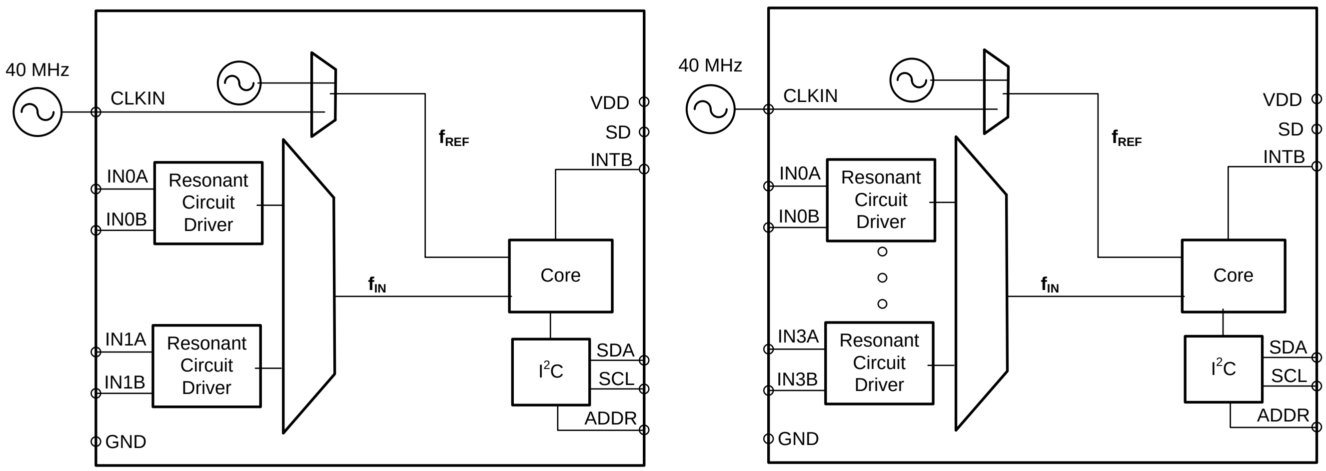


Figure 10. Block Diagrams for the LDC1312 (Left) and LDC1314 (Right)

The LDC1312/LDC1314 is composed of front-end resonant circuit drivers, followed by a multiplexer that sequences through the active channels, connecting them to the core that measures and digitizes the sensor frequency (f_{SENSOR}). The core uses a reference frequency (f_{REF}) to measure the sensor frequency. f_{REF} is derived from either an internal reference clock (oscillator), or an externally supplied clock. The digitized output for each channel is proportional to the ratio of f_{SENSOR}/f_{REF}. The I2C interface is used to support device configuration and to transmit the digitized frequency values to a host processor. The LDC can be placed in shutdown mode, saving current, using the SD pin. The INTB pin may be configured to notify the host of changes in system status.

8.3 Feature Description

8.3.1 Clocking Architecture

Figure 11 shows the clock dividers and multiplexers of the LDC.

Feature Description (continued)

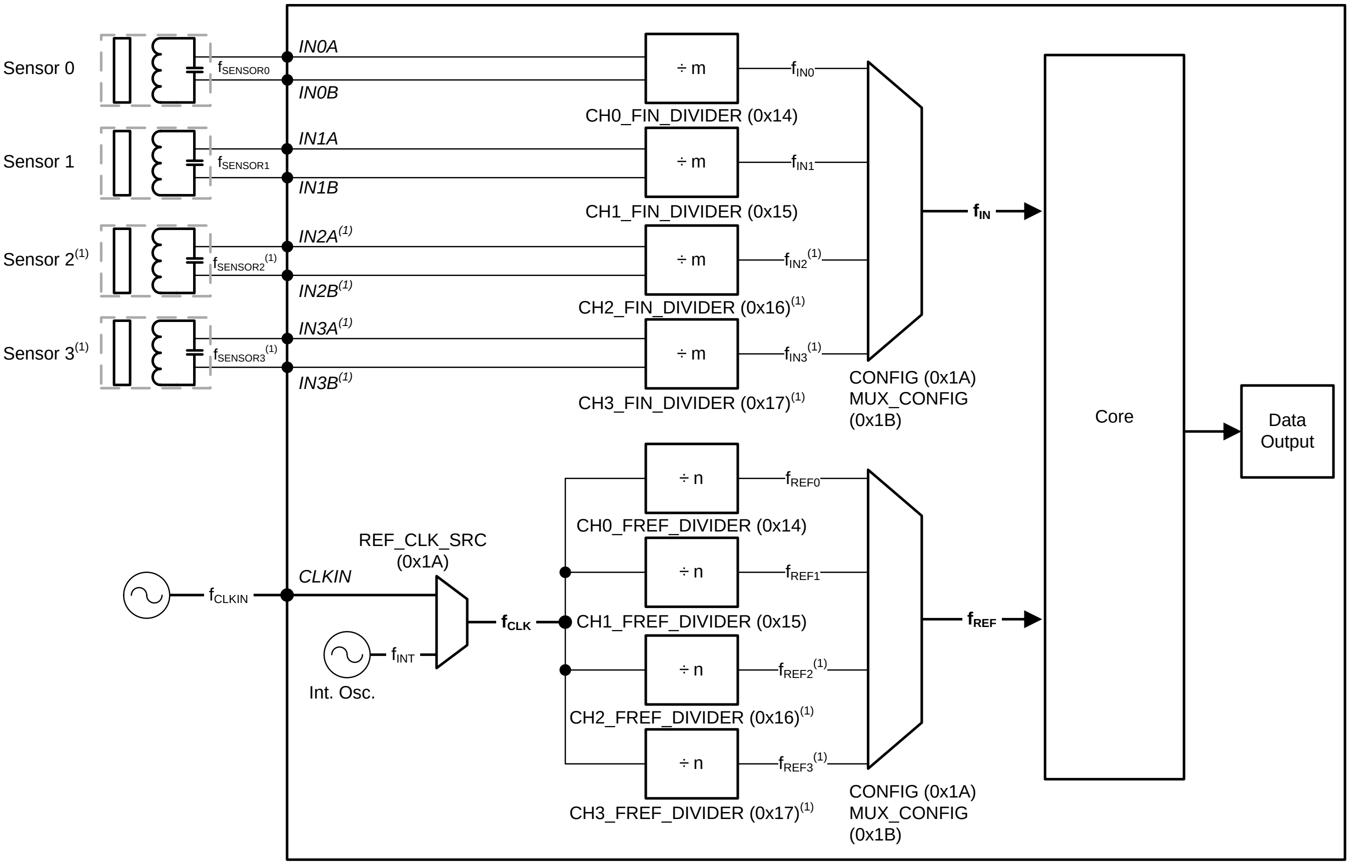


Figure 11. Clocking Diagram

(1) LDC1314 only

In Figure 11, the key clocks are f_{IN}, f_{REF}, and f_{CLK}. f_{CLK} is selected from either the internal clock source or external clock source (CLKIN). The frequency measurement reference clock, f_{REF}, is derived from the f_{CLK} source. TI recommends that precision applications use an external master clock that offers the stability and accuracy requirements needed for the application. The internal oscillator may be used in applications that require low cost and do not require high precision. The f_{INx} clock is derived from sensor frequency for a channel x, $f_{SENSORx}$. f_{REFx} and f_{INx} must meet the requirements listed in Table 1, depending on whether f_{CLK} (master clock) is the internal or external clock.

Table 1. Clock Configuration Requirements

MODE(1)	CLKIN SOURCE	VALID f_{REFx} RANGE (MHz)	VALID f_{INx} RANGE	SET CHx_FIN_DIVIDER to	SET CHx_SETTLECOUNT to	SET CHx_RCOUNT to
Multi-Channel	Internal	$f_{REFx} < 55$	$< f_{REFx} / 4$	≥ b0001 (2)	> 3	> 8
	External	$f_{REFx} < 40$				
Single-Channel	Either external or internal	$f_{REFx} < 35$				

(1) Channels 2 and 3 are only available for LDC1314
(2) If $f_{SENSOR} \geq 8.75$ MHz, then CHx_FIN_DIVIDER must be ≥ 2

Table 2 shows the clock configuration registers for all channels.

Table 2. Clock Configuration Registers

CHANNEL(1)	CLOCK	REGISTER	FIELD [BIT(S)]	VALUE
All	f_{CLK} = Master Clock Source	CONFIG, addr 0x1A	REF_CLK_SRC [9]	b0 = internal oscillator is used as the master clock b1 = external clock source is used as the master clock
0	f_{REF0}	CLOCK_DIVIDERS_CH0, addr 0x14	CH0_FREF_DIVIDER [9:0]	$f_{REF0} = f_{CLK}$ / CH0_FREF_DIVIDER
1	f_{REF1}	CLOCK_DIVIDERS_CH1, addr 0x15	CH1_FREF_DIVIDER [9:0]	$f_{REF1} = f_{CLK}$ / CH1_FREF_DIVIDER
2	f_{REF2}	CLOCK_DIVIDERS_CH2, addr 0x16	CH2_FREF_DIVIDER [9:0]	$f_{REF2} = f_{CLK}$ / CH2_FREF_DIVIDER
3	f_{REF3}	CLOCK_DIVIDERS_CH3, addr 0x17	CH3_FREF_DIVIDER [9:0]	$f_{REF3} = f_{CLK}$ / CH3_FREF_DIVIDER
0	f_{IN0}	CLOCK_DIVIDERS_CH0, addr 0x14	CH0_FIN_DIVIDER [15:12]	$f_{IN0} = f_{SENSOR0}$ / CH0_FIN_DIVIDER
1	f_{IN1}	CLOCK_DIVIDERS_CH1, addr 0x15	CH1_FIN_DIVIDER [15:12]	$f_{IN1} = f_{SENSOR1}$ / CH1_FIN_DIVIDER
2	f_{IN2}	CLOCK_DIVIDERS_CH2, addr 0x16	CH2_FIN_DIVIDER [15:12]	$f_{IN2} = f_{SENSOR2}$ / CH2_FIN_DIVIDER
3	f_{IN3}	CLOCK_DIVIDERS_CH3, addr 0x17	CH3_FIN_DIVIDER [15:12]	$f_{IN3} = f_{SENSOR3}$ / CH3_FIN_DIVIDER

(1) Channels 2 and 3 are only available for LDC1314

8.3.2 Multi-Channel and Single Channel Operation

The multi-channel package of the LDC enables the user to save board space and support flexible system design. For example, temperature drift can often cause a shift in component values, resulting in a shift in resonant frequency of the sensor. Using a 2nd sensor as a reference provides the capability to cancel out a temperature shift. When operated in multi-channel mode, the LDC sequentially samples the active channels. In single channel mode, the LDC samples a single channel, which is selectable. Table 3 shows the registers and values that are used to configure either multi-channel or single channel modes.

Table 3. Single and Multi-Channel Configuration Registers

MODE	REGISTER	FIELD [BIT(S)]	VALUE(1)
Single channel	CONFIG, addr 0x1A	ACTIVE_CHAN [15:14]	00 = chan 0 01 = chan 1 10 = chan 2 11 = chan 3
	MUX_CONFIG addr 0x1B	AUTOSCAN_EN [15]	0 = continuous conversion on a single channel (default)
Multi-channel	MUX_CONFIG addr 0x1B	AUTOSCAN_EN [15]	1 = continuous conversion on multiple channels
	MUX_CONFIG addr 0x1B	RR_SEQUENCE [14:13]	00 = Ch0, Ch 1 01 = Ch0, Ch 1, Ch 2 10 = Ch0, CH1, Ch2, Ch3

(1) Channels 2 and 3 are only available for LDC1314

The digitized sensor measurement for each channel (DATAx) represents the ratio of the sensor frequency to the reference frequency. The data outputs represent the 12 MSBs of a 16-bit result:

$$\mathrm{DATAx} / 2^{12} = f_{SENSORx} / f_{REFx} \quad (1)$$

The sensor frequency can be calculated from:

$$f_{\mathrm{sensorx}} = \frac{\mathrm{DATAx} * f_{\mathrm{REFx}}}{2^{12}} \quad (2)$$

Table 4 shows the registers that contain the fixed point sample values for each channel.

Table 4. LDC1314/1312 Sample Data Registers

CHANNEL[1]	REGISTER	FIELD NAME [BITS(S)]	VALUE
0	DATA_MSB_CH0, addr 0x00	DATA0 [11:0]	12 bits of the 16 bit result. 0x000 = under range 0xfff = over range
1	DATA_MSB_CH1, addr 0x02	DATA1 [11:0]	12 bits of the 16 bit result. 0x000 = under range 0xfff = over range
2	DATA_MSB_CH2, addr 0x04	DATA2 [11:0]	12 bits of the 16 bit result. 0x000 = under range 0xfff = over range
3	DATA_MSB_CH3, addr 0x06	DATA3 [11:0]	12 bits of the 16 bit result. 0x000 = under range 0xfff = over range

(1) Channels 2 and 3 available for LDC1314 only.

When the LDC sequences through the channels in multi-channel mode, the dwell time interval for each channel is the sum of 3 parts: sensor activation time + conversion time + channel switch delay.

The sensor activation time is the amount of settling time required for the sensor oscillation to stabilize, as shown in Figure 12. The settling wait time is programmable and should be set to a value that is long enough to allow stable oscillation. The settling wait time for channel x is given by:

$$t_{Sx} = (\mathrm{CHX\_SETTLECOUNT} \times 16)/f_{REFx} \quad (3)$$

Table 5 shows the registers and values for configuring the settling time for each channel.

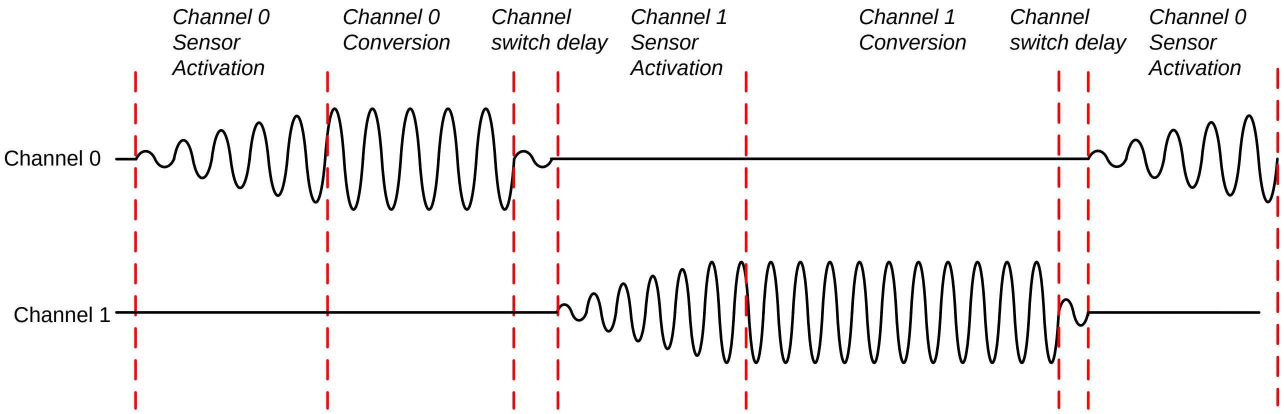


Figure 12. Multi-channel Mode Sequencing

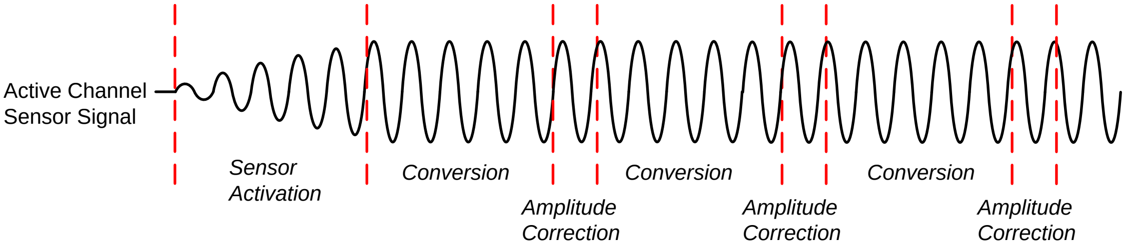


Figure 13. Single-channel Mode Sequencing

Table 5. Settling Time Register Configuration

CHANNEL [1]	REGISTER	FIELD	CONVERSION TIME [2]
0	SETTLECOUNT_CH0, addr 0x10	CH0_SETTLECOUNT (15:0)	$(CH0\_SETTLECOUNT*16)/f_{REF0}$
1	SETTLECOUNT_CH1, addr 0x11	CH1_SETTLECOUNT (15:0)	$(CH1\_SETTLECOUNT*16)/f_{REF1}$
2	SETTLECOUNT_CH2, addr 0x12	CH2_SETTLECOUNT (15:0)	$(CH2\_SETTLECOUNT*16)/f_{REF2}$
3	SETTLECOUNT_CH3, addr 0x13	CH3_SETTLECOUNT (15:0)	$(CH3\_SETTLECOUNT*16)/f_{REF3}$

(1) Channels 2 and 3 are available only in the LDC1314.
(2) f_{REFx} is the reference frequency configured for the channel.

The SETTLECOUNT for any channel x must satisfy:

$$CHx\_SETTLECOUNT \geq Q_{SENSORx} \times f_{REFx} / (16 \times f_{SENSORx})$$

where

- $f_{SENSORx}$ = Frequency of the Sensor on Channel x
- f_{REFx} = Reference frequency for Channel x
- $Q_{SENSORx}$ = Quality factor of the sensor on Channel x, where Q can be calculated by: (4)

$$Q = R_P \sqrt{\frac{C}{L}} \quad (5)$$

Round the result to the next highest integer (for example, if Equation 4 recommends a minimum value of 6.08, program the register to 7 or higher).

L, R_P and C values can be obtained by using Texas Instrument's WEBENCH® for the coil design.

The conversion time represents the number of reference clock cycles used to measure the sensor frequency. It is set by the CHx_RCOUNT register for the channel. The conversion time for any channel x is:

$$t_{Cx} = (CHx\_RCOUNT \times 16 + 4) / f_{REFx} \quad (6)$$

The reference count value must be chosen to support the required number of effective bits (ENOB). For details, refer to the application note Optimizing L Measurement Resolution for the LDC161x and LDC1101.

Table 6. Conversion Time Configuration Registers, Channels 0 - 3 [1]

CHANNEL	REGISTER	FIELD [BIT(S)]	CONVERSION TIME
0	RCOUNT_CH0, addr 0x08	CH0_RCOUNT (15:0)	$(CH0\_RCOUNT*16)/f_{REF0}$
1	RCOUNT_CH1, addr 0x09	CH1_RCOUNT (15:0)	$(CH1\_RCOUNT*16)/f_{REF1}$
2	RCOUNT_CH2, addr 0x0A	CH2_RCOUNT (15:0)	$(CH2\_RCOUNT*16)/f_{REF2}$
3	RCOUNT_CH3, addr 0x0B	CH3_RCOUNT (15:0)	$(CH3\_RCOUNT*16)/f_{REF3}$

(1) Channels 2 and 3 are available only for LDC1314.

The typical channel switch delay time between the end of conversion and the beginning of sensor activation of the subsequent channel is:

$$\text{Channel Switch Delay} = 692\text{ ns} + 5 / f_{ref} \quad (7)$$

The deterministic conversion time of the LDC allows data polling at a fixed interval. A data ready flag (DRDY) is also available for interrupt driven system designs (see the STATUS register description in *Register Maps*).

An offset value may be subtracted from each DATA value to compensate for a frequency offset or maximize the dynamic range of the sample data. The offset values should be < $f_{SENSORx\_MIN}$ / f_{REFx}. Otherwise, the offset might be so large that it masks the LSBs which are changing.

Table 7. Frequency Offset Registers

CHANNEL [(1)]	REGISTER	FIELD [BIT(S)]	VALUE
0	OFFSET_CH0, addr 0x0C	CH0_OFFSET [15:0]	$f_{OFFSET0}$ = CH0_OFFSET * ($f_{REF0}/2^{16}$)
1	OFFSET_CH1, addr 0x0D	CH1_OFFSET [15:0]	$f_{OFFSET1}$ = CH1_OFFSET * ($f_{REF1}/2^{16}$)
2	OFFSET_CH2, addr 0x0E	CH2_OFFSET [15:0]	$f_{OFFSET2}$ = CH2_OFFSET * ($f_{REF2}/2^{16}$)
3	OFFSET_CH3, addr 0x0F	CH3_OFFSET [15:0]	$f_{OFFSET3}$ = CH3_OFFSET * ($f_{REF3}/2^{16}$)

(1) Channels 2 and 3 are only available for LDC1314

Internally, the LDC measures with 16bits of resolution, while the conversion output word width is only 12bits. For systems in which the sensor signal variation is less than 25% of the full scale range, the LDC can report conversion results with higher resolution by setting the output gain. The output gain is applied to all device channels. An output gain can be used to apply a 2-bit, 3-bit, or 4-bit shift to the output code for all channels, allowing access to the 4LSBs of the original 16-bit result. The MSBs of the sample are shifted out when a gain is applied. Do not use the output gain if the MSBs of any active channel are toggling, as the MSBs for that channel will be lost when gain is applied.

Table 8. Output Gain Register

CHANNEL [(1)]	REGISTER	FIELD [BIT(S)]	VALUES	EFFECTIVE RESOLUTION (BITS)	OUTPUT RANGE
All	RESET_DEV, addr 0x1C	OUTPUT_GAIN [10:9]	00 (default): Gain =1 (0 bits shift)	12	100% full scale
			01: Gain = 4 (2 bits left shift)	14	25% full scale
			10: Gain = 8 (3 bits left shift)	15	12.5% full scale
			11 : Gain = 16 (4 bits left shift)	16	6.25% full scale

(1) Channels 2 and 3 are available for LDC1314 only.

Example: If the conversion result for a channel is 0x07A3, with OUTPUT_GAIN=0x0, the reported output code is 0x07A. If OUTPUT_GAIN is set to 0x3 in the same condition, then the reported output code is 0x7A3. The original 4 MSBs (0x0) are no longer accessible. Figure 14 shows the segments of the 16-bit sample that is reported for each possible gain setting.

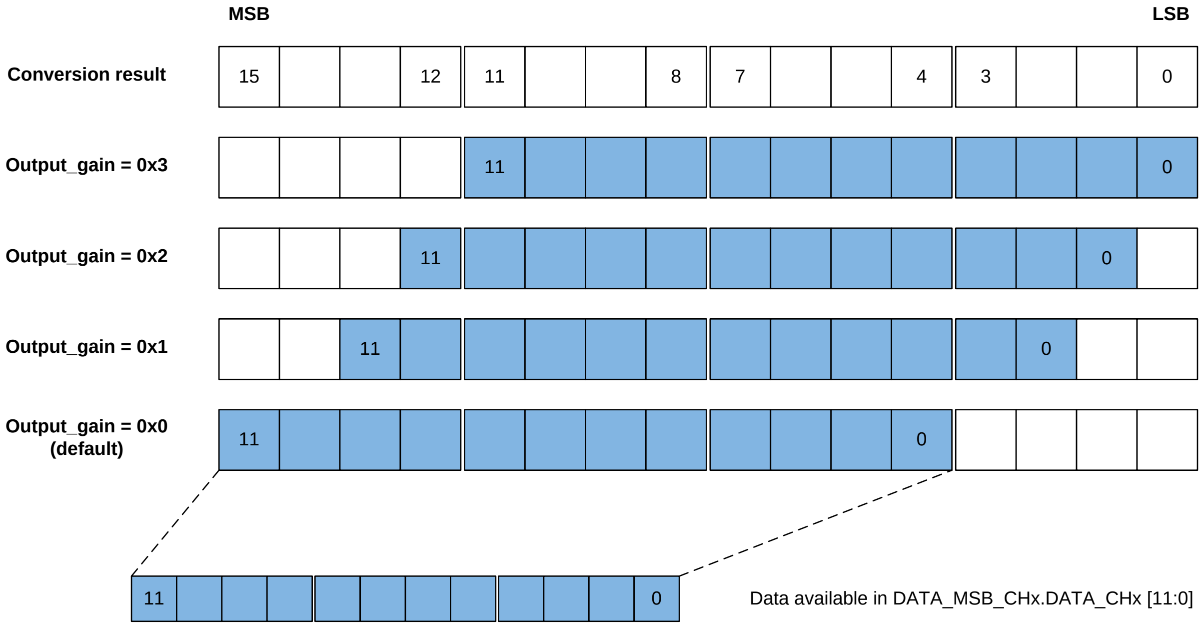


Figure 14. Conversion Data Output Gain

The sensor frequency can be determined by:

$$f_{SENSORx} = CHx\_FIN\_DIVIDER * f_{REFx} \left(\frac{DATAx}{2^{(12+OUTPUT\_GAIN)}} + \frac{CHx\_OFFSET}{2^{16}} \right)$$

where

- DATAx = Conversion result from the DATA_CHx register
- CHx_OFFSET = Offset value set in the OFFSET_CHx register
- OUTPUT_GAIN = output multiplication factor set in the RESET_DEVICE.OUTPUT_GAIN register (8)

8.3.3 Current Drive Control Registers

The registers listed in Table 9 are used to control the sensor drive current. The recommendations listed in the last column of Table 9 should be followed.

Auto-calibration mode is used to determine the optimal sensor drive current for a fixed sensor design. This mode should only be used during system prototyping.

The auto-amplitude correction attempts to maintain the sensor oscillation amplitude between 1.2V and 1.8V by adjusting the sensor drive current between conversions. When auto-amplitude correction is enabled, the output data may show non-monotonic behavior due to an adjustment in drive current. Auto-amplitude correction is only recommended for low-precision applications.

A high sensor current drive mode can be enabled to drive sensor coils with > 1.5mA on channel 0, only in single channel mode. This feature can be used when the sensor R_P is lower than 1kΩ. Set the HIGH_CURRENT_DRV register bit to b1 to enable this mode.

Table 9. Current Drive Control Registers

CHANNEL [1]	REGISTER	FIELD [BIT(S)]	VALUE
All	CONFIG, addr 0x1A	SENSOR_ACTIVATE_SEL [11]	Sets current drive for sensor activation. Recommended value is b0 (Full Current mode).
		RP_OVERRIDE_EN [12]	Set to b1 for normal operation (RP over ride enabled)
		AUTO_AMP_DIS [10]	Disables Automatic amplitude correction. Set to b1 for normal operation (disabled)
0	CONFIG, addr 0x1A	HIGH_CURRENT_DRV [6]	b0 = normal current drive (1.5 mA) b1 = Increased current drive (> 1.5 mA) for Ch 0 in single channel mode only. Cannot be used in multi-channel mode.
0	DRIVE_CURRENT_CH0, addr 0x1E	CH0_IDRIVE [15:11]	Drive current used during the settling and conversion time for Ch. 0 (auto-amplitude correction must be disabled and RP over ride=1)
		CH0_INIT_IDRIVE [10:6]	Initial drive current stored during auto-calibration. Not used for normal operation.
1	DRIVE_CURRENT_CH1, addr 0x1F	CH1_IDRIVE [15:11]	Drive current used during the settling and conversion time for Ch. 1 (auto-amplitude correction must be disabled and RP over ride=1)
		CH1_INIT_IDRIVE [10:6]	Initial drive current stored during auto-calibration. Not used for normal operation.
2	DRIVE_CURRENT_CH2, addr 0x20	CH2_IDRIVE [15:11]	Drive current used during the settling and conversion time for Ch. 2 (auto-amplitude correction must be disabled and RP over ride=1)
		CH2_INIT_IDRIVE [10:6]	Initial drive current stored during auto-calibration. Not used for normal operation.

---

(1) Channels 2 and 3 are available for LDC1314 only.

Table 9. Current Drive Control Registers (continued)

CHANNEL [1]	REGISTER	FIELD [BIT(S)]	VALUE
3	DRIVE_CURRENT_CH3, addr 0x21	CH3_IDRIVE [15:11]	Drive current used during the settling and conversion time for Ch. 3 (auto-amplitude correction must be disabled and RP override=1)
		CH3_INIT_IDRIVE [10:6]	Initial drive current stored during auto-calibration. Not used for normal operation.

If the R_P value of the sensor attached to channel x is known, Table 10 can be used to select the 5-bit value to be programmed into the CHx_IDRIVE field for the channel. If the measured R_P (at maximum spacing between the sensor and the target) falls between two of the table values, use the current drive value associated with the lower R_P from Table 10. All channels that use an identical sensor/target configuration should use the same IDRIVE value.

Table 10. CHx_IDRIVE Values for Maximum Measured R_P.

MEASURED R_P (kΩ)	CHx_IDRIVE REGISTER FIELD VALUE, BINARY (BITS [15:11])	NOMINAL CURRENT (µA)
90.0	b00000	16
77.6	b00001	18
66.9	b00010	20
57.6	b00011	23
49.7	b00100	28
42.8	b00101	32
36.9	b00110	40
31.8	b00111	46
27.4	b01000	52
23.3	b01001	59
20.4	b01010	72
17.6	b01011	82
15.1	b01100	95
13.0	b01101	110
11.2	b01110	127
9.7	b01111	146
8.4	b10000	169
7.2	b10001	195
6.2	b10010	212
5.4	b10011	244
4.6	b10100	297
4.0	b10101	342
3.4	b10110	424
3.0	b10111	489
2.5	b11000	551
2.2	b11001	635
1.9	b11010	763
1.6	b11011	880
1.4	b11100	1017
1.2	b11101	1173
1.0	b11110	1355
0.9	b11111	1563

If the R_P is not known, the following steps for auto-calibration can be used to configure the needed drive current, either during system prototyping, or during normal startup if feasible:

1. Set target at the maximum planned operating distance from the sensor.
2. Place the device into SLEEP mode by setting CONFIG.SLEEP_MODE_EN to b0.
3. Program the desired values of SETTLECOUNT and RCOUNT values for the channel.
4. Enable auto-calibration by setting RP_OVERDRIVE_EN to b0.
5. Take the device out of SLEEP mode by setting CONFIG.SLEEP_MODE_EN to b1.
6. Allow the device to perform at least one measurement, with the target stable (fixed) at the maximum operating range.
7. Read the channel current drive value from the appropriate DRIVE_CURRENT_CHx register (addresses 0x1e, 0x1f, 0x20, or 0x21), in the CHx_INIT_DRIVE field (bits 10:6). Save this value.
8. During startup for normal operating mode, write the value saved from the CHx_INIT_DRIVE bit field into the Chx_IDRIVE bit field (bits 15:11).
9. During normal operating mode, the RP_OVERRIDE_EN must set to b1 to force the fixed current drive.

If the current drive results in the oscillation amplitude greater than 1.8V, the internal ESD clamping circuit will become active. This may cause the sensor frequency to shift so that the output values no longer represent a valid system state. If the current drive is set at a lower value, the SNR performance of the system will decrease, and at near zero target range, oscillations may completely stop, and the output sample values will be all zeroes.

8.3.4 Device Status Registers

The registers listed in Table 11 may be used to read device status.

Table 11. Status Registers

CHANNEL [(1)]	REGISTER	FIELDS [BIT(S)]	VALUES
All	STATUS, addr 0x18	12 fields are available that contain various status bits [15:0]	Refer to Register Maps section for a description of the individual status bits.
All	ERROR_CONFIG, addr 0x19	12 fields are available that are used to configure error reporting [15:0]	Refer to Register Maps section for a description of the individual error configuration bits.

(1) Channels 2 and 3 are available for LDC1314 only.

See the STATUS and ERROR_CONFIG register description in the Register Map section. These registers can be configured to trigger an interrupt on the INTB pin for certain events. The following conditions must be met:

1. The error or status register must be unmasked by enabling the appropriate register bit in the ERROR_CONFIG register
2. The INTB function must be enabled by setting CONFIG.INTB_DIS to 0

When a bit field in the STATUS register is set, the entire STATUS register content is held until read or until the DATA_CHx register is read. Reading also de-asserts INTB.

Interrupts are cleared by one of the following events:

1. Entering Sleep Mode
2. Power-on reset (POR)
3. Device enters Shutdown Mode (SD is asserted)
4. S/W reset
5. I2C read of the STATUS register: Reading the STATUS register will clear any error status bit set in STATUS along with the ERR_CHAN field and de-assert INTB

Setting register CONFIG.INTB_DIS to b1 disables the INTB function and holds the INTB pin high.

8.3.5 Input Deglitch Filter

The input deglitch filter suppresses EMI and ringing above the sensor frequency. It does not impact the conversion result as long as its bandwidth is configured to be above the maximum sensor frequency. The input deglitch filter can be configured in MUX_CONFIG.DEGLITCH register field as shown in Table 12. For optimal performance, TI recommends to select the lowest setting that exceeds the sensor oscillation frequency. For example, if the maximum sensor frequency is 2.0 MHz, choose MUX_CONFIG.DEGLITCH = b100 (3.3 MHz).

Table 12. Input deglitch filter register

CHANNEL [(1)]	MUX_CONFIG.DEGLITCH REGISTER VALUE	DEGLITCH FREQEUNCY
ALL	001	1 MHz
ALL	100	3.3 MHz
ALL	101	10 MHz
ALL	011	33 MHz

(1) Channels 2 and 3 are available for LDC1314 only.

8.4 Device Functional Modes

8.4.1 Startup Mode

When the LDC powers up, it enters into Sleep Mode and will wait for configuration. Once the device is configured, exit Sleep Mode by setting CONFIG.SLEEP_MODE_EN to b0.

TI recommends to configure the LDC while in Sleep Mode. If a setting on the LDC needs to be changed, return the device to Sleep Mode, change the appropriate register, and then exit Sleep Mode.

8.4.2 Normal (Conversion) Mode

When operating in the normal (conversion) mode, the LDC is periodically sampling the frequency of the sensor(s) and generating sample outputs for the active channel(s).

8.4.3 Sleep Mode

Sleep Mode is entered by setting the CONFIG.SLEEP_MODE_EN register field to 1. While in this mode, the device configuration is maintained. To exit Sleep Mode, set the CONFIG.SLEEP_MODE_EN register field to 0. After setting CONFIG.SLEEP_MODE_EN to b0, sensor activation for the first conversion will begin after 16,384 f_{INT} clock cycles. While in Sleep Mode the I2C interface is functional so that register reads and writes can be performed. While in Sleep Mode, no conversions are performed. In addition, entering Sleep Mode will clear conversion results, any error condition and de-assert the INTB pin.

8.4.4 Shutdown Mode

When the SD pin is set to high, the LDC will enter Shutdown Mode. Shutdown Mode is the lowest power state. To exit Shutdown Mode, set the SD pin to low. Entering Shutdown Mode will return all registers to their default state.

While in Shutdown Mode, no conversions are performed. In addition, entering Shutdown Mode will clear any error condition and de-assert the INTB pin. While the device is in Shutdown Mode, is not possible to read to or write from the device via the I2C interface.

8.4.4.1 Reset

The LDC can be reset by writing to RESET_DEV.RESET_DEV. Any active conversion will stop and all register values will return to their default value. This register bit will always return 0b when read.

8.5 Programming

The LDC device uses an I2C interface to access control and data registers.

8.5.1 I2C Interface Specifications

The LDC uses an extended start sequence with I2C for register access. The maximum speed of the I2C interface is 400kbit/s. This sequence follows the standard I2C 7bit slave address followed by an 8bit pointer register byte to set the register address. When the ADDR pin is set low, the LDC I2C address is 0x2A; when the ADDR pin is set high, the LDC I2C address is 0x2B. The ADDR pin must not change state after the LDC exits Shutdown Mode.

Programming (continued)

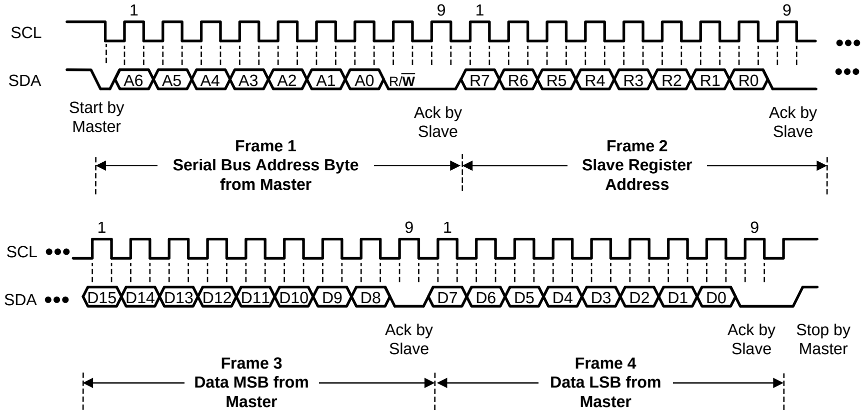


Figure 15. I2C Write Register Sequence

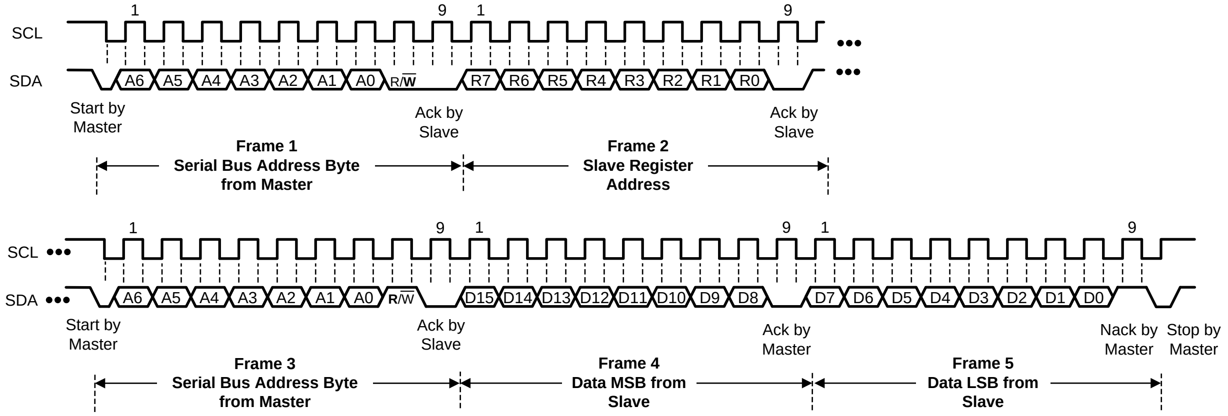


Figure 16. I2C Read Register Sequence

8.6 Register Maps

8.6.1 Register List

Fields indicated with Reserved must be written only with indicated values, otherwise improper device operation may occur. The R/W column indicates the Read-Write status of the corresponding field. A 'R/W' entry indicates read and write capability, a 'R' indicates read-only, and a 'W' indicates write-only.

Figure 17. Register List

ADDRESS	NAME	DEFAULT VALUE	DESCRIPTION
0x00	DATA_CH0	0x0000	Channel 0 Conversion Result and Error Status
0x02	DATA_CH1	0x0000	Channel 1 Conversion Result and Error Status
0x04	DATA_CH2	0x0000	Channel 2 Conversion Result and Error Status **(LDC1314 only)**
0x06	DATA_CH3	0x0000	Channel 3 Conversion Result and Error Status **(LDC1314 only)**
0x08	RCOUNT_CH0	0x0080	Reference Count setting for Channel 0
0x09	RCOUNT_CH1	0x0080	Reference Count setting for Channel 1
0x0A	RCOUNT_CH2	0x0080	Reference Count setting for Channel 2. **(LDC1314 only)**
0x0B	RCOUNT_CH3	0x0080	Reference Count setting for Channel 3.**(LDC1314 only)**
0x0C	OFFSET_CH0	0x0000	Offset value for Channel 0
0x0D	OFFSET_CH1	0x0000	Offset value for Channel 1
0x0E	OFFSET_CH2	0x0000	Offset value for Channel 2 **(LDC1314 only)**
0x0F	OFFSET_CH3	0x0000	Offset value for Channel 3 **(LDC1314 only)**
0x10	SETTLECOUNT_CH0	0x0000	Channel 0 Settling Reference Count
0x11	SETTLECOUNT_CH1	0x0000	Channel 1 Settling Reference Count
0x12	SETTLECOUNT_CH2	0x0000	Channel 2 Settling Reference Count **(LDC1314 only)**
0x13	SETTLECOUNT_CH3	0x0000	Channel 3 Settling Reference Count **(LDC1314 only)**
0x14	CLOCK_DIVIDERS_CH0	0x0000	Reference and Sensor Divider settings for Channel 0
0x15	CLOCK_DIVIDERS_CH1	0x0000	Reference and Sensor Divider settings for Channel 1
0x16	CLOCK_DIVIDERS_CH2	0x0000	Reference and Sensor Divider settings for Channel 2 **(LDC1314 only)**
0x17	CLOCK_DIVIDERS_CH3	0x0000	Reference and Sensor Divider settings for Channel 3 **(LDC1314 only)**
0x18	STATUS	0x0000	Device Status Report
0x19	ERROR_CONFIG	0x0000	Error Reporting Configuration
0x1A	CONFIG	0x2801	Conversion Configuration
0x1B	MUX_CONFIG	0x020F	Channel Multiplexing Configuration
0x1C	RESET_DEV	0x0000	Reset Device
0x1E	DRIVE_CURRENT_CH0	0x0000	Channel 0 sensor current drive configuration
0x1F	DRIVE_CURRENT_CH1	0x0000	Channel 1 sensor current drive configuration
0x20	DRIVE_CURRENT_CH2	0x0000	Channel 2 sensor current drive configuration **(LDC1314 only)**
0x21	DRIVE_CURRENT_CH3	0x0000	Channel 3 sensor current drive configuration **(LDC1314 only)**
0x7E	MANUFACTURER_ID	0x5449	Manufacturer ID
0x7F	DEVICE_ID	0x3054	Device ID

8.6.2 Address 0x00, DATA_CH0

Figure 18. Address 0x00, DATA_CH0

15	14	13	12	11	10	9	8
CH0_ERR_UR	CH0_ERR_OR	CH0_ERR_WD	CH0_ERR_AE	DATA0[11:0]			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DATA0[11:0]							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. Address 0x00, DATA_CH0 Field Descriptions

Bit	Field	Type	Reset	Description
15	CH0_ERR_UR	R	0	Channel 0 Conversion Under-range Error Flag. Cleared by reading the bit.
14	CH0_ERR_OR	R	0	Channel 0 Conversion Over-range Error Flag. Cleared by reading the bit.
13	CH0_ERR_WD	R	0	Channel 0 Conversion Watchdog Timeout Error Flag. Cleared by reading the bit.
12	CH0_ERR_AE	R	0	Channel 0 Conversion Watchdog Timeout Error Flag. Cleared by reading the bit.
11:0	DATA0[11:0]	R	0000 0000 0000	Channel 0 Conversion Result

8.6.3 Address 0x02, DATA_CH1

Figure 19. Address 0x02, DATA_CH1

15	14	13	12	11	10	9	8
CH1_ERR_UR	CH1_ERR_OR	CH1_ERR_WD	CH1_ERR_AE	DATA1[11:0]			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DATA1[11:0]							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. Address 0x02, DATA_CH1 Field Descriptions

Bit	Field	Type	Reset	Description
15	CH1_ERR_UR	R	0	Channel 1 Conversion Under-range Error Flag. Cleared by reading the bit.
14	CH1_ERR_OR	R	0	Channel 1 Conversion Over-range Error Flag. Cleared by reading the bit.
13	CH1_ERR_WD	R	0	Channel 1 Conversion Watchdog Timeout Error Flag. Cleared by reading the bit.
12	CH1_ERR_AE	R	0	Channel 1 Conversion Watchdog Timeout Error Flag. Cleared by reading the bit.
11:0	DATA1[11:0]	R	0000 0000 0000	Channel 1 Conversion Result

8.6.4 Address 0x04, DATA_CH2 (LDC1314 only)

Figure 20. Address 0x04, DATA_CH2

15	14	13	12	11	10	9	8
CH2_ERR_UR	CH2_ERR_OR	CH2_ERR_WD	CH2_ERR_AE	DATA2[11:0]			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DATA2[11:0]							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. Address 0x04, DATA_CH2 Field Descriptions

Bit	Field	Type	Reset	Description
15	CH2_ERR_UR	R	0	Channel 2 Conversion Under-range Error Flag. Cleared by reading the bit.
14	CH2_ERR_OR	R	0	Channel 2 Conversion Over-range Error Flag. Cleared by reading the bit.
13	CH2_ERR_WD	R	0	Channel 2 Conversion Watchdog Timeout Error Flag. Cleared by reading the bit.
12	CH2_ERR_AE	R	0	Channel 2 Conversion Watchdog Timeout Error Flag. Cleared by reading the bit.
11:0	DATA2[11:0]	R	0000 0000 0000	Channel 2 Conversion Result

8.6.5 Address 0x06, DATA_CH3 (LDC1314 only)

Figure 21. Address 0x06, DATA_CH3

15	14	13	12	11	10	9	8
CH3_ERR_UR	CH3_ERR_OR	CH3_ERR_WD	CH3_ERR_AE	DATA3[11:0]			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DATA3[11:0]							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. Address 0x06, DATA_CH3 Field Descriptions

Bit	Field	Type	Reset	Description
15	CH3_ERR_UR	R	0	Channel 3 Conversion Under-range Error Flag. Cleared by reading the bit.
14	CH3_ERR_OR	R	0	Channel 3 Conversion Over-range Error Flag. Cleared by reading the bit.
13	CH3_ERR_WD	R	0	Channel 3 Conversion Watchdog Timeout Error Flag. Cleared by reading the bit.
12	CH3_ERR_AE	R	0	Channel 3 Conversion Watchdog Timeout Error Flag. Cleared by reading the bit.
11:0	DATA3[11:0]	R	0000 0000 0000	Channel 3 Conversion Result

8.6.6 Address 0x08, RCOUNT_CH0

Figure 22. Address 0x08, RCOUNT_CH0

15	14	13	12	11	10	9	8
CH0_RCOUNT							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CH0_RCOUNT							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. Address 0x08, RCOUNT_CH0 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CH0_RCOUNT	R/W	0000 0000 1000 0000	Channel 0 Reference Count Conversion Interval Time 0x0000-0x0004: Reserved 0x0005-0xFFFF: Conversion Time (t_{C0}) = ($CH0\_RCOUNT^{\times}16$)/f_{REF0}

8.6.7 Address 0x09, RCOUNT_CH1

Figure 23. Address 0x09, RCOUNT_CH1

15	14	13	12	11	10	9	8
CH1_RCOUNT							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CH1_RCOUNT							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. Address 0x09, RCOUNT_CH1 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CH1_RCOUNT	R/W	0000 0000 1000 0000	Channel 1 Reference Count Conversion Interval Time 0x0000-0x0004: Reserved 0x0005-0xFFFF: Conversion Time (t_{C1})= ($CH1\_RCOUNT^{\times}16$)/f_{REF1}

8.6.8 Address 0x0A, RCOUNT_CH2 (LDC1314 only)

Figure 24. Address 0x0A, RCOUNT_CH2

15	14	13	12	11	10	9	8
CH2_RCOUNT							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CH2_RCOUNT							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. Address 0x0A, RCOUNT_CH2 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CH2_RCOUNT	R/W	0000 0000 1000 0000	Channel 2 Reference Count Conversion Interval Time 0x0000-0x0004: Reserved 0x0005-0xFFFF: Conversion Time (t_{C2})= ($CH2\_RCOUNT^{\times}16$)/f_{REF2}

8.6.9 Address 0x0B, RCOUNT_CH3 (LDC1314 only)

Figure 25. Address 0x0B, RCOUNT_CH3

15	14	13	12	11	10	9	8
CH3_RCOUNT							
7	6	5	4	3	2	1	0
CH3_RCOUNT							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 20. Address 0x0B, RCOUNT_CH3 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CH3_RCOUNT	R/W	0000 0000 1000 0000	Channel 3 Reference Count Conversion Interval Time 0x0000-0x0004: Reserved 0x0005-0xFFFF: Conversion Time (t_{C3})= (CH3_RCOUNT×16)/f_{REF3}

8.6.10 Address 0x0C, OFFSET_CH0

Figure 26. Address 0x0C, CH0_OFFSET

15	14	13	12	11	10	9	8
CH0_OFFSET							
7	6	5	4	3	2	1	0
CH0_OFFSET							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21. CH0_OFFSET Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CH0_OFFSET	R/W	0000 0000 0000 0000	Channel 0 Conversion Offset. f_{OFFSET_0} = (CH0_OFFSET/2^{16})*f_{REF0}

8.6.11 Address 0x0D, OFFSET_CH1

Figure 27. Address 0x0D, OFFSET_CH1

15	14	13	12	11	10	9	8
CH1_OFFSET							
7	6	5	4	3	2	1	0
CH1_OFFSET							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 22. Address 0x0D, OFFSET_CH1 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CH1_OFFSET	R/W	0000 0000 0000 0000	Channel 1 Conversion Offset. f_{OFFSET_1} = (CH1_OFFSET/2^{16})*f_{REF1}

8.6.12 Address 0x0E, OFFSET_CH2 (LDC1314 only)

Figure 28. Address 0x0E, OFFSET_CH2

15	14	13	12	11	10	9	8
CH2_OFFSET							
7	6	5	4	3	2	1	0
CH2_OFFSET							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 23. Address 0x0E, OFFSET_CH2 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CH2_OFFSET	R/W	0000 0000 0000 0000	Channel 2 Conversion Offset. f_{OFFSET_2} = $(CH2\_OFFSET/2^{16})*f_{REF2}$

8.6.13 Address 0x0F, OFFSET_CH3 (LDC1314 only)

Figure 29. Address 0x0F, OFFSET_CH3

15	14	13	12	11	10	9	8
CH3_OFFSET							
7	6	5	4	3	2	1	0
CH3_OFFSET							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. Address 0x0F, OFFSET_CH3 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CH3_OFFSET	R/W	0000 0000 0000 0000	Channel 3 Conversion Offset. f_{OFFSET_3} = $(CH3\_OFFSET/2^{16})*f_{REF3}$

8.6.14 Address 0x10, SETTLECOUNT_CH0

Figure 30. Address 0x10, SETTLECOUNT_CH0

15	14	13	12	11	10	9	8
CH0_SETTLECOUNT							
7	6	5	4	3	2	1	0
CH0_SETTLECOUNT							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 25. Address 0x11, SETTLECOUNT_CH0 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CH0_SETTLECOUNT	R/W	0000 0000 0000 0000	Channel 0 Conversion Settling The LDC will use this settling time to allow the LC sensor to stabilize before initiation of a conversion on Channel 0. If the amplitude has not settled prior to the conversion start, an Amplitude error will be generated if reporting of this type of error is enabled. 0x0000: Settle Time (t_{S0})= 32 ÷ f_{REF0} 0x0001: Settle Time (t_{S0})= 32 ÷ f_{REF0} 0x0002- 0xFFFF: Settle Time (t_{S0})= (CH0_SETTLECOUNT×16) ÷ f_{REF0}

8.6.15 Address 0x11, SETTLECOUNT_CH1

Figure 31. Address 0x11, SETTLECOUNT_CH1

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CH1_SETTLECOUNT</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CH1_SETTLECOUNT</td></tr>
<tr><td colspan="8"></td></tr>
</table>

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 26. Address 0x12, SETTLECOUNT_CH1 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CH1_SETTLECOUNT	R/W	0000 0000 0000 0000	Channel 1 Conversion Settling The LDC will use this settling time to allow the LC sensor to stabilize before initiation of a conversion on a Channel 1. If the amplitude has not settled prior to the conversion start, an Amplitude error will be generated if reporting of this type of error is enabled. 0x0000: Settle Time (t_{S1})= 32 ÷ f_{REF1} 0x0001: Settle Time (t_{S1})= 32 ÷ f_{REF1} 0x0002- 0xFFFF: Settle Time (t_{S1})= (CH1_SETTLECOUNT×16) ÷ f_{REF1}

8.6.16 Address 0x12, SETTLECOUNT_CH2 (LDC1314 only)

Figure 32. Address 0x12, SETTLECOUNT_CH2

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">CH2_SETTLECOUNT</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CH2_SETTLECOUNT</td></tr>
<tr><td colspan="8"></td></tr>
</table>

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 27. Address 0x12, SETTLECOUNT_CH2 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CH2_SETTLECOUNT	R/W	0000 0000 0000 0000	Channel 2 Conversion Settling The LDC will use this settling time to allow the LC sensor to stabilize before initiation of a conversion on Channel 2. If the amplitude has not settled prior to the conversion start, an Amplitude error will be generated if reporting of this type of error is enabled. 0x0000: Settle Time (t_{S2})= 32 ÷ f_{REF2} 0x0001: Settle Time (t_{S2})= 32 ÷ f_{REF2} 0x0002- 0xFFFF: Settle Time (t_{S2})= (CH2_SETTLECOUNT×16) ÷ f_{REF2}

8.6.17 Address 0x13, SETTLECOUNT_CH3 (LDC1314 only)

Figure 33. Address 0x13, SETTLECOUNT_CH3

15	14	13	12	11	10	9	8
CH3_SETTLECOUNT							

7	6	5	4	3	2	1	0
CH3_SETTLECOUNT							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 28. Address 0x13, SETTLECOUNT_CH3 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CH3_SETTLECOUNT	R/W	0000 0000 0000 0000	Channel 3 Conversion Settling The LDC will use this settling time to allow the LC sensor to stabilize before initiation of a conversion on Channel 3. If the amplitude has not settled prior to the conversion start, an Amplitude error will be generated if reporting of this type of error is enabled 0x0000: Settle Time (t_{S3})= 32 ÷ f_{REF3} 0x0001: Settle Time (t_{S3})= 32 ÷ f_{REF3} 0x0002- 0xFFFF: Settle Time (t_{S3})= (CH3_SETTLECOUNT^{x}16) ÷ f_{REF3}

8.6.18 Address 0x14, CLOCK_DIVIDERS_CH0

Figure 34. Address 0x14, CLOCK_DIVIDERS_CH0

15	14	13	12	11	10	9	8
CH0_FIN_DIVIDER				RESERVED		CH0_FREF_DIVIDER	

7	6	5	4	3	2	1	0
CH0_FREF_DIVIDER							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 29. Address 0x14, CLOCK_DIVIDERS_CH0 Field Descriptions

Bit	Field	Type	Reset	Description
15:12	CH0_FIN_DIVIDER	R/W	0000	Channel 0 Input Divider Sets the divider for Channel 0 input. Must be set to ≥2 if the Sensor frequency is ≥ 8.75MHz b0000: Reserved. Do not use. CH0_FIN_DIVIDER≥b0001: f_{in0} = $f_{SENSOR0}$/CH0_FIN_DIVIDER
11:10	RESERVED	R/W	00	Reserved. Set to b00.
9:0	CH0_FREF_DIVIDER	R/W	00 0000 0000	Channel 0 Reference Divider Sets the divider for Channel 0 reference. Use this to scale the maximum conversion frequency. b00’0000’0000: Reserved. Do not use. CH0_FREF_DIVIDER≥b00’0000’0001: f_{REF0} = f_{CLK}/CH0_FREF_DIVIDER

8.6.19 Address 0x15, CLOCK_DIVIDERS_CH1

Figure 35. Address 0x15, CLOCK_DIVIDERS_CH1

15	14	13	12	11	10	9	8
CH1_FIN_DIVIDER				RESERVED		CH1_FREF_DIVIDER	
7	6	5	4	3	2	1	0
CH1_FREF_DIVIDER							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 30. Address 0x15, CLOCK_DIVIDERS_CH1 Field Descriptions

Bit	Field	Type	Reset	Description
15:12	CH1_FIN_DIVIDER	R/W	0000	Channel 1 Input Divider. Sets the divider for Channel 1 input. Used when the Sensor frequency is greater than the maximum F_{IN}. b0000: Reserved. Do not use. CH1_FIN_DIVIDER≥b0001: $f_{in1} = f_{SENSOR1}$/CH1_FIN_DIVIDER
11:10	RESERVED	R/W	00	Reserved. Set to b00.
9:0	CH1_FREF_DIVIDER	R/W	00 0000 0000	Channel 1 Reference Divider. Sets the divider for Channel 1 reference. Use this to scale the maximum conversion frequency. b00’0000’0000: Reserved. Do not use. CH1_FREF_DIVIDER≥ b00’0000’0001: $f_{REF1} = f_{CLK}$/CH1_FREF_DIVIDER

8.6.20 Address 0x16, CLOCK_DIVIDERS_CH2 (LDC1314 only)

Figure 36. Address 0x16, CLOCK_DIVIDERS_CH2

15	14	13	12	11	10	9	8
CH2_FIN_DIVIDER				RESERVED		CH2_FREF_DIVIDER	
7	6	5	4	3	2	1	0
CH2_FREF_DIVIDER							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 31. Address 0x16, CLOCK_DIVIDERS_CH2 Field Descriptions

Bit	Field	Type	Reset	Description
15:12	CH2_FIN_DIVIDER	R/W	0000	Channel 2 Input Divider. Sets the divider for Channel 2 input. Must be set to ≥2 if the Sensor frequency is ≥ 8.75MHz. b0000: Reserved. Do not use. CH2_FIN_DIVIDER≥b0001: $f_{IN2} = f_{SENSOR2}$/CH2_FIN_DIVIDER
11:10	RESERVED	R/W	00	Reserved. Set to b00
9:0	CH2_FREF_DIVIDER	R/W	00 0000 0000	Channel 2 Reference Divider. Sets the divider for Channel 2 reference. Use this to scale the maximum conversion frequency. b00’0000’0000: Reserved. Do not use. CH2_FREF_DIVIDER ≥ b00’0000’0001: $f_{REF2} = f_{CLK}$/CH2_FREF_DIVIDER

8.6.21 Address 0x17, CLOCK_DIVIDERS_CH3 (LDC1314 only)

Figure 37. Address 0x17, CLOCK_DIVIDERS_CH3

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">CH3_FIN_DIVIDER</td><td colspan="2">RESERVED</td><td colspan="2">CH3_FREF_DIVIDER</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">CH3_FREF_DIVIDER</td></tr>
<tr><td colspan="8"></td></tr>
</table>

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 32. Address 0x17, CLOCK_DIVIDERS_CH3

Bit	Field	Type	Reset	Description
15:12	CH3_FIN_DIVIDER	R/W	0000	Channel 3 Input Divider. Sets the divider for Channel 3 input. Must be set to ≥2 if the Sensor frequency is ≥ 8.75MHz. b0000: Reserved. Do not use. CH3_FIN_DIVIDER≥b0001: $f_{IN3} = f_{SENSOR3}$/CH3_FIN_DIVIDER
11:10	RESERVED	R/W	00	Reserved. Set to b00
9:0	CH3_FREF_DIVIDER	R/W	00 0000 0000	Channel 3 Reference Divider. Sets the divider for Channel 3 reference. Use this to scale the maximum conversion frequency. b00’0000’0000: reserved CH3_FREF_DIVIDER ≥ b00’0000’0001: f_{REF3} = f_{CLK}/CH3_FREF_DIVIDER

8.6.22 Address 0x18, STATUS

Figure 38. Address 0x18, STATUS

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">ERR_CHAN</td><td>ERR_UR</td><td>ERR_OR</td><td>ERR_WD</td><td>ERR_AHE</td><td>ERR_ALE</td><td>ERR_ZC</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>DRDY</td><td colspan="2">RESERVED</td><td>CH0_UNREADCONV</td><td>CH1_ UNREADCONV</td><td>CH2_ UNREADCONV</td><td>CH3_ UNREADCONV</td></tr>
<tr><td colspan="8"></td></tr>
</table>

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 33. Address 0x18, STATUS Field Descriptions

Bit	Field	Type	Reset	Description
15:14	ERR_CHAN	R	00	Error Channel Indicates which channel has generated a Flag or Error. Once flagged, any reported error is latched and maintained until either the STATUS register or the DATA_CHx register corresponding to the Error Channel is read. b00: Channel 0 is source of flag or error. b01: Channel 1 is source of flag or error. b10: Channel 2 is source of flag or error (LDC1314 only). b11: Channel 3 is source of flag or error (LDC1314 only).
13	ERR_UR	R	0	Conversion Under-range Error b0: No Conversion Under-range error was recorded since the last read of the STATUS register. b1: An active channel has generated a Conversion Under-range error. Refer to STATUS.ERR_CHAN field to determine which channel is the source of this error.
12	ERR_OR	R	0	Conversion Over-range Error. b0: No Conversion Over-range error was recorded since the last read of the STATUS register. b1: An active channel has generated a Conversion Over-range error. Refer to STATUS.ERR_CHAN field to determine which channel is the source of this error.

Table 33. Address 0x18, STATUS Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	ERR_WD	R	0	Watchdog Timeout Error b0: No Watchdog Timeout error was recorded since the last read of the STATUS register. b1: An active channel has generated a Watchdog Timeout error. Refer to STATUS.ERR_CHAN field to determine which channel is the source of this error.
10	ERR_AHE	R	0	Amplitude High Error b0: No Amplitude High error was recorded since the last read of the STATUS register. b1: An active channel has generated an Amplitude High error. Refer to STATUS.ERR_CHAN field to determine which channel is the source of this error.
9	ERR_ALE	R	0	Amplitude Low Error b0: No Amplitude Low error was recorded since the last read of the STATUS register. b1: An active channel has generated an Amplitude Low error. Refer to STATUS.ERR_CHAN field to determine which channel is the source of this error.
8	ERR_ZC	R	0	Zero Count Error b0: No Zero Count error was recorded since the last read of the STATUS register. b1: An active channel has generated a Zero Count error. Refer to STATUS.ERR_CHAN field to determine which channel is the source of this error.
6	DRDY	R	0	Data Ready Flag. b0: No new conversion result was recorded in the STATUS register. b1: A new conversion result is ready. When in Single Channel Conversion, this indicates a single conversion is available. When in sequential mode, this indicates that a new conversion result for all active channels is now available.
3	CH0_UNREADCONV	R	0	Channel 0 Unread Conversion b0: No unread conversion is present for Channel 0. b1: An unread conversion is present for Channel 0. Read Register DATA_CH0 to retrieve conversion results.
2	CH1_ UNREADCONV	R	0	Channel 1 Unread Conversion b0: No unread conversion is present for Channel 1. b1: An unread conversion is present for Channel 1. Read Register DATA_CH1 to retrieve conversion results.
1	CH2_ UNREADCONV	R	0	Channel 2 Unread Conversion b0: No unread conversion is present for Channel 2. b1: An unread conversion is present for Channel 2. Read Register DATA_CH2 to retrieve conversion results (LDC1314 only)
0	CH3_ UNREADCONV	R	0	Channel 3 Unread Conversion b0: No unread conversion is present for Channel 3. b1: An unread conversion is present for Channel 3. Read Register DATA_CH3 to retrieve conversion results (LDC1314 only)

8.6.23 Address 0x19, ERROR_CONFIG

Figure 39. Address 0x19, ERROR_CONFIG

15	14	13	12	11	10	9	8
UR_ERR2OUT	OR_ERR2OUT	WD_ ERR2OUT	AH_ERR2OUT	AL_ERR2OUT	RESERVED		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
UR_ERR2INT	OR_ERR2INT	WD_ERR2INT	AH_ERR2INT	AL_ERR2INT	ZC_ERR2INT	Reserved	DRDY_2INT

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 34. Address 0x19, ERROR_CONFIG

Bit	Field	Type	Reset	Description
15	UR_ERR2OUT	R/W	0	Under-range Error to Output Register b0: Do not report Under-range errors in the DATA_CHx registers. b1: Report Under-range errors in the DATA_CHx.CHx_ERR_UR register field corresponding to the channel that generated the error.
14	OR_ERR2OUT	R/W	0	Over-range Error to Output Register b0: Do not report Over-range errors in the DATA_CHx registers. b1: Report Over-range errors in the DATA_CHx.CHx_ERR_OR register field corresponding to the channel that generated the error.
13	WD_ ERR2OUT	R/W	0	Watchdog Timeout Error to Output Register b0: Do not report Watchdog Timeout errors in the DATA_CHx registers. b1: Report Watchdog Timeout errors in the DATA_CHx.CHx_ERR_WD register field corresponding to the channel that generated the error.
12	AH_ERR2OUT	R/W	0	Amplitude High Error to Output Register b0:Do not report Amplitude High errors in the DATA_CHx registers. b1: Report Amplitude High errors in the DATA_CHx.CHx_ERR_AE register field corresponding to the channel that generated the error.
11	AL_ERR2OUT	R/W	0	Amplitude Low Error to Output Register b0: Do not report Amplitude High errors in the DATA_CHx registers. b1: Report Amplitude High errors in the DATA_CHx.CHx_ERR_AE register field corresponding to the channel that generated the error.
7	UR_ERR2INT	R/W	0	Under-range Error to INTB b0: Do not report Under-range errors by asserting INTB pin and STATUS register. b1: Report Under-range errors by asserting INTB pin and updating STATUS.ERR_UR register field.
6	OR_ERR2INT	R/W	0	Over-range Error to INTB b0: Do not report Over-range errors by asserting INTB pin and STATUS register. b1: Report Over-range errors by asserting INTB pin and updating STATUS.ERR_OR register field.
5	WD_ERR2INT	R/W	0	Watchdog Timeout Error to INTB b0: Do not report Under-range errors by asserting INTB pin and STATUS register. b1: Report Watchdog Timeout errors by asserting INTB pin and updating STATUS.ERR_WD register field.
4	AH_ERR2INT	R/W	0	Amplitude High Error to INTB b0: Do not report Amplitude High errors by asserting INTB pin and STATUS register. b1: Report Amplitude High errors by asserting INTB pin and updating STATUS.ERR_AHE register field.
3	AL_ERR2INT	R/W	0	Amplitude Low Error to INTB b0: Do not report Amplitude Low errors by asserting INTB pin and STATUS register. b1: Report Amplitude Low errors by asserting INTB pin and updating STATUS.ERR_ALE register field.
2	ZC_ERR2INT	R/W	0	Zero Count Error to INTB b0: Do not report Zero Count errors by asserting INTB pin and STATUS register. b1: Report Zero Count errors by asserting INTB pin and updating STATUS. ERR_ZC register field.
1	Reserved	R/W	0	Reserved (set to b0)
0	DRDY_2INT	R/W	0	Data Ready Flag to INTB b0: Do not report Data Ready Flag by asserting INTB pin and STATUS register. b1: Report Data Ready Flag by asserting INTB pin and updating STATUS. DRDY register field.

8.6.24 Address 0x1A, CONFIG

Figure 40. Address 0x1A, CONFIG

15	14	13	12	11	10	9	8
ACTIVE_CHAN		SLEEP_MODE_EN	RP_OVERRIDE_EN	SENSOR_ACTIVATE_SEL	AUTO_AMP_DIS	REF_CLK_SRC	RESERVED

7	6	5	4	3	2	1	0
INTB_DIS	HIGH_CURRENT_DRV	RESERVED					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 35. Address 0x1A, CONFIG Field Descriptions

Bit	Field	Type	Reset	Description
15:14	ACTIVE_CHAN	R/W	00	Active Channel Selection Selects channel for continuous conversions when MUX_CONFIG.SEQUENTIAL is 0. b00: Perform continuous conversions on Channel 0 b01: Perform continuous conversions on Channel 1 b10: Perform continuous conversions on Channel 2 (LDC1314 only) b11: Perform continuous conversions on Channel 3 (LDC1314 only)
13	SLEEP_MODE_EN	R/W	1	Sleep Mode Enable Enter or exit low power Sleep Mode. b0: Device is active. b1: Device is in Sleep Mode.
12	RP_OVERRIDE_EN	R/W	0	Sensor R_P Override Enable Provides control over Sensor current drive used during the conversion time for Ch. x, based on the programmed value in the CHx_IDRIVE field. b0: Override off b1: R_P Override on
11	SENSOR_ACTIVATE_SEL	R/W	1	Sensor Activation Mode Selection. Set the mode for sensor initialization. b0: Full Current Activation Mode – the LDC will drive maximum sensor current for a shorter sensor activation time. b1: Low Power Activation Mode – the LDC uses the value programmed in DRIVE_CURRENT_CHx during sensor activation to minimize power consumption.
10	AUTO_AMP_DIS	R/W	0	Automatic Sensor Amplitude Correction Disable Setting this bit will disable the automatic Amplitude correction algorithm and stop the updating of the CHx_INIT_IDRIVE field. b0: Automatic Amplitude correction enabled b1: Automatic Amplitude correction is disabled. Recommended for precision applications.
9	REF_CLK_SRC	R/W	0	Select Reference Frequency Source b0: Use Internal oscillator as reference frequency b1: Reference frequency is provided from CLKIN pin.
8	RESERVED	R/W	0	Reserved. Set to b0.
7	INTB_DIS	R/W	0	INTB Disable b0: INTB pin will be asserted when status register updates. b1: INTB pin will not be asserted when status register updates
6	HIGH_CURRENT_DRV	R/W	0	High Current Sensor Drive b0: The LDC will drive all channels with normal sensor current (1.5mA max). b1: The LDC will drive channel 0 with current >1.5mA. This mode is not supported if AUTOSCAN_EN = b1 (multi-channel mode)
5:0	RESERVED	R/W	00 0001	Reserved Set to b00’0001

8.6.25 Address 0x1B, MUX_CONFIG

Figure 41. Address 0x1B, MUX_CONFIG

15	14	13	12	11	10	9	8
AUTOSCAN_EN	RR_SEQUENCE		RESERVED				

7	6	5	4	3	2	1	0
RESERVED					DEGLITCH		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 36. Address 0x1B, MUX_CONFIG Field Descriptions

Bit	Field	Type	Reset	Description
15	AUTOSCAN_EN	R/W	0	Auto-Scan Mode Enable b0: Continuous conversion on the single channel selected by CONFIG.ACTIVE_CHAN register field. b1: Auto-Scan conversions as selected by MUX_CONFIG.RR_SEQUENCE register field.
14:13	RR_SEQUENCE	R/W	00	Auto-Scan Sequence Configuration Configure multiplexing channel sequence. The LDC will perform a single conversion on each channel in the sequence selected, and then restart the sequence continuously. b00: Ch0, Ch1 b01: Ch0, Ch1, Ch2 (LDC1314 only) b10: Ch0, Ch1, Ch2, Ch3 (LDC1314 only) b11: Ch0, Ch1
12:3	RESERVED	R/W	00 0100 0001	Reserved. Must be set to 00 0100 0001
2:0	DEGLITCH	R/W	111	Input deglitch filter bandwidth. Select the lowest setting that exceeds the oscillation tank oscillation frequency. b001: 1MHz b100: 3.3MHz b101: 10MHz b111: 33MHz

8.6.26 Address 0x1C, RESET_DEV

Figure 42. Address 0x1C, RESET_DEV

15	14	13	12	11	10	9	8
RESET_DEV	RESERVED				OUTPUT_GAIN		RESERVED

7	6	5	4	3	2	1	0
RESERVED							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 37. Address 0x1C, RESET_DEV Field Descriptions

Bit	Field	Type	Reset	Description
15	RESET_DEV	R/W	0	Device Reset Write b1 to reset the device. Will always readback 0.
14:11	RESERVED	R/W	0000	Reserved. Set to b0000
10:9	OUTPUT_GAIN	R/W	00	Output gain control 00: Gain = 1 (0 bits shift) 01: Gain = 4 (2 bits shift) 10: Gain = 8 (3 bits shift) 11: Gain = 16 (4 bits shift)
8:0	RESERVED	R/W	0 0000 0000	Reserved, Set to b0 0000 0000

8.6.27 Address 0x1E, DRIVE_CURRENT_CH0

Figure 43. Address 0x1E, DRIVE_CURRENT_CH0

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">CH0_IDRIVE</td><td colspan="3">CH0_INIT_IDRIVE</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CH0_INIT_IDRIVE</td><td colspan="6">RESERVED</td></tr>
<tr><td colspan="8"></td></tr>
</table>

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 38. Address 0x1E, DRIVE_CURRENT_CH0 Field Descriptions

Bit	Field	Type	Reset	Description
15:11	CH0_IDRIVE	R/W	0 0000	Channel 0 L-C Sensor drive current This field defines the Drive Current used during the settling + conversion time of Channel 0 sensor clock. RP_OVERRIDE_EN bit must be set to 1.
10:6	CH0_INIT_IDRIVE	R	0 0000	Channel 0 Sensor Current Drive This field stores the Initial Drive Current calculated during the initial Amplitude Calibration phase. It is updated after each Amplitude Correction phase of the sensor clock if the AUTO_AMP_DIS field is NOT set.
5:0	RESERVED	–	00 0000	Reserved

8.6.28 Address 0x1F, DRIVE_CURRENT_CH1

Figure 44. Address 0x1F, DRIVE_CURRENT_CH1

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">CH1_IDRIVE</td><td colspan="3">CH1_INIT_IDRIVE</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">CH1_INIT_IDRIVE</td><td colspan="6">RESERVED</td></tr>
<tr><td colspan="8"></td></tr>
</table>

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 39. Address 0x1F, DRIVE_CURRENT_CH1 Field Descriptions

Bit	Field	Type	Reset	Description
15:11	CH1_IDRIVE	R/W	0 0000	Channel 1 L-C Sensor drive current This field defines the Drive Current used during the settling + conversion time of Channel 1 sensor clock. RP_OVERRIDE_EN bit must be set to 1.
10:6	CH1_INIT_IDRIVE	R	0 0000	Channel 1 Sensor Current Drive This field stores the Initial Drive Current calculated during the initial Amplitude Calibration phase. It is updated after each Amplitude Correction phase of the sensor clock if the AUTO_AMP_DIS field is NOT set.
5:0	RESERVED	-	00 0000	Reserved

8.6.29 Address 0x20, DRIVE_CURRENT_CH2 (LDC1314 only)

Figure 45. Address 0x20, DRIVE_CURRENT_CH2

15	14	13	12	11	10	9	8
CH2_IDRIVE					CH2_INIT_IDRIVE		

7	6	5	4	3	2	1	0
CH2_INIT_IDRIVE		RESERVED					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 40. Address 0x20, DRIVE_CURRENT_CH2 Field Descriptions

Bit	Field	Type	Reset	Description
15:11	CH2_IDRIVE	R/W	0 0000	Channel 2 L-C Sensor drive current This field defines the Drive Current to be used during the settling + conversion time of Channel 2 sensor clock. RP_OVERRIDE_EN bit must be set to 1.
10:6	CH2_INIT_IDRIVE	R	0 0000	Channel 2 Sensor Current Drive This field stores the Initial Drive Current calculated during the initial Amplitude Calibration phase. It is updated after each Amplitude Correction phase of the sensor clock if the AUTO_AMP_DIS field is NOT set.
5:0	RESERVED	–	00 0000	Reserved

8.6.30 Address 0x21, DRIVE_CURRENT_CH3 (LDC1314 only)

Figure 46. Address 0x21, DRIVE_CURRENT_CH3

15	14	13	12	11	10	9	8
CH3_IDRIVE					CH3_INIT_IDRIVE		

7	6	5	4	3	2	1	0
CH3_INIT_IDRIVE		RESERVED					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 41. DRIVE_CURRENT_CH3 Field Descriptions

Bit	Field	Type	Reset	Description
15:11	CH3_IDRIVE	R/W	0 0000	Channel 3 L-C Sensor drive current This field defines the Drive Current to be used during the settling + conversion time of Channel 3 sensor clock. RP_OVERRIDE_EN bit must be set to 1.
10:6	CH3_INIT_IDRIVE	R	0 0000	Channel 3 Sensor Current Drive This field stores the Initial Drive Current calculated during the initial Amplitude Calibration phase. It is updated after each Amplitude Correction phase of the sensor clock if the AUTO_AMP_DIS field is NOT set.
5:0	RESERVED	–	00 0000	Reserved

8.6.31 Address 0x7E, MANUFACTURER_ID

Figure 47. Address 0x7E, MANUFACTURER_ID

15	14	13	12	11	10	9	8
MANUFACTURER_ID							

7	6	5	4	3	2	1	0
MANUFACTURER_ID							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 42. Address 0x7E, MANUFACTURER_ID Field Descriptions

Bit	Field	Type	Reset	Description
15:0	MANUFACTURER_ID	R	0101 0100 0100 1001	Manufacturer ID = 0x5449

8.6.32 Address 0x7F, DEVICE_ID

Figure 48. Address 0x7F, DEVICE_ID

7	6	5	4	3	2	1	0
DEVICE_ID							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 43. Address 0x7F, DEVICE_ID Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID	R	0011 0000 0101 0100	Device ID = 0x3054

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Theory of Operation

9.1.1.1 Conductive Objects in an EM Field

An AC current flowing through an inductor will generate an AC magnetic field. If a conductive material, such as a metal object, is brought into the vicinity of the inductor, the magnetic field will induce a circulating current (eddy current) on the surface of the conductor.

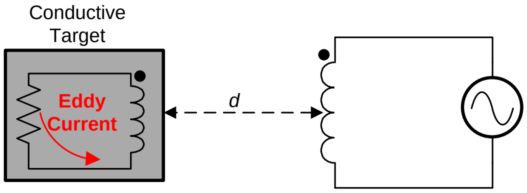


Figure 49. Conductor in AC Magnetic Field

The eddy current is a function of the distance, size, and composition of the conductor. The eddy current generates its own magnetic field, which opposes the original field generated by the sensor inductor. This effect is equivalent to a set of coupled inductors, where the sensor inductor is the primary winding and the eddy current in the target object represents the secondary inductor. The coupling between the inductors is a function of the sensor inductor, and the resistivity, distance, size, and shape of the conductive target. The resistance and inductance of the secondary winding caused by the eddy current can be modeled as a distance dependent resistive and inductive component on the primary side (coil). Figure 49 shows a simplified circuit model of the sensor and the target as coupled coils.

9.1.1.2 L-C Resonators

An EM field can be generated using an L-C resonator, or L-C tank. One topology for an L-C tank is a parallel R-L-C construction, as shown in Figure 50.

Application Information (continued)

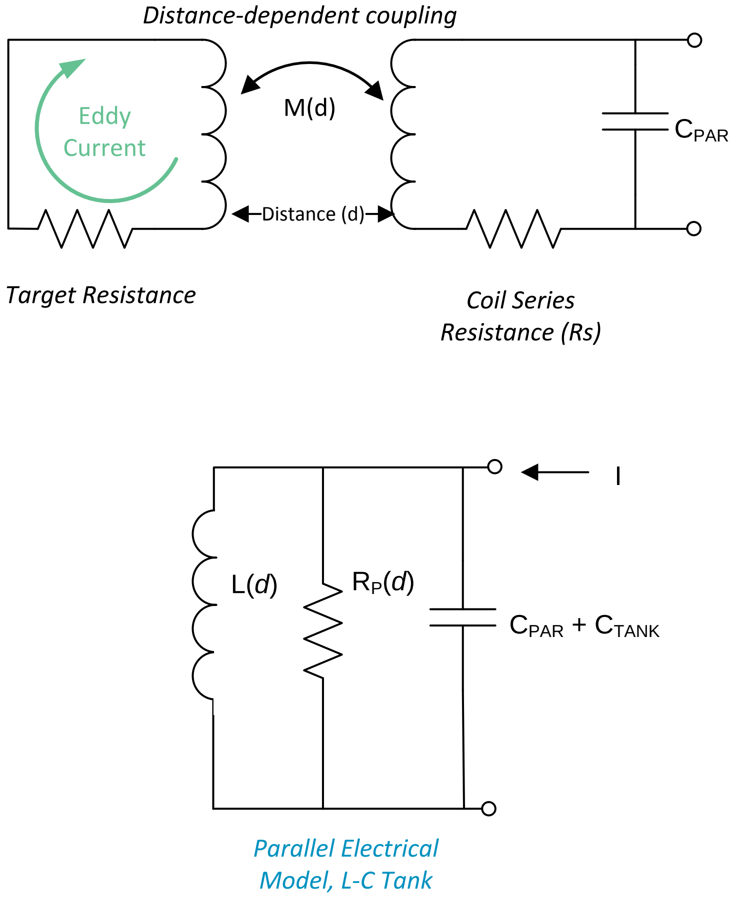


Figure 50. Electrical Model of the L-C Tank Sensor

An oscillator can be constructed by combining a frequency selective circuit (resonator) with a gain block in a closed loop. The criteria for oscillation are: (1) loop gain > 1, and (2) closed loop phase shift of 2π radians. The R-L-C resonator provides the frequency selectivity and contributes to the phase shift. At resonance, the impedance of the reactive components (L and C) cancels, leaving only R_P, the lossy (resistive) element in the circuit. The voltage amplitude is maximized. The R_P can be used to determine the sensor drive current. A lower R_P requires a larger sensor current to maintain a constant oscillation amplitude. The sensor oscillation frequency is given by:

$$f_{\text{SENSOR}} = \frac{1}{2\pi\sqrt{LC}} * \sqrt{1 - \frac{1}{Q^2} - \frac{5*10^{-9}}{Q\sqrt{LC}}} \approx \frac{1}{2\pi\sqrt{LC}}$$

where

- C is the sensor capacitance (C_{TANK} + C_{PAR})
- L is the inductance
- Q is the quality factor of the resonator. Q can be approximated by: (9)

$$Q = R_P\sqrt{\frac{C}{L}}$$

where

- R_S is the AC series resistance of the inductor (10)

Application Information (continued)

Texas Instruments' WEBENCH design tool can be used for coil design, in which the parameter values for R_P, L and C are calculated. See http://www.ti.com/webench.

R_P is a function of target distance, target material, and sensor characteristics. Figure 51 shows that R_P is directly proportional to the distance between the sensor and the target. The graph represents a 14-mm diameter PCB coil (23 turns, 4-mil trace width, 4-mil spacing between traces, 1-oz copper thickness, FR4).

Figure 51. Example RP vs. Distance with a 14-mm PCB Coil and 2mm Thick Stainless Steel Target

It is important to configure the LDC current drive so that the sensor will still oscillate at the minimum R_P value. For example, if the closest target distance in a system with the response shown in Figure 51 is 1mm, then the LDC R_P value is 5 kΩ. The objective is to maintain a sufficient sensor oscillation voltage so that the sensor frequency can be measured even at the minimum operating distance. See section *Current Drive Control Registers* for details on setting the current drive.

The inductance that is measured by the LDC is

$$L(d) = L_{inf} - M(d) = \frac{1}{(2\pi * f_{SENSOR})^2 * C}$$

where

- L(d) is the measured sensor inductance, for a distance d between the sensor coil and target
- L_{inf} is the inductance of the sensing coil without a conductive target (target at infinite distance)
- M(d) is the mutual inductance
- f_{SENSOR} = sensor oscillation frequency for a distance d between the sensor coil and target
- $C = C_{TANK} + C_{PAR}$ (11)

Figure 52 shows an example of variation in sensor frequency and inductance as a function of distance for a 14-mm diameter PCB coil (23 turns, 4-mil trace width, 4-mil spacing between traces, 1-oz copper thickness, FR4).

Application Information (continued)

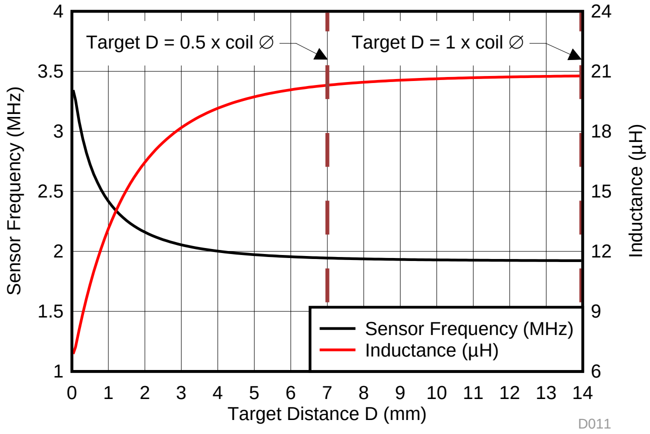


Figure 52. Example Sensor Frequency, Inductance vs. Target Distance with 14-mm PCB Coil and 1.5 mm Thick Aluminum Target

In the absence of magnetic materials, such as ferrous metals and ferrites, the inductance shift, and therefore the measured frequency shift, depends only on current flow geometries. Temperature drift is dominated by physical expansion of the inductor and other mechanical system components over temperature which alter current flow geometries. Note that the additional temperature drift of the sensor capacitor must also be taken into account.

For additional information on temperature effects and temperature compensation, see *LDC1000 Temperature Compensation* (SNAA212)

9.2 Typical Application

Example of a multi-channel implementation using the LDC1312. This example is representative of an axial displacement application, in which the target movement is perpendicular to the plane of the coil. The second channel can be used to sense proximity of a second target, or it can be used for temperature compensation by connecting a reference coil.

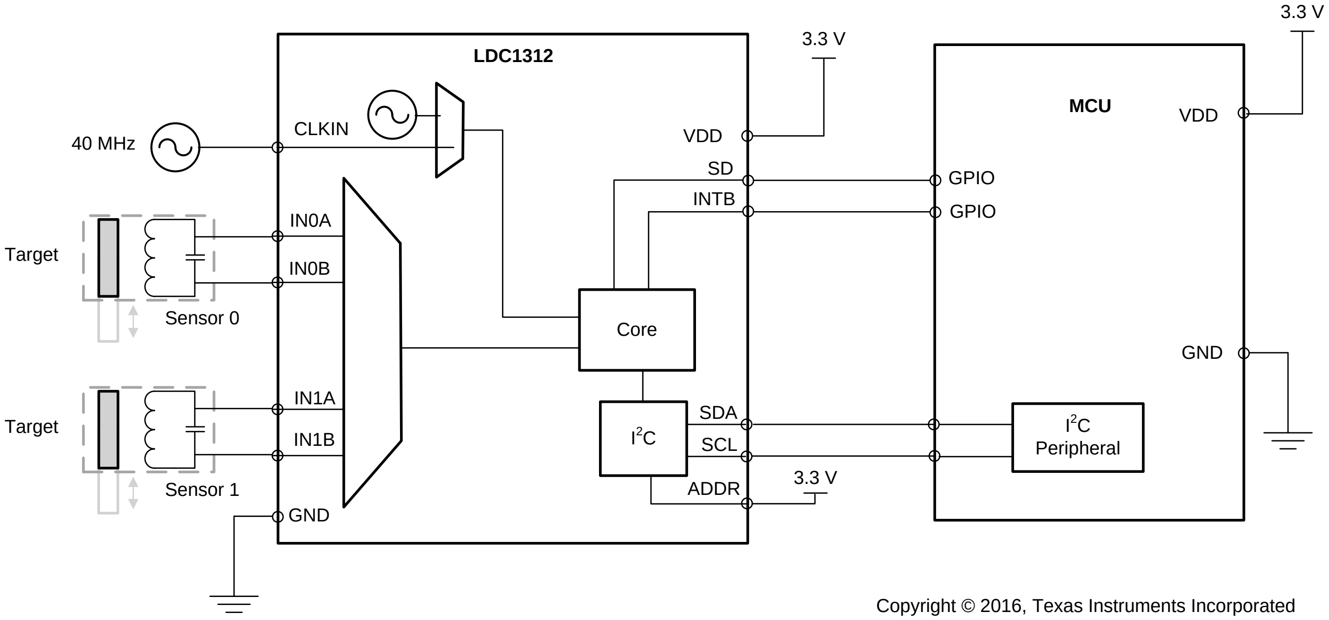


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Figure 53. Example Multi-Channel Application - LDC1312

Typical Application (continued)

9.2.1 Design Requirements

- Design example in which Sensor 0 is used for proximity measurement and Sensor 1 is used for temperature compensation:
- Using WEBENCH for coil design
- Target distance = 0.1 cm
- Distance resolution = 0.2 µm
- Target diameter = 1 cm
- Target material = stainless steel (SS416)
- Number of PCB layers for the coil = 2
- The application requires 500SPS (T_{SAMPLE} = 2000 µs)

9.2.2 Detailed Design Procedure

The target distance, resolution and diameter are used as inputs to WEBENCH to design the sensor coil, The resulting coil design is a 2 layer coil, with an area of 2.5 cm^2, diameter of 1.77 cm, and 39 turns. The values for R_P, L and C are: R_P = 6.6 kΩ, L = 43.9 µH, C = 100 pF.

Using L and C, $f_{SENSOR} = 1/2\pi\sqrt{(LC)} = 1/2\pi\sqrt{(43.9*10^{-6} * 100*10^{-12})} = 2.4$ MHz

Using a system master clock of 40 MHz applied to the CLKIN pin allows flexibility for setting the internal clock frequencies. The sensor coil is connected to channel 0 (IN0A and IN0B pins).

After powering on the LDC, it will be in Sleep Mode. Program the registers as follows (example sets registers for channel 0 only; channel 1 registers can use equivalent configuration):

1. Set the dividers for channel 0.
   (a) Because the sensor freqeuncy is less than 8.75 MHz, the sensor divider can be set to 1, which means setting field CH0_FIN_DIVIDER to 0x1. By default, $f_{IN0} = f_{SENSOR}$ = 2.4MHz.
   (b) The design constraint for f_{REF0} is > 4 × f_{SENSOR}. A 20 MHz reference frequency satisfies this constraint, so the reference divider should be set to 2. This is done by setting the CH0_FREF_DIVIDER field to 0x02.
   (c) The combined value for Chan. 0 divider register (0x14) is 0x1002.
2. Program the settling time for Channel 0. The calculated Q of the coil is 10 (see *Multi-Channel and Single Channel Operation*).
   (a) CH0_SETTLECOUNT ≥ Q × f_{REF0} / (16 × $f_{SENSOR0}$) → 5.2, rounded up to 6. To provide margin to account for system tolerances, a higher value of 10 is chosen.
   (b) Register 0x10 should be programmed to a minimum of 10.
   (c) The settle time is: (10 x 16)/20,000,000 = 8 µs
   (d) The value for Chan. 0 SETTLECOUNT register (0x10) is 0x000A.
3. The channel switching delay is ~1µs for f_{REF} = 20 MHz (see *Multi-Channel and Single Channel Operation*)
4. Set the conversion time by the programming the reference count for Channel 0. The budget for the conversion time is : T_{SAMPLE} – settling time – channel switching delay = 1000 – 8 – 1 = 991 µs
   (a) To determine the conversion time register value, use the following equation and solve for CH0_RCOUNT: Conversion Time (t_{C0})= (CH0_RCOUNT×16)/f_{REF0}.
   (b) This results in CH0_RCOUNT having a value of 1238 decimal (rounded down)
   (c) Set the CH0_RCOUNT register (0x08) to 0x04D6.
5. Use the default values for the ERROR_CONFIG register (address 0x19). By default, no interrupts are enabled
6. Sensor drive current: to set the CH0_IDRIVE field value, read the value from Table 10 using R_P = 6.6 kΩ. In this case the IDRIVE value should be set to 18 (decimal). The INIT_DRIVE current field should be set to 0x00. The combined value for the DRIVE_CURRENT_CH0 register (addr 0x1E) is 0x9000.
7. Program the MUX_CONFIG register
   (a) Set the AUTOSCAN_EN to b1 bit to enable sequential mode
   (b) Set RR_SEQUENCE to b00 to enable data conversion on two channels (channel 0, channel 1)
   (c) Set DEGLITCH to b100 to set the input deglitch filter bandwidth to 3.3MHz, the lowest setting that exceeds the oscillation tank frequency.
   (d) The combined value for the MUX_CONFIG register (address 0x1B) is 0x820C

Typical Application (continued)

8. Finally, program the CONFIG register as follows:
   (a) Set the ACTIVE_CHAN field to b00 to select channel 0.
   (b) Set SLEEP_MODE_EN field to b0 to enable conversion.
   (c) Set RP_OVERRIDE_EN to b1 to disable auto-calibration.
   (d) Set SENSOR_ACTIVATE_SEL = b0, for full current drive during sensor activation
   (e) Set the AUTO_AMP_DIS field to b1 to disable auto-amplitude correction
   (f) Set the REF_CLK_SRC field to b1 to use the external clock source.
   (g) Set the other fields to their default values.
   (h) The combined value for the CONFIG register (address 0x1A) is 0x1601.

   We then read the conversion results for channel 0 and channel 1 every 1000 µs from register addresses 0x00 and 0x02.

9.2.2.1 *Recommended Initial Register Configuration Values*

Based on the example configuration in section *Detailed Design Procedure*, the following register write sequence is recommended:

Table 44. Recommended Initial Register Configuration Values (Single-channel Operation)

Address	Value	Register Name	Comments
0x08	0x04D6	RCOUNT_CH0	Reference count calculated from timing requirements (1 kSPS) and resolution requirements
0x10	0x000A	SETTLECOUNT_CH0	Minimum settling time for chosen sensor
0x14	0x1002	CLOCK_DIVIDERS_CH0	CH0_FIN_DIVIDER = 1, CH0_FREF_DIVIDER = 2
0x19	0x0000	ERROR_CONFIG	Can be changed from default to report status and error conditions
0x1B	0x020C	MUX_CONFIG	Enable Ch 0 (continuous mode), set Input deglitch bandwidth to 3.3MHz
0x1E	0x9000	DRIVE_CURRENT_CH0	Sets sensor drive current on ch 0
0x1A	0x1601	CONFIG	Select active channel = ch 0, disable auto-amplitude correction and auto-calibration, enable full current drive during sensor activation, select external clock source, wake up device to start conversion. This register write must occur last because device configuration is not permitted while the LDC is in active mode.

Table 45. Recommended Initial Register Configuration Values (Multi-channel Operation)

Address	Value	Register Name	Comments
0x08	0x04D6	RCOUNT_CH0	Reference count calculated from timing requirements (1 kSPS) and resolution requirements
0x09	0x04D6	RCOUNT_CH1	Reference count calculated from timing requirements (1 kSPS) and resolution requirements
0x10	0x000A	SETTLECOUNT_CH0	Minimum settling time for chosen sensor
0x11	0x000A	SETTLECOUNT_CH1	Minimum settling time for chosen sensor
0x14	0x1002	CLOCK_DIVIDERS_CH0	CH0_FIN_DIVIDER = 1, CH0_FREF_DIVIDER = 2
0x15	0x1002	CLOCK_DIVIDERS_CH1	CH1_FIN_DIVIDER = 1, CH1_FREF_DIVIDER = 2
0x19	0x0000	ERROR_CONFIG	Can be changed from default to report status and error conditions
0x1B	0x820C	MUX_CONFIG	Enable Ch 0 and Ch 1 (sequential mode), set Input deglitch bandwidth to 3.3MHz
0x1E	0x9000	DRIVE_CURRENT_CH0	Sets sensor drive current on ch 0
0x1F	0x9000	DRIVE_CURRENT_CH1	Sets sensor drive current on ch 1

Table 45. Recommended Initial Register Configuration Values (Multi-channel Operation) (continued)

Address	Value	Register Name	Comments
0x1A	0x1601	CONFIG	disable auto-amplitude correction and auto-calibration, enable full current drive during sensor activation, select external clock source, wake up device to start conversion. This register write must occur last because device configuration is not permitted while the LDC is in active mode.

9.2.2.2 Inductor Self-Resonant Frequency

Every inductor has a distributed parasitic capacitance, which is dependent on construction and geometry. At the Self-Resonant Frequency (SRF), the reactance of the inductor cancels the reactance of the parasitic capacitance. Above the SRF, the inductor will electrically appear to be a capacitor. Because the parasitic capacitance is not well-controlled or stable, TI recommends that: $f_{SENSOR} < 0.8 \times f_{SR}$.

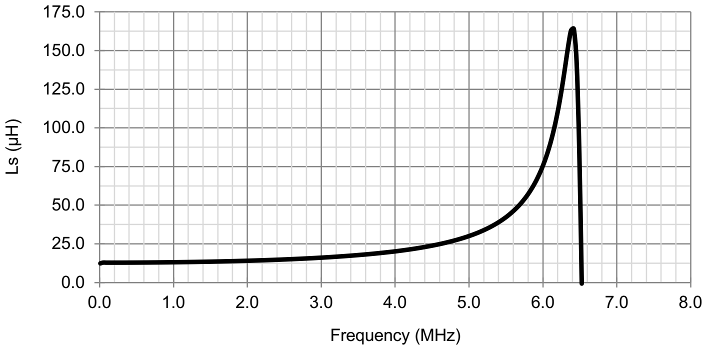

Figure 54. Example Coil Inductance vs. Frequency

In Figure 54, the inductor has a SRF at 6.38 MHz; therefore the inductor should not be operated above 0.8×6.38 MHz, or 5.1 MHz.

9.2.3 Application Curves

Common test conditions (unless specified otherwise):

- Sensor inductor: 2 layer, 32 turns/layer, 14mm diameter, PCB inductor with L=19.4 µH, R_P=5.7 kΩ at 2 MHz
- Sensor capacitor: 330pF 1% COG/NP0
- Target: Aluminum, 1.5 mm thickness
- Channel = Channel 0 (continuous mode)
- CLKIN = 40MHz, CHx_FIN_DIVIDER = 0x01, CHx_FREF_DIVIDER = 0x001
- CH0_RCOUNT = 0xFFFF, SETTLECOUNT_CH0 = 0x0100
- RP_OVERRIDE = 1, AUTO_AMP_DIS = 1, DRIVE_CURRENT_CH0 = 0x9800

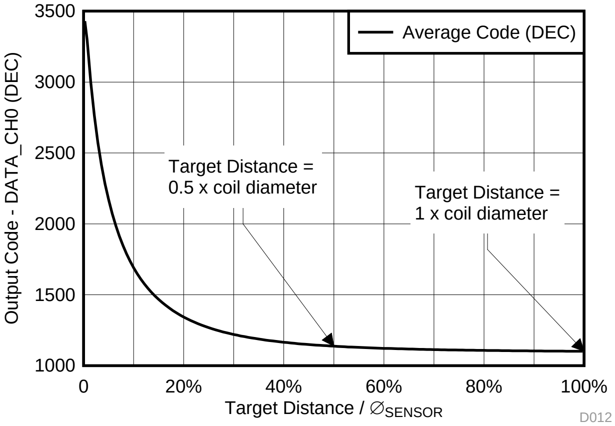

Figure 55. Typical Output Code vs. Target Distance (0 to 14mm)

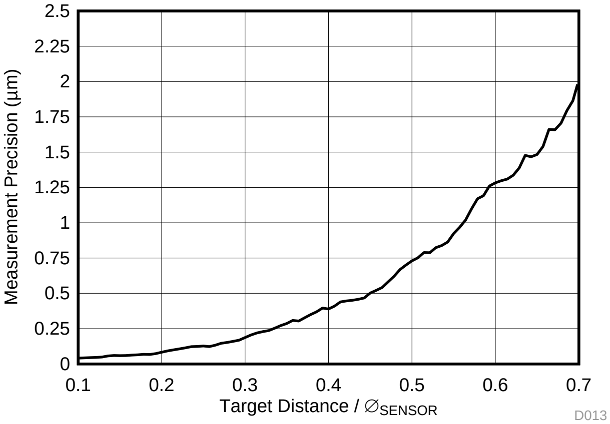

Figure 56. Measurement precision in Distance vs. Target Distance (0 to 10mm)

10 Power Supply Recommendations

- The LDC requires a voltage supply within 2.7 V and 3.6 V. A multilayer ceramic bypass X7R capacitor of 1µF between the VDD and GND pins is recommended. If the supply is located more than a few inches from the LDC, additional bulk capacitance may be required in addition to the ceramic bypass capacitor. An electrolytic capacitor with a value of 10µF is a typical choice.
- The optimum placement is closest to the VDD and GND terminals of the device. Care should be taken to minimize the loop area formed by the bypass capacitor connection, the VDD terminal, and the GND terminal of the IC. See Figure 57 and Figure 58 for a layout example.

11 Layout

11.1 Layout Guidelines

Avoid long traces to connect the sensor to the LDC. Short traces reduce parasitic capacitances between sensor inductor and offer higher system performance.

11.2 Layout Example

Figure 57 to Figure 60 show the LDC1312 evaluation module (EVM) layout.

Layout Example (continued)

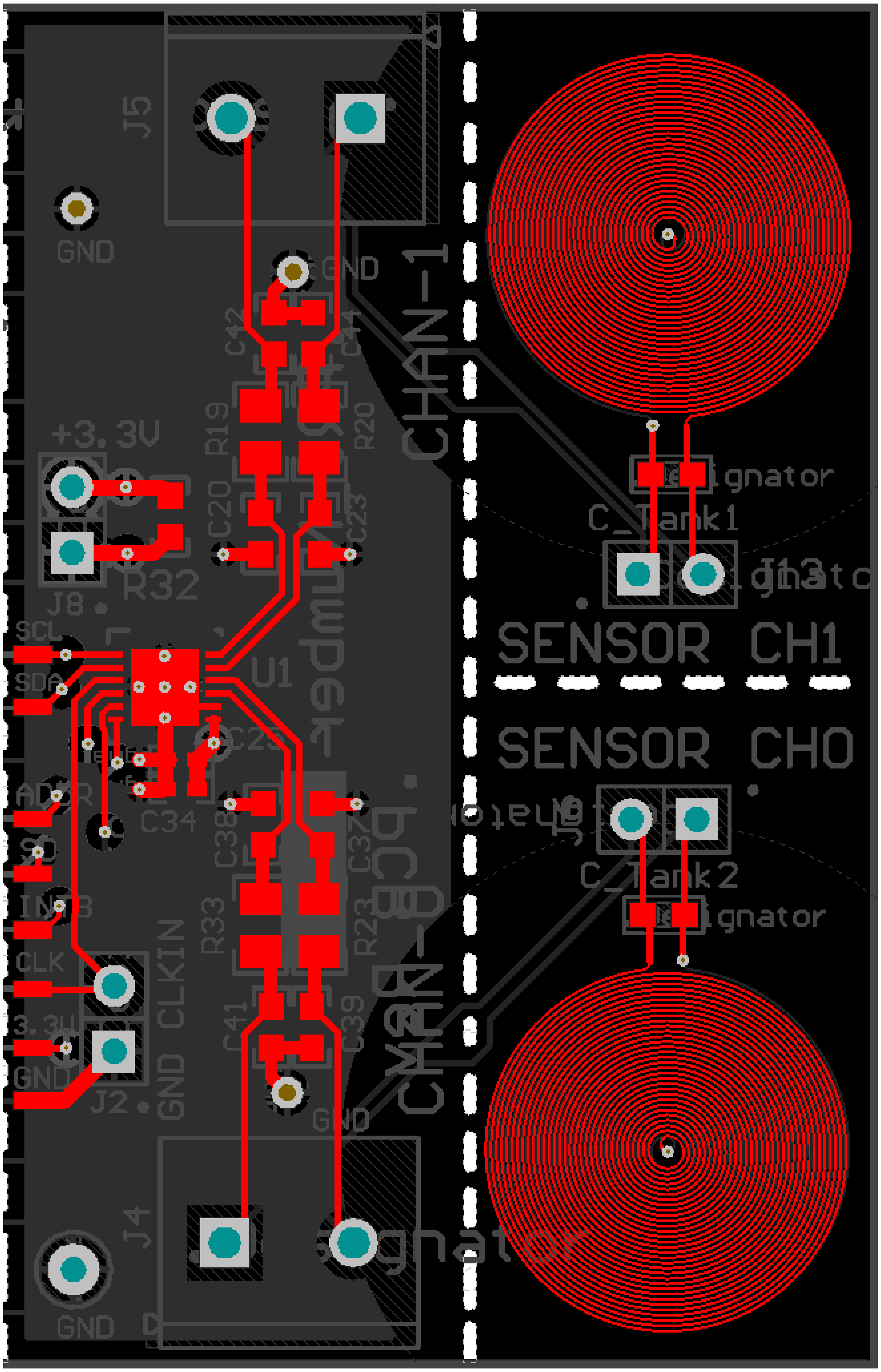

Figure 57. Example PCB Layout: Top Layer (Signal)

Layout Example (continued)

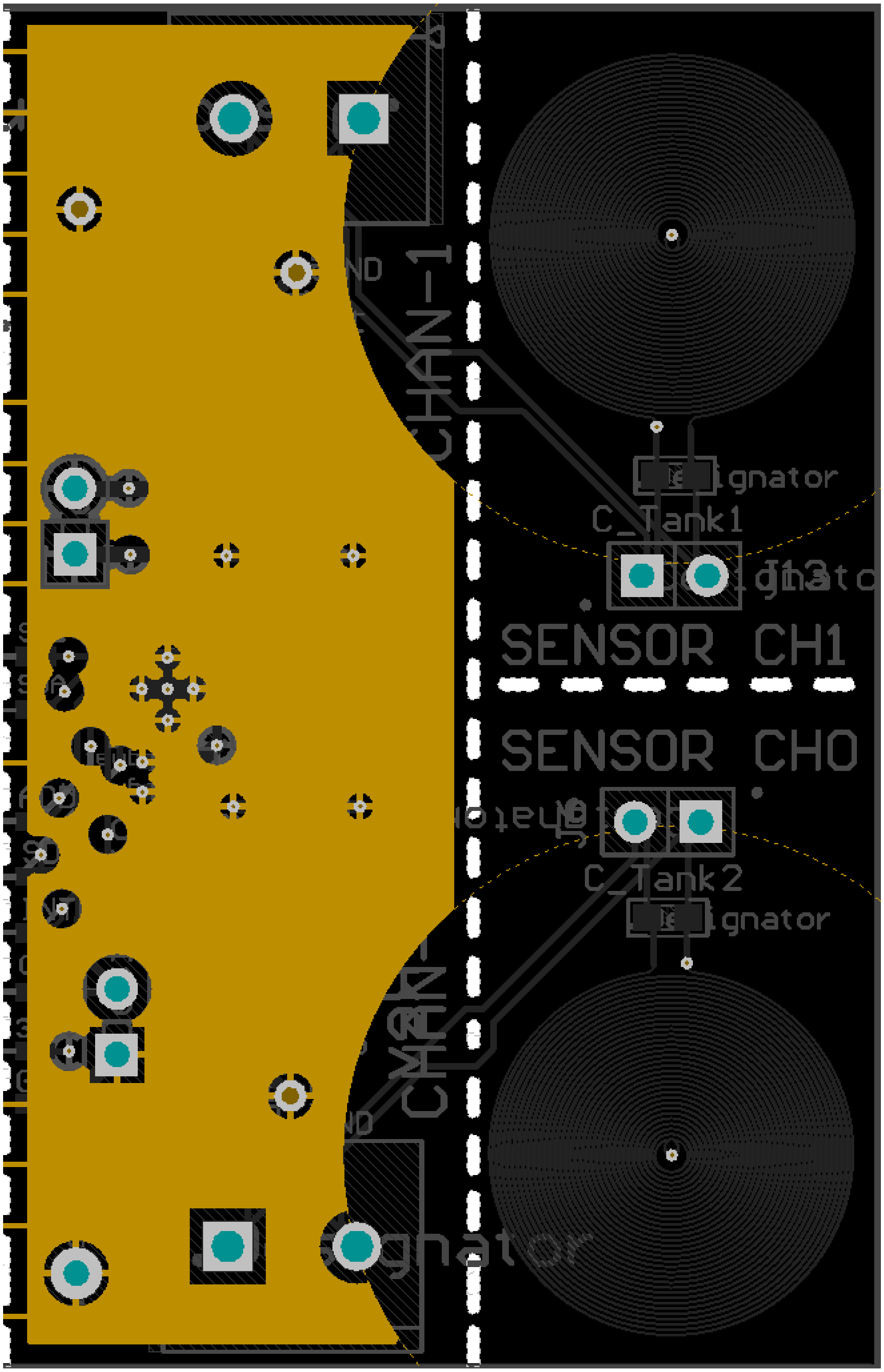

Figure 58. Example PCB Layout: Mid-layer 1 (GND)

Layout Example (continued)

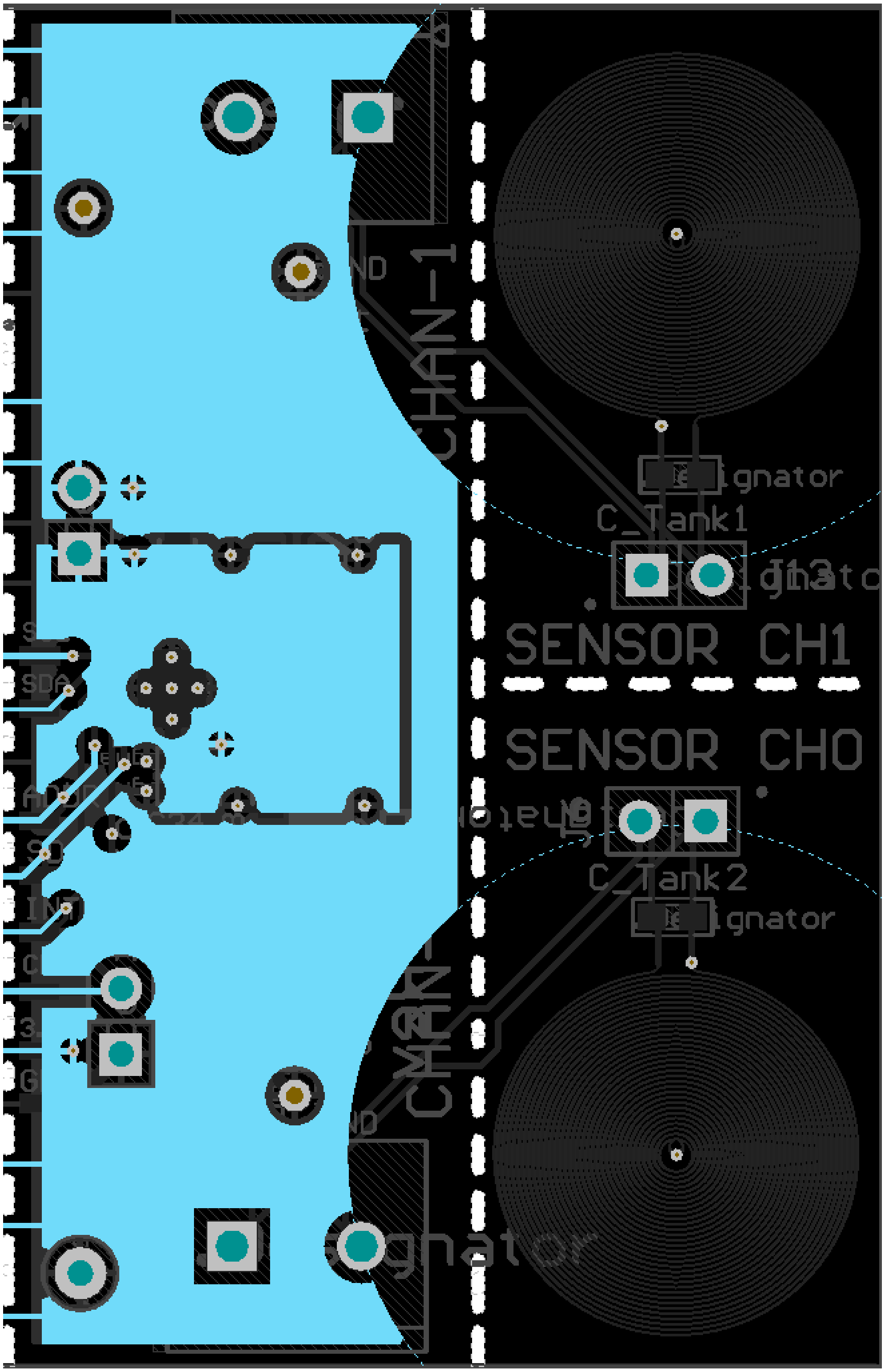

Figure 59. Example PCB Layout: Mid-layer 2 (Power)

Layout Example (continued)

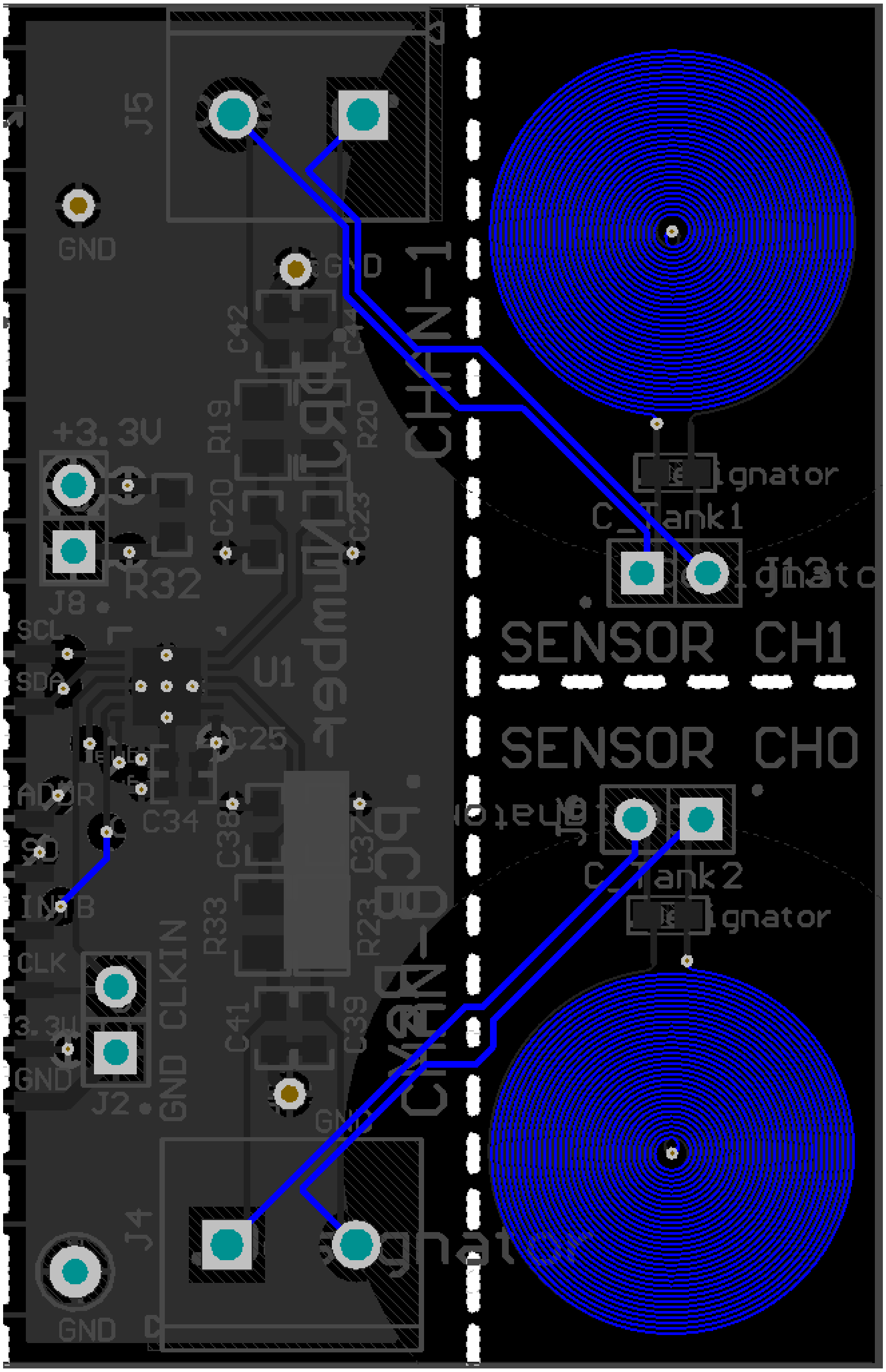

Figure 60. Example PCB Layout: Bottom Layer (Signal)

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

For related links, see the following:

- Texas Instruments' WEBENCH tool: http://www.ti.com/webench

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, refer to the following:

- *LDC1000 Temperature Compensation* (SNAA212)

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Related Links

The Table 46 below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 46. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LDC1312-Q1	Click here	Click here	Click here	Click here	Click here
LDC1314-Q1	Click here	Click here	Click here	Click here	Click here

12.5 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LDC1312QDNTRQ1	ACTIVE	WSON	DNT	12	4500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LC1312Q Q1	Samples
LDC1312QDNTTQ1	ACTIVE	WSON	DNT	12	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LDC1312 Q1	Samples
LDC1314QRGHRQ1	ACTIVE	WQFN	RGH	16	4500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LC1314Q	Samples
LDC1314QRGHTQ1	ACTIVE	WQFN	RGH	16	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LC1314Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LDC1312-Q1, LDC1314-Q1 :

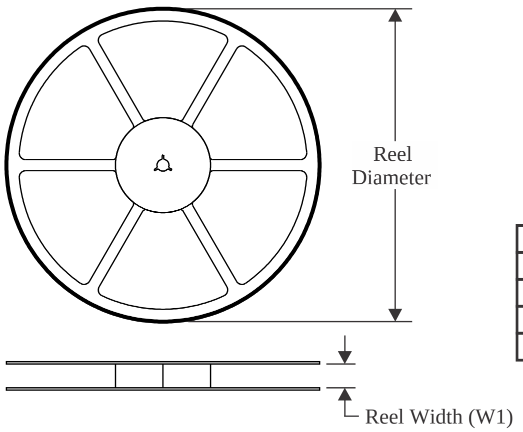
- Catalog: LDC1312, LDC1314

NOTE: Qualified Version Definitions:

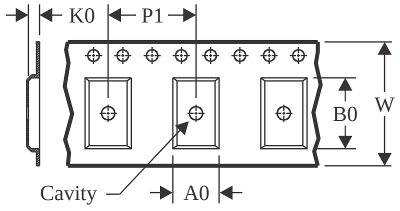
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

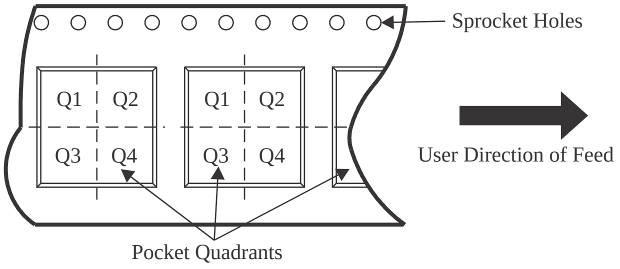


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

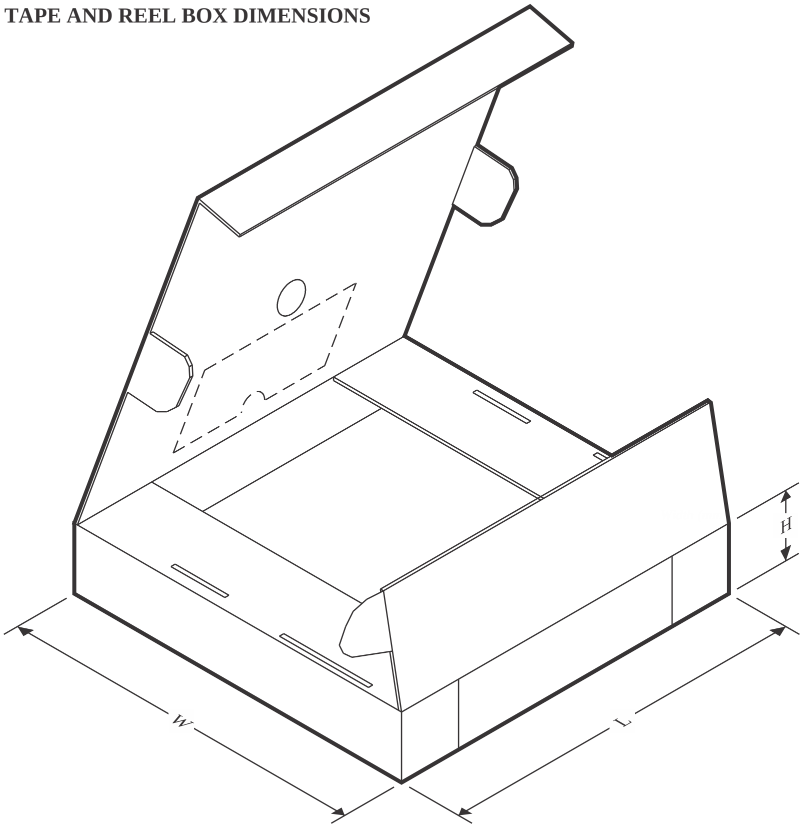
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LDC1312QDNTRQ1	WSON	DNT	12	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LDC1312QDNTTQ1	WSON	DNT	12	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LDC1314QRGHRQ1	WQFN	RGH	16	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LDC1314QRGHTQ1	WQFN	RGH	16	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



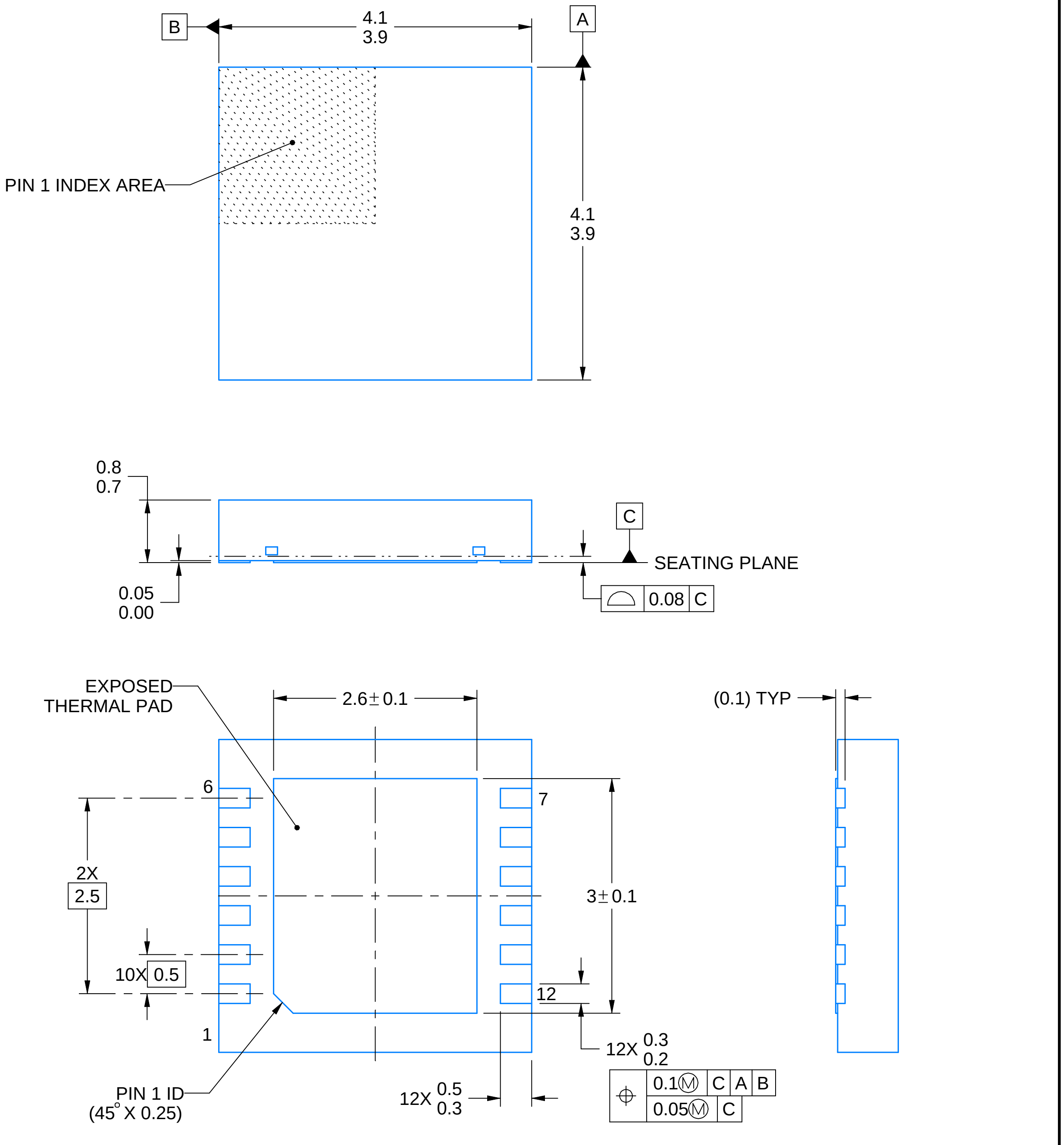
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LDC1312QDNTRQ1	WSON	DNT	12	4500	356.0	356.0	35.0
LDC1312QDNTTQ1	WSON	DNT	12	250	367.0	367.0	35.0
LDC1314QRGHRQ1	WQFN	RGH	16	4500	356.0	356.0	35.0
LDC1314QRGHTQ1	WQFN	RGH	16	250	208.0	191.0	35.0

DNT0012B

WSON - 0.8 mm max height

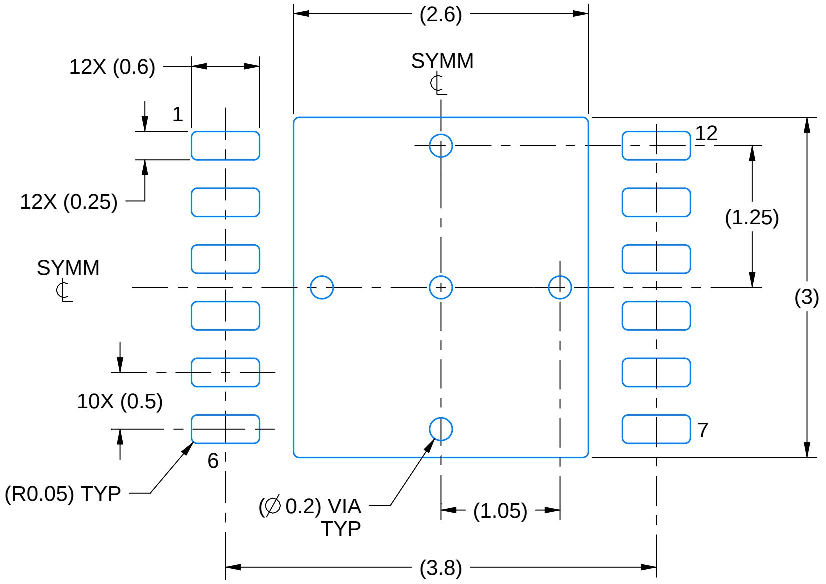
PLASTIC SMALL OUTLINE - NO LEAD



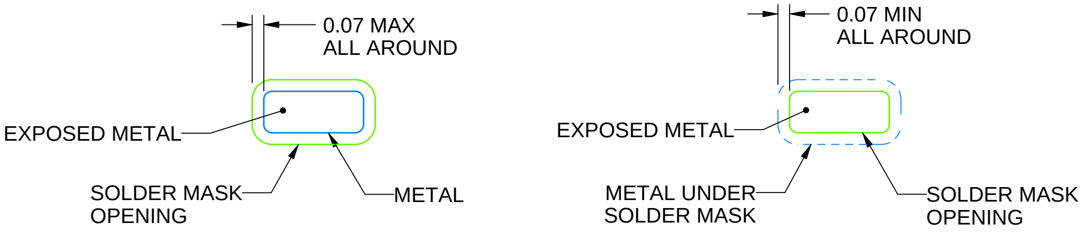
4214928/C 10/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



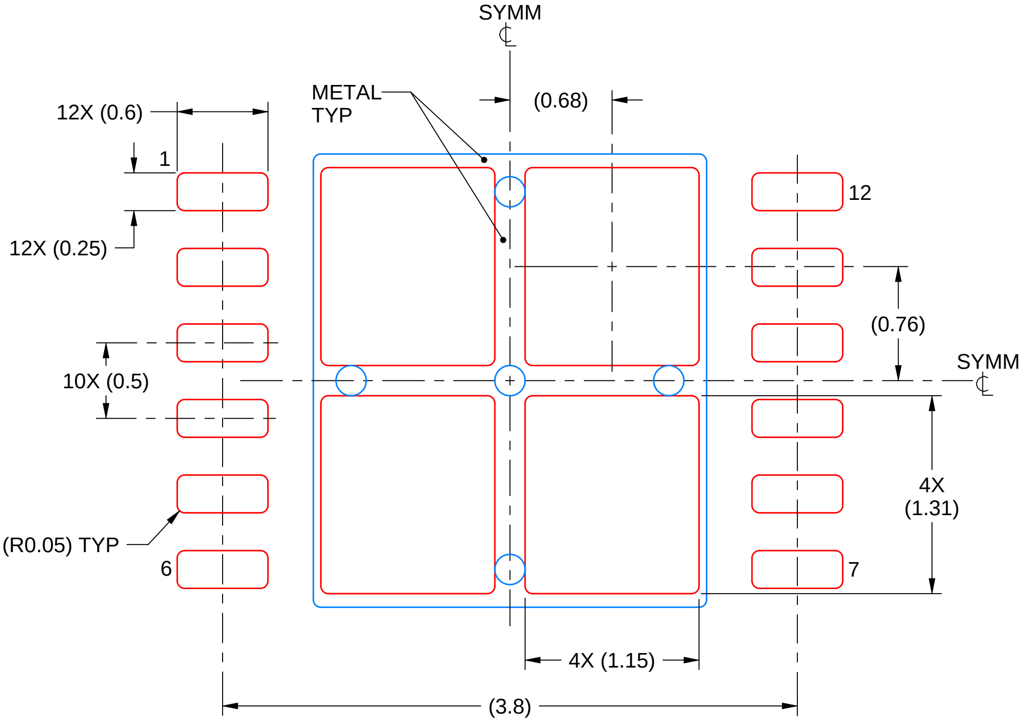
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



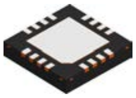
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

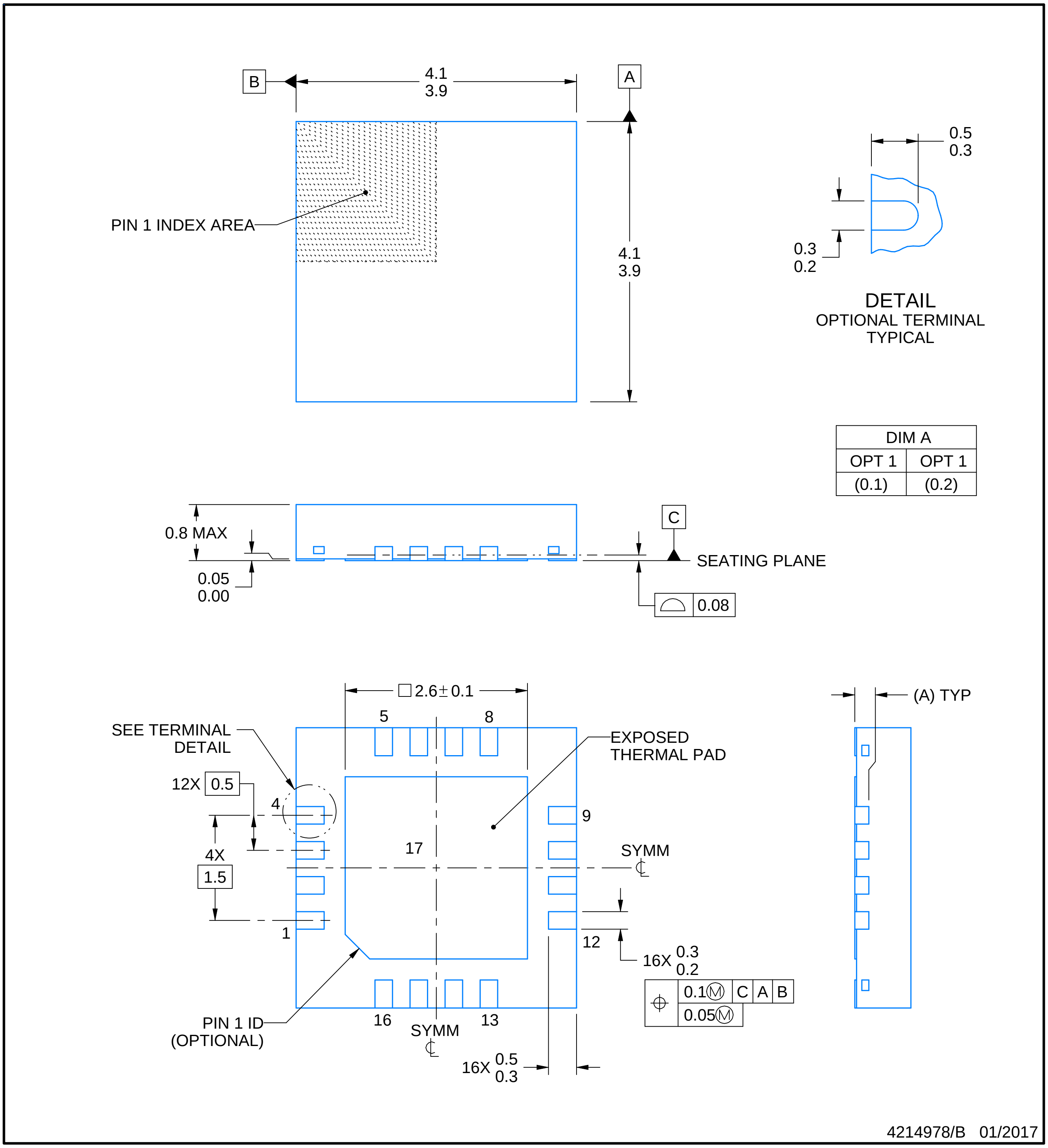
RGH0016A



PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



DIM A	
OPT 1	OPT 1
(0.1)	(0.2)

4214978/B 01/2017

NOTES:

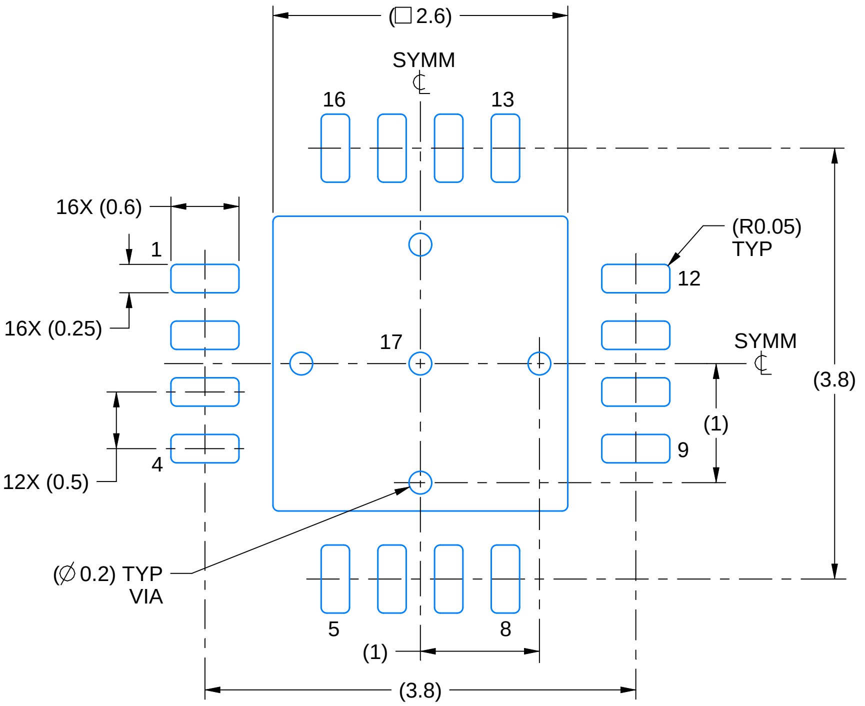
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

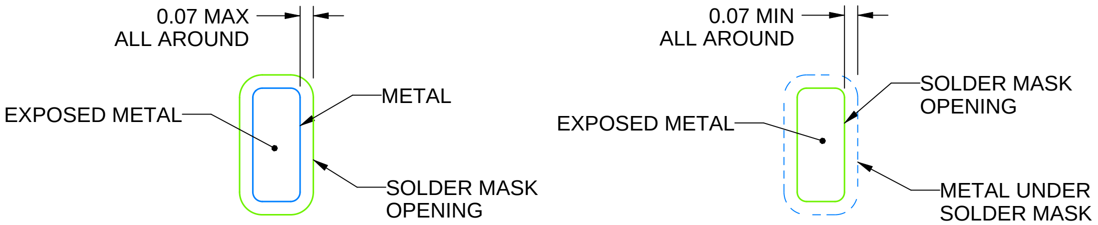
RGH0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



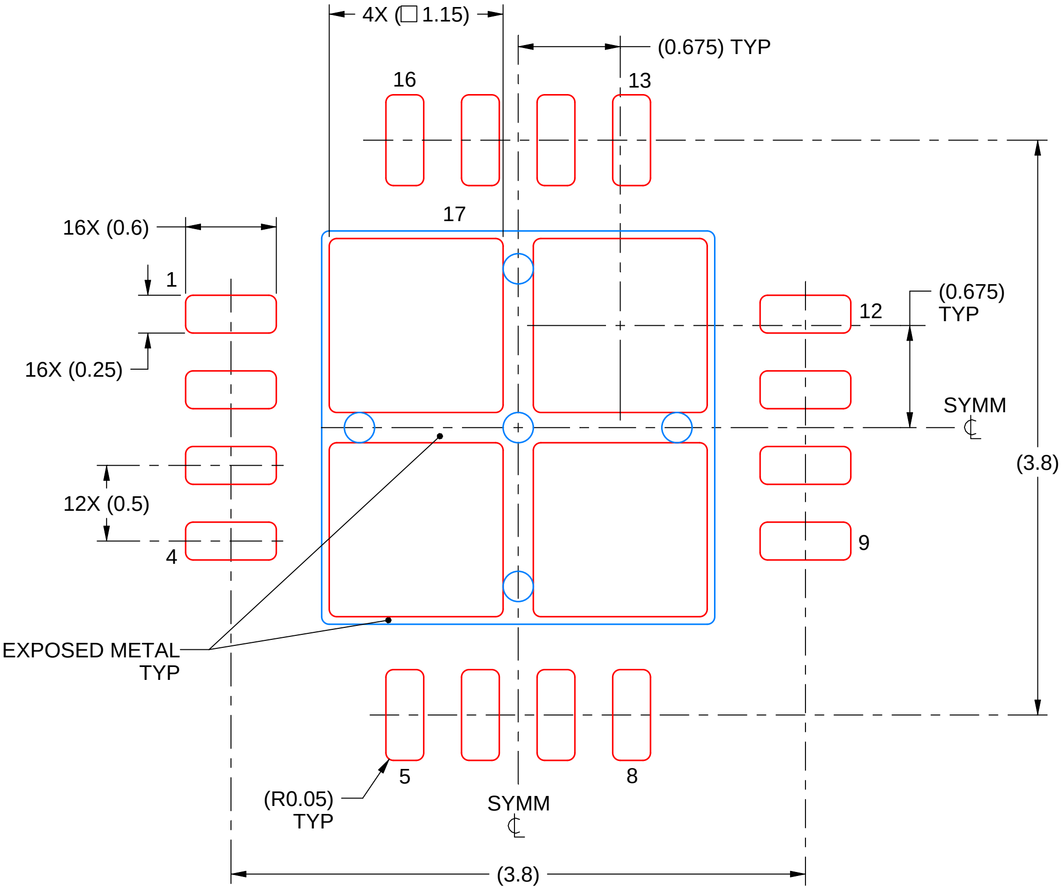
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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