Application Report
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Optimizing L Measurement Resolution for the LDC161x and LDC1101

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ABSTRACT

TI's LDC1612, LDC1614, and LDC1101 devices are versatile devices which use the LHR core (High-Resolution L measurement) for Inductance measurements. This application note covers configuration options and methods to improve the effective resolution of these devices.

Contents

1 Understanding LDC Resolution

For an ADC, the resolution is generally the number of bits in the output word, and the effective resolution is determined from the either the INL of static linearity or from the SINAD of a full scale sinewave. If the signal amplitude input to an ADC is less than full scale, the resolution of the output word is still the same, but the effective resolution decreases. For example, given an ADC with an input range of 1 VPP and an effective resolution of 16 bits, if the input signal is only 500 mVPP, then the effective resolution will usually be halved to 15 bits.

Most inductive sensors are not able to utilize the full scale input range that TI's LDCs provide. This results in a reduction in the effective resolution of the system. The larger the shift in sensor inductance due to target movement, the more effective resolution the LDC can provide. A system which has an inductance shift of 20% will have twice the effective resolution of an equivalent system which has a 10% shift.

TI's LDC devices measure the inductance by measuring the resonant frequency of a sensor, and so the LDC can be considered a frequency measurement version of an ADC. Where an ADC has an LSB measured in voltage, an LDC has an LSB measured in Hz.

For example, with an LDC system with a frequency resolution of 1 Hz (1 LSB = 1 Hz), if the sensor signal varies by 100 kHz, then the LDC would have an effective resolution of 16.6 bits.

There are two basic approaches to increase the effective resolution – first by improving the frequency resolution, and second by increasing the sensor frequency variation.

2 LDC Configuration Parameters

There are several LDC parameters which determine the device resolution.

2.1 Reference Count and RCOUNT

The primary device setting which determines the conversion resolution is the RCOUNT setting. A higher value for RCOUNT corresponds to a higher resolution L measurement.

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Table 1. RCOUNT Registers

DEVICE	REGISTERS
LDC1612	RCOUNT_CH0 (address 0x08) RCOUNT_CH1 (address 0x09)
LDC1614	RCOUNT_CH0 (address 0x08) RCOUNT_CH1 (address 0x09) RCOUNT_CH2 (address 0x0A) RCOUNT_CH3 (address 0x0B)
LDC1101	LHR_RCOUNT (address 0x30 + 0x31)

Due to device restrictions, RCOUNT must be ≥3 and ≤65535. For the LDC1101, RCOUNT is set in two 8-bit wide registers, LHR_RCOUNT_LSB and LHR_RCOUNT_MSB. For the LDC1612 and LDC1614, there are 2 or 4 16-bit wide registers, respectively, for setting RCOUNT independently for each device channel.

The effective LDC resolution is a function of the RCOUNT and sensor frequency. Higher values of RCOUNT deliver increased resolution, and lower sensor frequencies can provide improved resolution.

2.2 Reference Frequency

The reference frequency determines the conversion time for a given RCOUNT value. The basic conversion time equation is shown in Equation 1.

$$t_{CONVERSION}(s) = \frac{RCOUNT \times 16}{f_{REF}} \quad (1)$$

It is clear that to increase the sample rate, the reference frequency should be increased and/or the setting of RCOUNT should be decreased. As mentioned previously, decreasing RCOUNT will decrease the measurement resolution.

As a general rule, use the highest reference frequency supported by a given LDC. Then set RCOUNT value that the sample rate matches the minimum system requirement.

Table 2. Supported Reference Frequency and Sample Rates

	LDC161x	LDC1101
Number of channels	2 (LDC1612) 4 (LDC1614)	1
Maximum reference frequency	40-MHz dual channel 35-MHz single channel	16 MHz
Maximum output resolution	28 bits	24 bits
Conversion time for maximum RCOUNT at highest f_{REF}	26.2 ms at 40 MHz 30.0 ms at 35 MHz	65.5 ms

2.3 Reference Dividers

The LDC devices include input and clock dividers for more flexibility in setting the sensor frequency and reference frequency in a system.

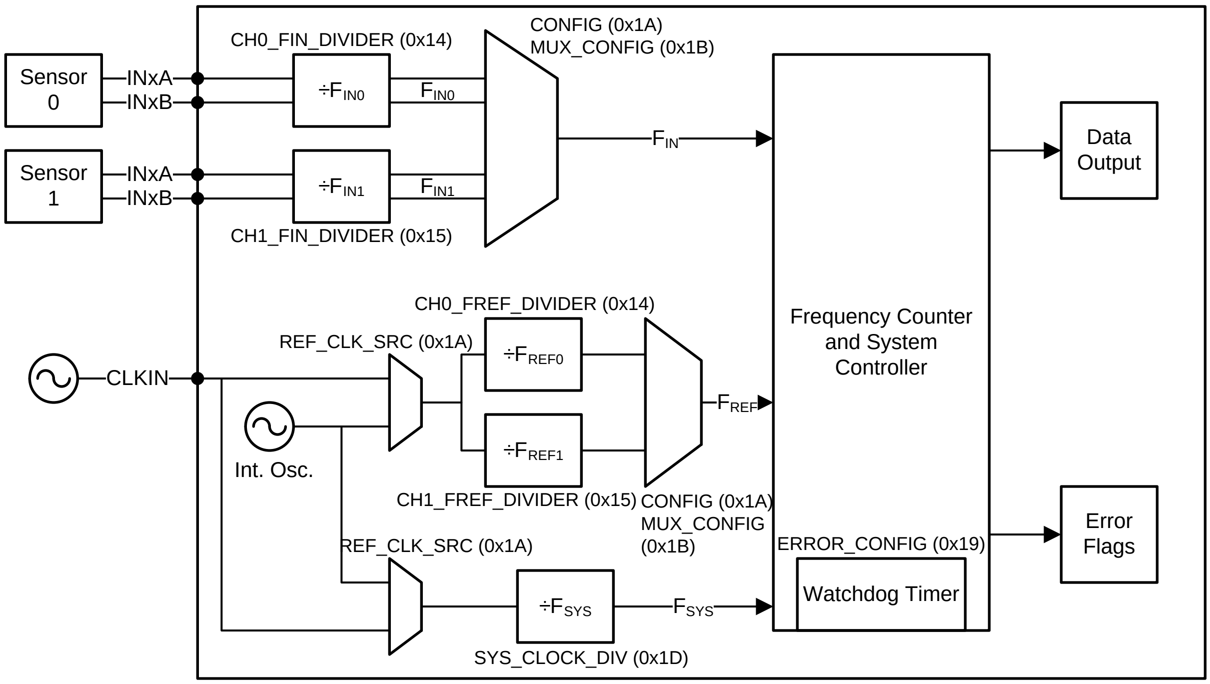

Figure 1. LDC161x Clocking Diagram

2.3.1 Divider Recommendations for LDC161x

For the LDC161x devices, set f_{REF} divider to 1 when:

- sampling in sequential mode and $f_{CLKIN} \leq 40$ MHz, or
- using one channel (continuous sampling mode) and $f_{CLKIN} \leq 35$ MHz

For the LDC161x devices, set f_{REF} divider to 2 when using one channel (continuous sampling mode) and 35 MHz < $f_{CLKIN} \leq 40$ MHz

2.3.2 Divider Recommendations for LDC1101

For the LDC1101, there is only a divider on the sensor input. Normal usage is to set SENSOR_DIV to 1. When f_{CLKIN} is less than f_{SENSOR}, set SENSOR_DIV to an appropriate value so that f_{SENSOR}/SENSOR_DIV < f_{CLKIN}.

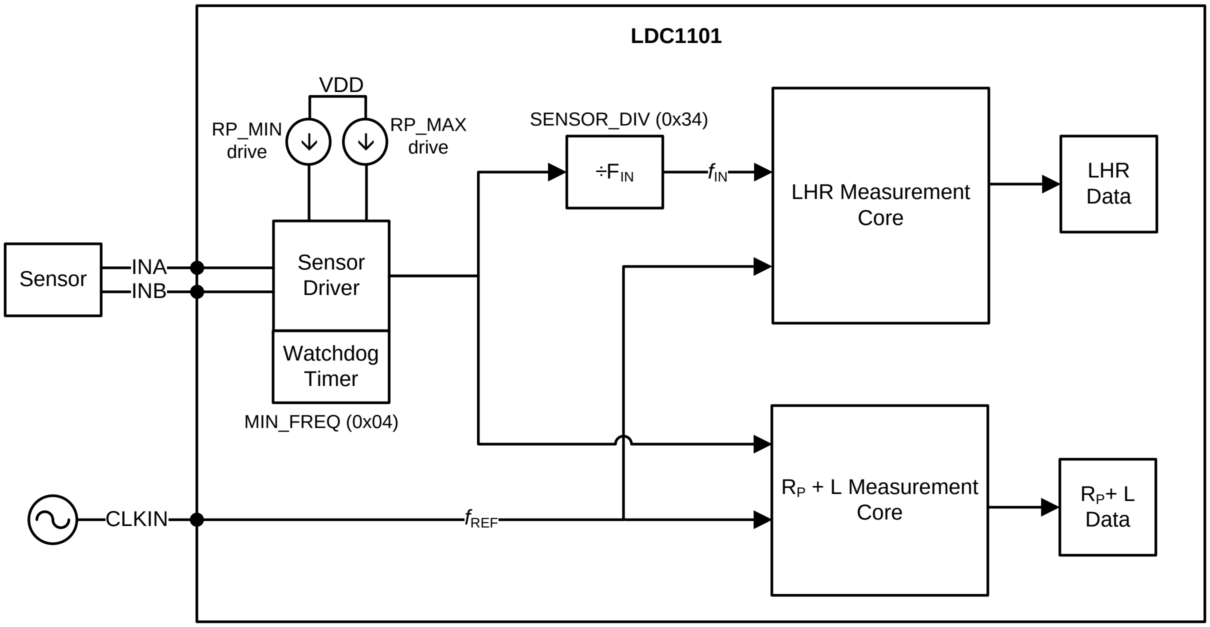

Figure 2. LDC1101 Clocking Diagram

2.4 *Resolution as a Function of Sensor Frequency*

The effective resolution also varies based on the sensor frequency. At higher sensor frequencies, the LDC will appear to having missing codes, where the gaps between subsequent output codes will become larger and larger as the sensor frequency increases. This is why the effective resolution drops off as the sensor frequency increases. Note that set of output codes is a function of the value of RCOUNT – a different value for RCOUNT will produce a different set of output codes.

At low sensor frequencies, the LDC output code will increment by 1 code as the sensor frequency increases, as expected. However, as the frequency increases further, then the output code will start skipping 1 code, then skipping several codes, and then gap between output codes will become larger and larger.

At very low frequencies, the resolution of the LDC161x device is limited by the output word width of 28bits. At these low frequencies, the LDC161x will output sequential codes. While the resolution may be maximized with a low sensor frequency, the maximum useful resolution occurs with f_{SENSOR} between 400 kHz and 6 MHz (with f_{REF} = 40 MHz).

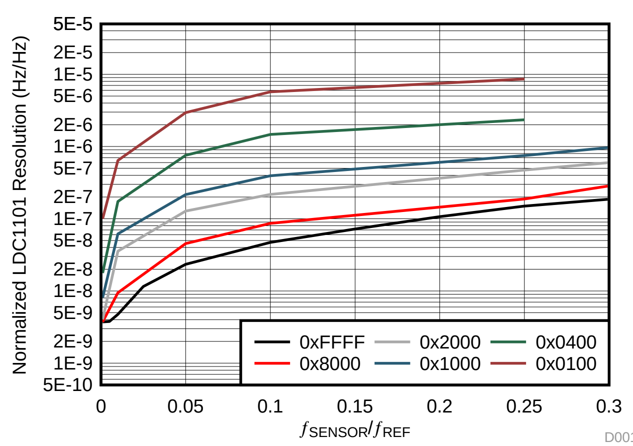

Figure 3. Normalized Frequency Resolution of the LDC161x vs f_{SENSOR} and RCOUNT

In Figure 3, the effective resolution of the LDC161x across various RCOUNT settings and sensor frequencies is shown. Smaller values of normalized resolution correspond to higher effective resolution, and so setting RCOUNT = 0x0100 will have a lower effective resolution than RCOUNT = 0xFFFF. When the f_{SENSOR}/f_{REF} ratio is below 0.005 for RCOUNT=0xFFFF, the LDC161x is output-bit limited. Lower values of RCOUNT will be bit limited at lower ratio values.

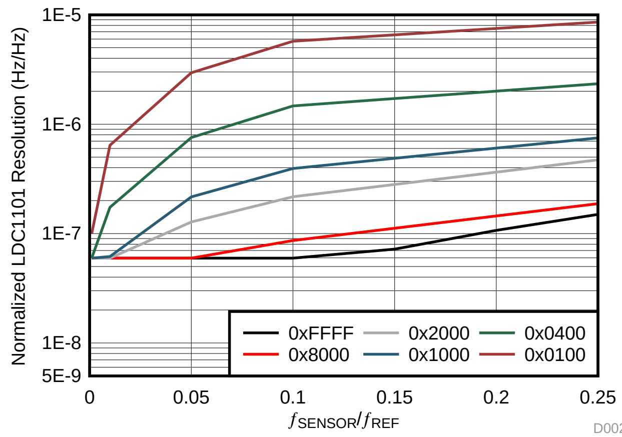

Figure 4. Normalized LDC1101 Resolution vs f_{SENSOR} and RCOUNT

For the LDC1101, the transfer curve is similar to the LDC161x, except that the 24 bits of resolution result in a bit-limited resolution limit at higher ratio settings.

The normalized resolution shown in Figure 3 needs to be scaled by the device reference frequency to obtain the LDC sensor resolution.

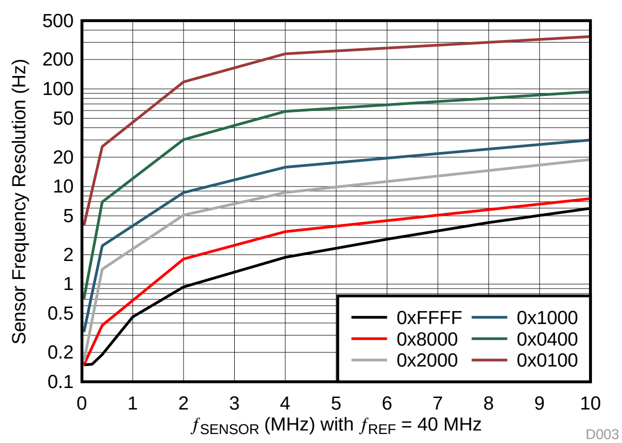

Figure 5. LDC161x Resolution with f_{REF} = 40 MHz

This maximum performance can be seen as the larger value of unique output codes for a 1% sensor frequency variation. This number of unique of output codes corresponds to the effective device resolution for the system configuration.

Table 3. LDC161x Resolution of a 1% f_{SENSOR} Variation with RCOUNT = 0xFFFF

f_{SENSOR} (f_{REF} = 40 MHz)	RATIO f_{SENSOR}/f_{REF}	# UNIQUE OUTPUT CODES	OUTPUT CODE
39.6 kHz → 40.0 kHz	0.001	2684	2684
198.0 kHz → 200.0 kHz	0.005	13237	13422
396.0 kHz → 400.0 kHz	0.01	21066	26844
990.0 kHz → 1.0 MHz	0.025	21686	67109
1.98 MHz → 2.00 MHz	0.05	21381	134218

Table 3. LDC161x Resolution of a 1% f_{SENSOR} Variation with RCOUNT = 0xFFFF (continued)

f_{SENSOR} (f_{REF} = 40 MHz)	RATIO f_{SENSOR}/f_{REF}	# UNIQUE OUTPUT CODES	OUTPUT CODE
3.96 MHz → 4.00 MHz	0.10	21274	268435
5.94 MHz → 6.00 MHz	0.15	20798	402653
7.92 MHz → 8.00 MHz	0.20	18725	536871
9.90 MHz → 10.00 MHz	0.25	16709	671089

The **# UNIQUE OUTPUT CODES** is the important column in Table 3 as the number of unique codes is the effective resolution of the LDC for the given signal. The range of output codes does not correspond to the effective resolution; for example, a 1% shift for a 6-MHz sensor has range of 402653 codes, but only 20798 unique output codes when RCOUNT = 0xFFFF. If the sensor frequency is increased to 10 MHz, a 1% frequency shift will have a code range of 671089 output codes, which is 67% higher; however the number of unique codes is 20% lower.

The ratio of 0.025 provides the highest resolution.

Increasing the frequency variation and increasing RCOUNT will improve the number of unique output codes.

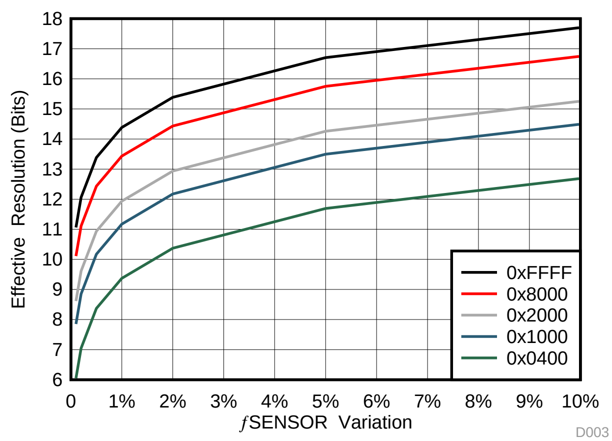

Figure 6. Effective Resolution vs RCOUNT and Variation for f_{SENSOR} = 2 MHz

2.5 Sensor Amplitude

The sensor oscillation amplitude indirectly affects the effective measurement resolution of LDC devices. In general, higher sensor oscillation amplitude improves the SNR for a given sensor. The LDC1612 and LDC1614 devices control the sensor amplitude based on the IDRIVE current setting. Configuring the sensor amplitude to the recommended range of 1.2 V to 1.8 V will provide the optimum measurement resolution.

2.5.1 LDC1101 L-Only Mode

By default, the LDC1101 applies an amplitude modulated envelope to the sensor oscillation. This envelope is used to measure the sensor RP in conjunction with the inductance measurement. The LDC1101 monitors the sensor amplitude and automatically adjusts the sensor drive by alternating between the RPMIN and RPMAX current drive settings.

For systems which do not require the RP measurement, this modulation can be disabled to improve the effective L measurement. Refer to the LDC1101 data sheet (SNOSD01) for information on how to enable this mode and to properly configure the LDC1101 sensor amplitude.

2.5.2 Deglitch Filter Setting

The LDC1612 and LDC1614 feature internal filters which improve the frequency measurement accuracy. There are 4 settings: 1 MHz, 3.3 MHz, 10 MHz, and 33 MHz. This setting should be set to the lowest of the 4 values that exceeds the maximum sensor frequency, which typically occurs with the highest target-sensor interaction.

2.5.3 Injection Resonance Locking

In the same way that independent pendulum clocks can become synchronized (as first documented by Christiaan Huygens), the LDC can exhibit resonance locking. With low sensor amplitudes, a small amount of energy can couple from an external clock source into the sensor, and lock the sensor frequency to an integer divider of the clock frequency. For example, if the sensor frequency should be 8.0003 MHz due to the target interaction, the sensor frequency could remain at 8 MHz if the reference frequency was 40 MHz.

This effect is more pronounced with lower value odd dividers of the reference frequency (f_{CLKIN}÷3, f_{CLKIN}÷5, f_{CLKIN}÷7) than higher value dividers or even dividers. It is important to note that it is the external frequency f_{CLKIN} that couples into the oscillator, not the internal frequency f_{REF}.

This effect can be reduced by:

- Shifting the sensor frequency away from a strong locking frequency (one way is to simply adjust the sensor capacitance).
- Increasing the sensor current drive value.
- Using a different f_{CLKIN} that does not have an odd integer divider in the sensor frequency variation.
- Ensuring the CLKIN line has well-controlled Z0 and does not exhibit significant overshoot/undershoot.
- Using a good ground plane for the LDC
- Maintaining separation between the sensor traces and the CLKIN line.

3 LDC Clocking

3.1 Internal Oscillator vs External Oscillator

The LDC1612 and LDC1614 devices include an internal oscillator; the LDC1101 does not include this feature. While the internal oscillator has a small shift across temperature, it is not as stable as a good external oscillator. For the LDC161x, it is recommended to use an external oscillator whenever possible.

Figure 7 was collected from a typical LDC1614 EVM. It shows the increase in RMS code noise when the internal oscillator is enabled when compared to the external oscillator is used.

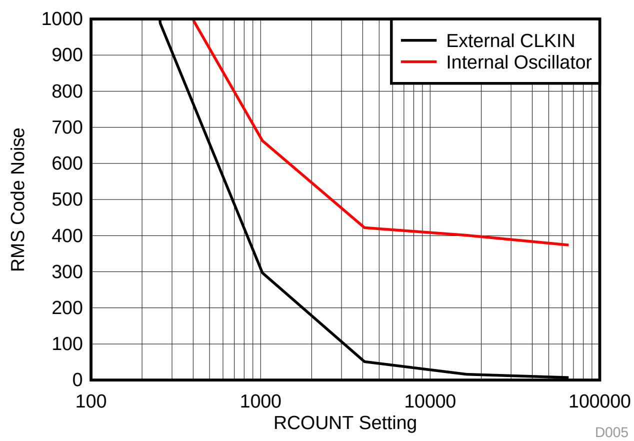

Figure 7. LDC161x RMS Code vs RCOUNT for Internal and External Clock Sources with the LDC161x EVM Sensor

3.2 Single-Channel f_{REF} Limitation Work-Around

If using the LDC1612 or LDC1614 in single channel mode, the maximum reference frequency supported is 35 MHz. For systems which have a fixed sample rate, this limitation results in a 14% reduction in resolution compared to the 40 MHz maximum available for multi-channel operation.

For systems where f_{CLKIN} = 40MHz, the CLKIN Divider must be set to 2 to comply with the maximum f_{REF} of 35 MHz. This division produces a f_{REF} = 20 MHz, which results in a 50% drop in resolution compared to the maximum 40-MHz f_{REF}.

If the Channel 0 activation time (which is roughly Q/f_{SENSOR}) is short enough, it may be advantageous to attach an additional sensor onto channel 1 but ignore the conversion data from Channel 1. In this way the LDC161x can operate with f_{REF}=40 MHz, but at the cost of conversion time on the second channel. The sensor geometries do not need to match Channel 0's sensor.

To maximize the effectiveness of this technique, the Channel 1's conversion time and settling count should be set to the device minimum (RCOUNT_CH1=3, SETTLECOUNT_CH1 = 1).

For a 1-MHz sensor with a Q of 20 up to sample rates of 1500 SPS, this technique improves the resolution compared to using a 35-MHz f_{REF}. For a sensor frequency of 5 MHz with a Q of 20, this technique is useful up to sample rates over 6k SPS, which exceeds the data rate of the LDC161x.

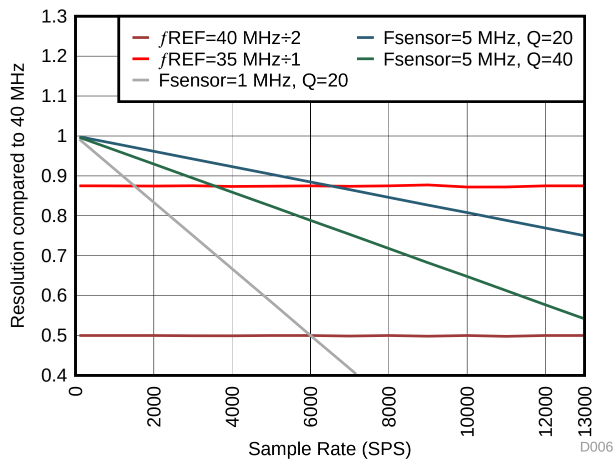

Figure 8. Effective Resolution Comparison for Various LDC Clocking Configurations

The sensor activation time is based on the sensor frequency and Q. Decreasing the sensor Q and/or increasing f_{SENSOR} for the dummy second channel will reduce the activation time, which makes this technique more effective.

4 Summary

There are several parameters in the LDC devices which affect the device resolution. These are primarily managing the sensor frequency, RCOUNT values, using a clean reference clock source, and properly setting the sensor current drive.

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