LM3281 3.3-V, 1.2-A, 6-MHz Miniature Step-Down DC-DC Converter for Wireless Connectivity Solutions

1 Features

- Operates from a Single Li-Ion Cell (3 V to 5.5 V)
- 6-MHz (typ.) PWM Switching Frequency
- Fixed Output Voltage: 3.3 V
- Up to 1.2-A Maximum Load Capability
- High Efficiency: 94% (typ.) with 3.8-V V_{IN} at 300 mA
- Analog Bypass: 60-mV (typ.) Drop-Out at 600 mA
- Low I_Q: 16 µA typical, 25 µA maximum
- Automatic ECO/PWM/Bypass Mode Change
- Forced PWM Mode for Low Output-Voltage Ripple
- Soft-Start Limits Input Current on Start-Up
- Current Overload Protection
- Thermal Overload Protection
- Small Total Solution Size: < 7.5 mm^2

2 Applications

- WLAN, WiFi Station Devices
- WiFi RF PC Cards
- Battery-Powered RF Devices

3 Description

The LM3281 is a high-efficiency low-noise miniature DC-DC converter optimized for powering noise-sensitive wireless connectivity chipsets and RF Front End Modules (FEMs) from a single Lithium-Ion cell. The LM3281 is ideal for “always on” applications with very low unloaded quiescent current of 16 µA (typ.).

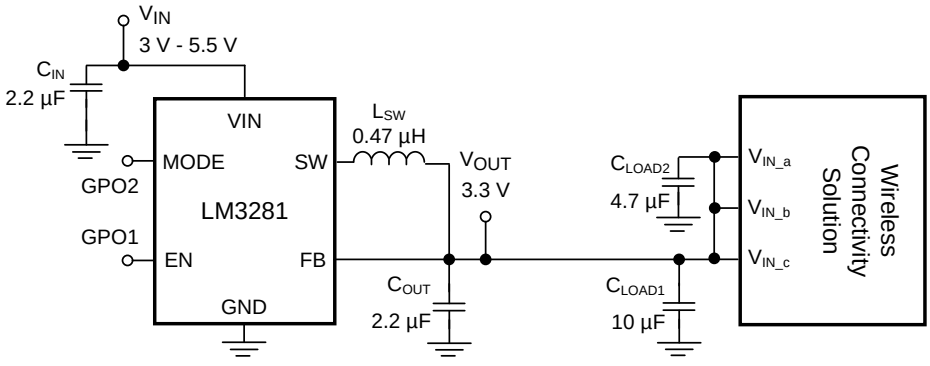
The LM3281 steps down an input supply voltage to a fixed output voltage of 3.3 V with output current up to 1200 mA. Five different modes of operation are used to optimize efficiency and minimize battery drain. In Pulse Width Modulation (PWM) mode, the device operates at a fixed frequency of 6 MHz which minimizes RF interference when driving medium-to-heavy loads. At light load, the device automatically enters into Economy (ECO) mode with reduced quiescent current. In a low-battery voltage condition, a bypass mode reduces the voltage dropout to 60 mV (typ.) at 600 mA. If very low output voltage ripple is desired at light loads, the device can also be forced into PWM mode. Shutdown mode turns the device off and reduces battery consumption to 0.1 µA (typ.).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
LM3281	DSBGA (6)	1.465 mm x 1.190 (MAX)

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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4 Revision History

DATE	REVISION	NOTES
November 2014	*	Initial release.

5 Pin Configuration and Functions

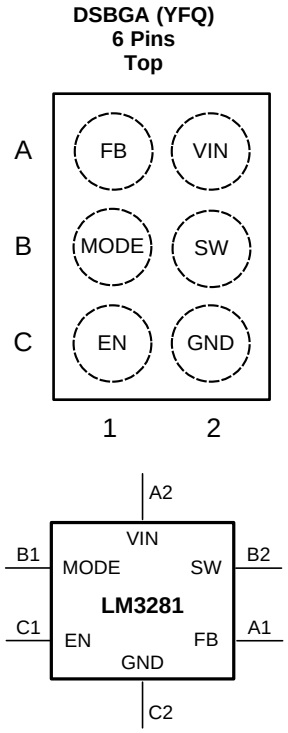


Figure 1. Pin Out

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	FB	Power	Connect to the output at the output filter capacitor C_{OUT} by lowest inductance path with a trace rated for 2 A.
A2	VIN	Power	Connect to input filter capacitor C_{IN} by lowest inductance path, then connect to supply voltage with a trace rated for 2 A.
B1	MODE	Logic	Selects automatic ECO/PWM mode or forced PWM mode. When MODE is HIGH the LM3281 automatically transitions between PWM and ECO operation. When MODE is LOW the LM3281 operates in PWM mode only. Do not leave MODE pin floating.
B2	SW	Power	Connect to inductor LSW with a trace rated for 2 A.
C1	EN	Logic	Set this digital input logic high for normal operation. For shutdown, set to logic low. Do not leave EN pin floating.
C2	GND	Ground	Connect to input filter capacitor C_{IN} by lowest inductance path, then to system ground by a very low inductance path.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

	MIN	MAX	UNIT
VIN pin to GND pin voltage	–0.2	6	V
EN, FB, MODE, SW pins to GND pin voltage	–0.2	V_{IN} + 0.2 or 6 (whichever is smaller)	
Junction temperature (T_J)		150	°C
Continuous power dissipation(3)	Internally limited		
Maximum lead temperature (soldering)		260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Internal thermal shutdown circuitry protects the device from permanent damage. It engages at T_J = 150°C (typ.) and disengages at T_J = 125°C (typ.).

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–1000	1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–250	250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage (with respect to GND pin)	3	5.5	V
I_{LOAD} (1)	Output current	0	1200	mA
I_{LOAD_BURST}(1)	Output current, short bursts (< 100 µS burst at < 10% duty cycle)	0	1400	
EN	EN pin voltage (with respect to GND pin)	0	V_{IN}	V
MODE	Mode select pin voltage (with respect to GND pin)	0	V_{IN}	
T_J	Junction temperature	–30	125	°C
T_A	Ambient temperature	–30	90	
T_B	PC board temperature	–30	105	

(1) Refer to section *High Maximum Current* in this data sheet for load current use case profile.

6.4 Thermal Information

THERMAL METRIC[1]		DSBGA YFQ 6 PINS	UNIT
$R_{\theta JA}$[2]	Junction-to-ambient thermal resistance	131.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	25.6	
ψ_{JT}	Junction-to-top characterization parameter	4.7	
ψ_{JB}	Junction-to-board characterization parameter	25.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) $R_{\theta JA}$ is not useful for CSP packages because the dominant heat loss mechanism is through the PCB. Instead, $R_{\theta JB}$ is more useful and is used.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) (1)(2)(3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range[4]		3		5.5	V
V_{OUT}	Output voltage measured at FB pin		3.2	3.3	3.4	
I_{SHDN_IN}	Total supply current in shutdown	EN = SW = FB = MODE = 0 V, Steady State		0.1	1	µA
I_{Q_OL}	Quiescent current	No switching		15	25	
F_{OSC}	Internal oscillator frequency		5.4	6	6.6	MHz
V_{IH}	EN, MODE pins high level input voltage		1.2			V
V_{IL}	EN, MODE pins low level input voltage				0.4	
I_{IH}	EN, MODE high level input current				1	µA
I_{IL}	EN, MODE low level input current	EN = MODE = 0 V	–1			

(1) All voltages are with respect to the GND pin.
(2) All characteristics apply to the *Simplified Schematic* with V_{IN} = 3.8 V, EN = MODE = VIN, at T_A = 25°C, device in PWM operation unless otherwise noted.
(3) Minimum (MIN) and Maximum (MAX) limits are specified by design, test, or statistical analysis over the ambient temperature operating range –30°C to 90°C. Limits are not specified by production testing.
(4) Device is functional at a minimum V_{IN} = 2.6 V but is specified for operation over the range V_{IN} = 3 V to 5.5 V.

6.6 System Characteristics[1][2][3][4]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LOAD_MAX}[5]	Maximum load current		1200			mA
$V_{O\_RIPPLE\_PWM}$	PWM mode V_{OUT} ripple	I_{LOAD} = 600 mA		1		mV
$V_{O\_RIPPLE\_ECO}$	ECO mode V_{OUT} ripple	I_{LOAD} = 30 mA		60		
$V_{O\_PWM\_ACC}$	PWM mode V_{OUT}	V_{IN} = 3.8 V	3.2	3.3	3.4	V
$V_{O\_ECO\_ACC}$	ECO mode V_{OUT}		3.2	3.3	3.4	
$I_{TRIG\_PWM\_TO\_ECO}$	PWM to ECO mode I_{LOAD} threshold	I_{LOAD} falling		50		mA
$I_{TRIG\_ECO\_TO\_PWM}$	ECO to PWM mode I_{LOAD} threshold	I_{LOAD} rising		70		
$V_{DROPOUT\_BYPASS}$	Bypass mode total dropout voltage with L_{SW} inductor DCR = 40 mΩ	I_{LOAD} = 600 mA, V_{IN} = 3.2V		60	80	mV
		I_{LOAD} = 1200 mA, V_{IN} = 3.2V		120	160	
$I_{ON\_SOFT\_START}$	Soft-start supply current during turnon averaged in any 10-µs window	EN = low-to-high, I_{LOAD} ≤ 1 mA		500	1000	mA
T_{ON}	Turnon transient time from EN = high until V_{OUT} is settled to within ±50 mV of settled value, and full 1200-mA load may be applied	EN = low-to-high, I_{LOAD} ≤ 1 mA			150	µs
η	PWM mode efficiency	I_{LOAD} = 1200 mA		89%		
		I_{LOAD} = 600 mA		93%		
		I_{LOAD} = 300 mA		94%		
	ECO mode efficiency	I_{LOAD} = 30 mA		91%		
I_{Q_CL}	Closed loop quiescent current	I_{LOAD} = 0 mA		16	25	µA
$V_{LINE\_TR\_PWM\_PWM}$[6]	PWM-to-PWM line transient response	I_{LOAD} = 600 mA V_{IN} = 4.2 V to 3.8 V V_{IN} = 3.8 V to 4.2 V with 7-µs edge rate		20		mVpk
$T_{LINE\_TR\_PWM\_PWM}$[7]				0[8]		µS
$V_{LOAD\_TR\_PWM\_PWM}$[6]	PWM-to-PWM load transient response	I_{LOAD} = 150 mA to 600 mA or I_{LOAD} = 600 mA to 150 mA with 1-µs edge rate, V_{IN} = 3.8 V		80		mVpk
$T_{LOAD\_TR\_PWM\_PWM}$[7]				3		µS
$V_{LOAD\_TR\_ECO\_TO\_PWM}$[6]	ECO-to-PWM load transient response	I_{LOAD} = 30 mA to 600 mA with 1-µs edge rate, V_{IN} = 3.8 V		200		mVpk
$T_{LOAD\_TR\_ECO\_TO\_PWM}$[7]				6		µS
V_{IN_RAMP}[9]	Input voltage ramp time	I_{LOAD} = 0 mA Input power supply rising from 1.2 V to 2.6 V			20	µs

(1) All voltages are with respect to the GND pin.
(2) All TYP characteristics apply to the *Simplified Schematic* with V_{IN} = 3.8 V, EN = MODE = VIN, at T_A = 25°C, device in PWM operation, unless otherwise noted and assume the following passive components:
  (a) C_{IN} = C_{OUT} = Samsung 2.2 µF 0201 case size (PN: CL03A225MQ3CRNC)
  (b) L_{SW} = Murata 0.47 µH 2012 case size (PN: LQM21PNR47MGH)
  (c) C_{LOAD1} = Samsung 10 µF 0402 case size (PN: CL05A106MP5NUNC)
  (d) C_{LOAD2} = Samsung 4.7 µF 0402 case size (PN: CL05A475MP5NRNC)
(3) All system characteristics are specified by design, test or statistical analysis and are not specified by production testing.
(4) Minimum (MIN) and Maximum (MAX) limits apply over the ambient temperature operating range –30°C to 90°C and over the V_{IN} range 3 V to 5.5 V, unless otherwise noted.
(5) Refer to section *High Maximum Current* in this data sheet for load current use case profile.
(6) Transient magnitude is defined as maximum deviation from final settled value during transient time.
(7) Transient time is defined as time elapsed from the start of the event to when V_{OUT} is finally within ±50 mV of settled value.
(8) Transient magnitude does not exceed ± 50 mV of settled value, so transient time is 0 µS.
(9) This parameter is only applicable when EN is tied to VIN. See *Power-On Reset* section for further details.

6.7 Typical Characteristics

All curves are at T_A = 25°C and V_{IN} = 3.8 V, unless otherwise specified. C_{IN}, C_{OUT} = 2.2 µF, C_{LOAD2} = 4.7 µF, C_{LOAD1} = 10 µF, L_{SW} = 0.47 µH.

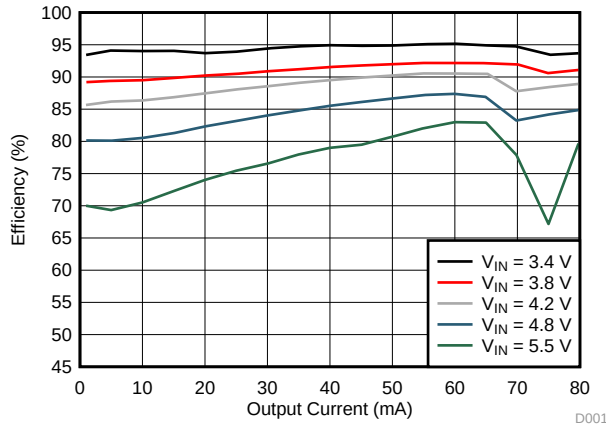


Figure 2. ECO Efficiency vs Output Current

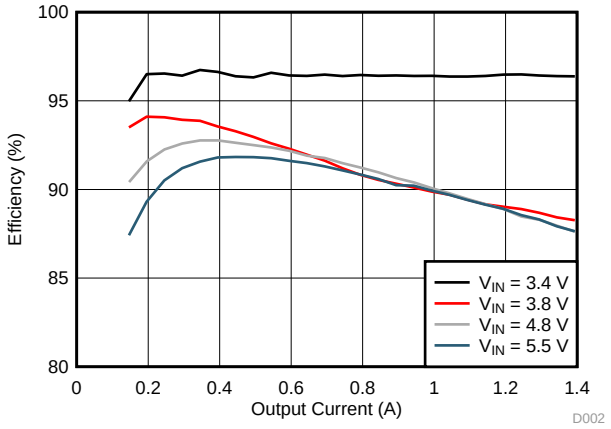


Figure 3. PWM Efficiency vs Output Current

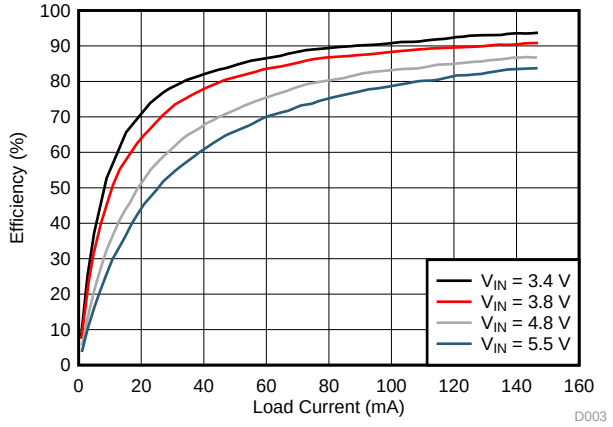


Figure 4. Forced PWM Efficiency vs Output Current

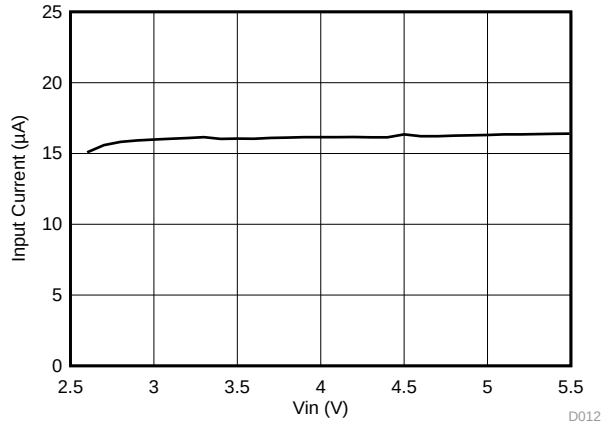


Figure 5. No Load ECO Input Current vs V_{IN}

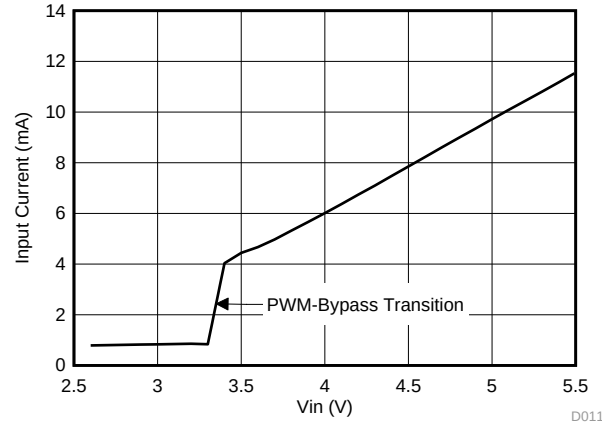
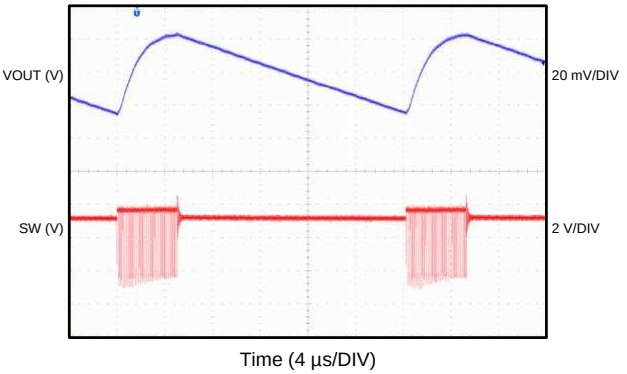


Figure 6. No Load Forced PWM Input Current vs V_{IN}

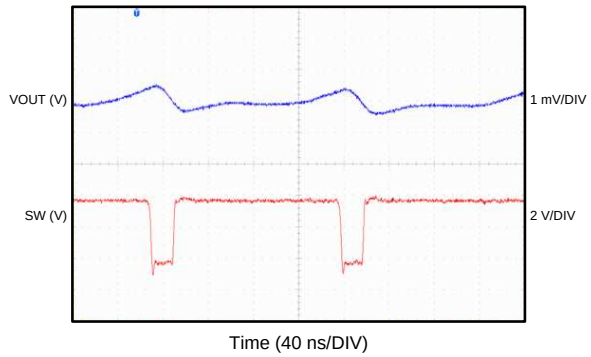


I_{OUT} = 10 mA

Figure 7. Output Voltage Ripple in ECO Mode

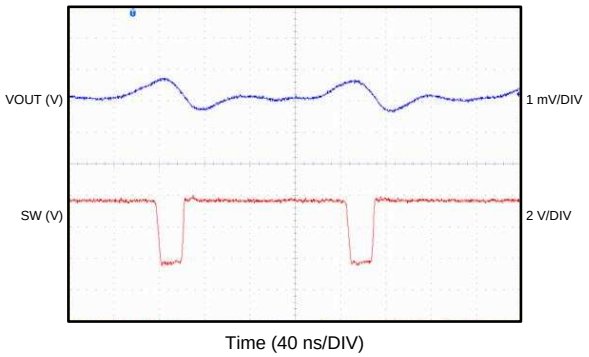
Typical Characteristics (continued)

All curves are at T_A = 25°C and V_{IN} = 3.8 V, unless otherwise specified. C_{IN}, C_{OUT} = 2.2 µF, C_{LOAD2} = 4.7 µF, C_{LOAD1} = 10 µF, L_{SW} = 0.47 µH.



I_{OUT} = 100 mA

Figure 8. Output Voltage Ripple in PWM Mode



I_{OUT} = 10 mA

Figure 9. Output Voltage Ripple in Forced PWM Mode

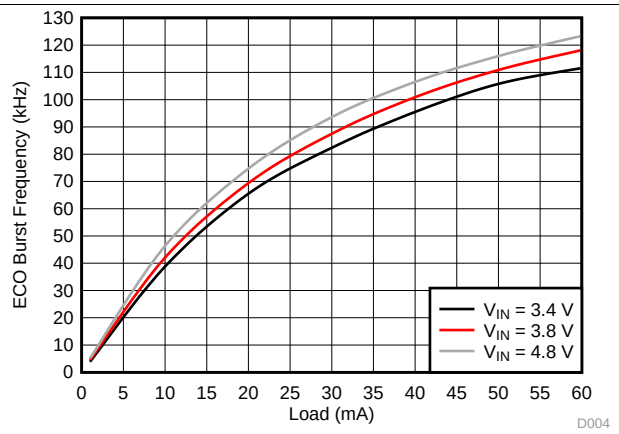


Figure 10. ECO Burst Frequency vs Output Current

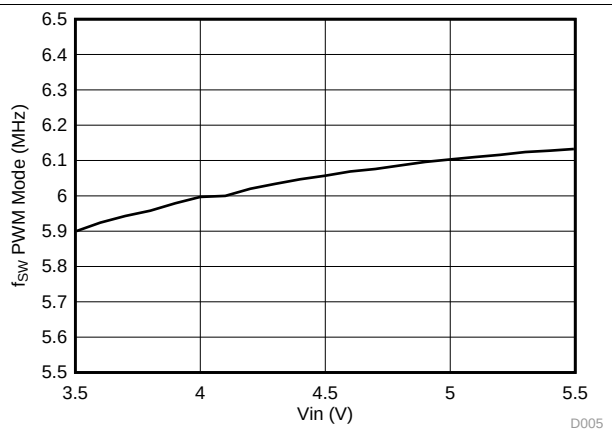


Figure 11. PWM Switching Frequency vs V_{IN}

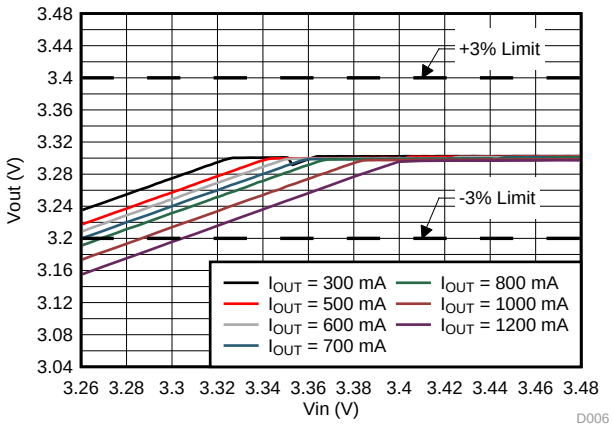


Figure 12. PWM-to-Analog Bypass Transition, Falling V_{IN}

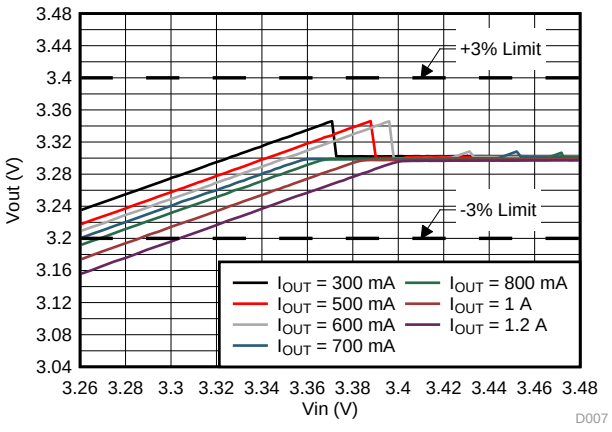


Figure 13. Analog Bypass-to-PWM Transition, Rising V_{IN}

Typical Characteristics (continued)

All curves are at T_A = 25°C and V_{IN} = 3.8 V, unless otherwise specified. C_{IN}, C_{OUT} = 2.2 µF, C_{LOAD2} = 4.7 µF, C_{LOAD1} = 10 µF, L_{SW} = 0.47 µH.

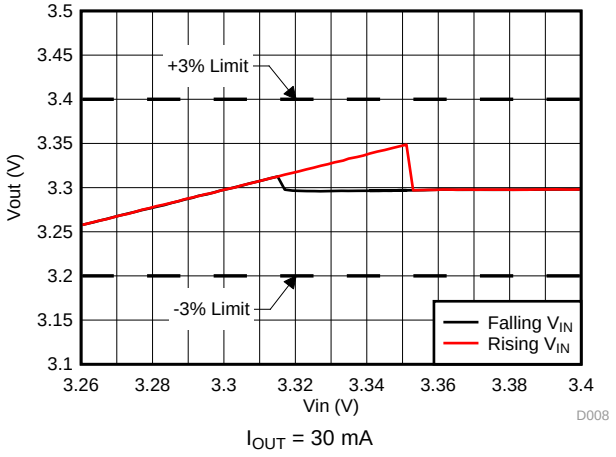


Figure 14. Analog Bypass Transition at Light Load vs V_{IN}

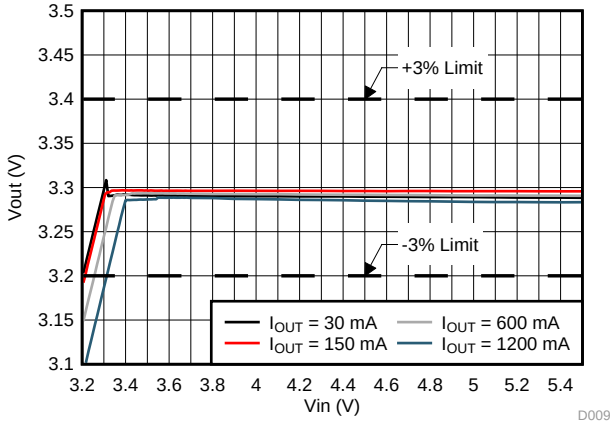


Figure 15. Line Regulation vs Output Current

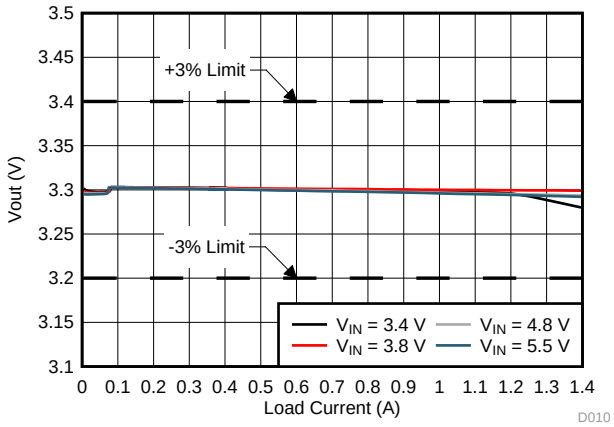


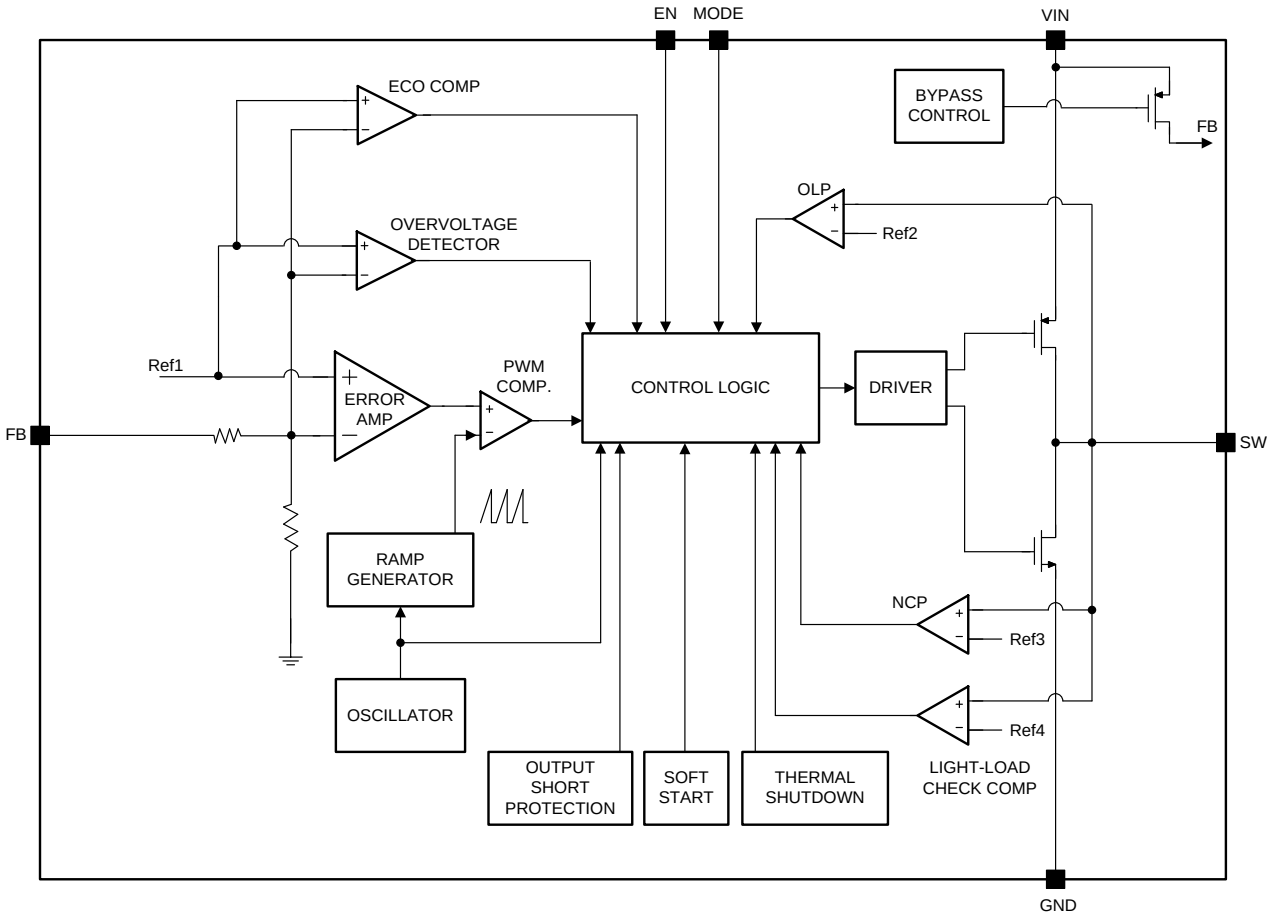
Figure 16. Load Regulation vs Output Current

7 Detailed Description

7.1 Overview

The LM3281 is a size- and performance-optimized step-down DC-DC converter for powering power amplifiers, front-end modules, wireless connectivity solutions, and a wide variety of other applications. The device complements the portfolio of SuPA (Supply for PA) products by combining small solution size, low dropout analog bypass with smooth mode transitions, very low standby current for always-on applications, very low ripple with “forced PWM” mode operation, high maximum output current, ability to drive large load capacitance while retaining transient performance, and soft start to limit start-up current.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Small Solution Size

Solution size less than 7.5 mm^2 is possible using the LM3281 in combination with only three small passive components.

7.3.2 Automatic Analog Bypass with Low Dropout

An internal bypass transistor under analog control automatically engages as V_{IN} falls below the V_{OUT} target. Output stays regulated in analog bypass mode until full dropout. The parallel impedance of this additional bypass transistor with normal DC-DC output path reduces V_{OUT} voltage drop-out, maximizing V_{OUT} supply voltage to the load at low V_{IN} conditions. The analog implementation provides a smooth transition among regulation and bypass modes, avoiding V_{OUT} distortion.

Feature Description (continued)

7.3.3 Low I_Q

An ECOnomy (ECO) mode of operation draws 16 µA (typ.) quiescent current, permitting the LM3281 to be used in “always-on” applications. This low I_Q is achieved over the entire input supply range of 5.5 V to 2.6 V, irrespective of whether LM3281 is operating in regulation (ECO Mode or Analog Bypass mode) or in full dropout (full bypass).

7.3.4 Forced PWM Operation

ECO mode provides low I_Q while PWM mode optimizes output voltage ripple and transient performance. When high, the MODE pin permits automatic mode selection based on load current. When MODE is pulled low the LM3281 enters “forced PWM” operation with very low ripple and optimized transient response. Alternately, the MODE pin can be tied high in an application to allow the device to always select a mode of operation automatically.

7.3.5 High Maximum Current

Load current of 1.2 A is supported with short bursts (of < 100 µS with < 10% duty cycle) up to 1.4 A.

A wide variety of load current use cases are accommodated by the LM3281. Examples are described in Table 1 and Table 2: one for high ambient temperature all the time, and one for a more typical ambient temperature use case. Many alternate use case scenarios are available; please contact TI to discuss the load current relevant for a given application.

For the high ambient temperature of 85°C for the entire device operational lifetime, see Table 1:

Table 1. I_{LOAD} Example for Constant 85°C Ambient Temperature

I_{LOAD}	AMBIENT TEMPERATURE	PERCENT OPERATIONAL LIFETIME
100 mA	85°C	Up to 100%
700 mA	85°C	Up to 60%
1400 mA	85°C	Up to 3%

For a more typical ambient temperature distribution of $T_A \le 70°C$ for ≥ 80% of the operational lifetime and $70°C < T_A \le 85\%$ for ≤ 20% of the operational lifetime, see Table 2:

Table 2. I_{LOAD} Example for a More Typical Ambient Temperature Use

I_{LOAD}	AMBIENT TEMPERATURE	PERCENT OPERATIONAL LIFETIME
100 mA	$70°C < T_A \le 85°C$ for ≤ 20% of time $T_A \le 70°C$ for ≥ 80% of time	Up to 100%
850 mA	$70°C < T_A \le 85°C$ for ≤ 20% of time $T_A \le 70°C$ for ≥ 80% of time	Up to 60%
1400 mA	$70°C < T_A \le 85°C$ for ≤ 20% of time $T_A \le 70°C$ for ≥ 80% of time	Up to 3%

7.3.6 High-Capacitance Load and Line Transient Performance

The LM3281 is internally compensated to drive loads with large bypass capacitance, including transceiver modules, without sacrificing transient performance. Please reference *Total Effective Output Capacitance (C_{OUT} + C_{LOAD1} + C_{LOAD2})* regarding output capacitance requirements.

7.3.7 Soft Start

During start-up a soft-start feature prevents high input current which could cause supply voltage bus drops and interfere with other subsystems sharing the supply bus. Soft start is especially valuable in applications where large load capacitance must be charged on start-up. Loading of the output during start-up condition will extend the soft-start time. Excessive loading may even prevent the output from reaching the target voltage, and the device may therefore stay in the soft-start condition indefinitely.

7.3.8 Thermal Overload Protection

The LM3281 device has a thermal overload protection that protects the device from short-term misuse and overload conditions. If the junction temperature exceeds 150°C, the LM3281 shuts itself down. Normal operation resumes after the temperature drops below 125°C. Prolonged operation in thermal overload condition may damage the device and is therefore not recommended.

7.3.9 Current Limit

The current limit feature allows the LM3281 to protect itself and external components during overload conditions. In PWM mode, the cycle-by-cycle current limit of the SW pin is 1.9-A peak, and the bypass current limit is 1.3 A. Thus, the total current limit is 2.2 A (typ.). During the start-up condition or when the output voltage is less than 0.34 V, the SW pin current limit is reduced to 0.85 A peak, and the bypass current is disabled. If excessive load prevents the output from rising above 0.34 V for more than 40 µs, the LM3281 enters the short-circuit-protection state.

7.3.10 Power-On Reset

Some applications may require tying the EN pin directly to the VIN pin. For this reason, the LM3281 features a Power on Reset (POR) that ensures that the part will enter a deterministic state when power is first applied. When the EN pin is tied directly to the VIN pin, the input power supply needs to rise fast enough for the POR circuit to work properly. The V_{IN} voltage should not stay between 1.2 V and 2.6 V for longer than 20 µs. This is not required if the EN pin voltage remains below V_{IL} (below 0.2 V) until V_{IN} is at least at 2.6 V.

7.4 Device Functional Modes

The LM3281 includes five steady-state modes of operation depending on MODE, V_{IN}, and I_{LOAD} conditions: PWM (Pulse Width Modulation), Forced PWM, ECO (ECOnomy), Analog Bypass, and Shutdown. Two protection mechanisms include current limiting and thermal overload protection. Finally, soft-start operation is active to prevent excessive input current only when the part is first enabled.

7.4.1 PWM Mode

When the LM3281 operates in PWM mode, the switching frequency is constant, and the switcher regulates the output voltage by changing the energy per cycle to support the load required. During the first portion of each switching cycle, the control block in the LM3281 turns on the internal PFET switch. This allows current to flow from the input through the inductor and to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of $(V_{IN} – V_{OUT})/L$, by storing energy in its magnetic field. During the second portion of each cycle, the control block turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET and to the output filter capacitor and load, which ramps the inductor current down with a slope of $–V_{OUT}/L$. The output filter capacitor stores charge when the inductor current is greater than the load current and releases it when the inductor current is less than the load current, smoothing the voltage across the load. At the next rising edge of the clock, the cycle repeats. An increase of load pulls the output voltage down, increasing the error signal. As the error signal increases, the peak inductor current becomes higher, thus increasing the average inductor current. The output voltage is therefore regulated by modulating the PFET switch on-time to control the average current sent to the load. The circuit generates a duty-cycle modulated rectangular signal that is averaged using a low pass filter formed by the inductor and output capacitor. The output voltage is equal to the average of the duty-cycle modulated rectangular signal.

7.4.2 Forced PWM (FPWM) Mode

To maintain high efficiency at lighter loads, LM3281 automatically goes into what is called ECO mode which has low I_Q but higher ripple compared to PWM mode. If an application requires very low ripple and/or fast transient response, LM3281 can be forced to operate in PWM mode even at lighter loads. When high, the MODE pin permits automatic PWM or ECO mode operation based on load current. When MODE is pulled low the LM3281 enters “forced PWM” operation with very low ripple and optimized transient response. If automatic PWM/ECO mode operation is desired, the MODE pin can be permanently tied high in an application to allow the device to always select a mode of operation automatically based on the load current conditions.

It should be noted that LM3281 transient performance is quite good in ECO mode, and it may not be necessary to operate in FPWM mode for transient performance reasons alone. Normally, FPWM operation is selected for lower output voltage ripple.

Device Functional Modes (continued)

7.4.3 Analog Bypass Mode

The LM3281 contains an internal BPFET (Bypass FET) transistor connected from the battery directly to the output for bypassing the PWM DC-DC converter when V_{IN} approaches V_{OUT}. In Analog Bypass mode, this BPFET is turned on just enough for the PWM DC-DC to maintain regulation by providing a parallel path from the battery directly to the load for maximum usable battery range and extended operating time while maintaining regulation. When the part is in dropout and is operating in full bypass mode, the output voltage will be the input voltage less the voltage drop across the resistance of the BPFET in parallel with the PFET + Switch Inductor. Analog Bypass mode is more efficient than operating in PWM mode at 100% duty cycle because the combined resistance of the circuit is significantly less than the series resistance of just the PWM PFET and inductor. This translates into higher voltage available at the output in Analog Bypass mode for a given battery voltage. The bypass operation is very system resource friendly in that the bypass PFET is gradually turned on automatically when the input voltage gets close to the output voltage (while always maintaining regulation), a typical scenario of a discharging battery. Likewise, it is also automatically gradually turned off when the input voltage rises, a typical scenario when connecting a charger.

7.4.4 ECO (Economy) Mode

At light load current, the converter enters ECO mode operation with reduced quiescent supply current to maintain high efficiency. During ECO mode operation, a switching burst brings the output just above target voltage. This period of switching is followed by no switching in which the output coasts to just below target voltage, and then this cycle is repeated. The frequency of how often the switching burst occurs is dependent on the load current. PWM operation resumes once the load current reaches a specific threshold.

7.4.5 Shutdown Mode

Setting the EN digital input pin low (< 0.4 V) places the LM3281 in Shutdown mode where it consumes less than 0.1 µA current typically. In shutdown, the PFET switch, the NFET synchronous rectifier, the BPFET, reference voltage source, control, and bias circuitry of the LM3281 are turned off. Setting EN high (> 1.2 V) enables normal operation.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM3281 is a high efficiency DC-DC converter optimized to power Wireless Connectivity Solutions in cell phones, portable communication devices or other battery-powered RF devices. The device is designed to operate from an input supply voltage between 3 V and 5.5 V with a maximum load current of 1.2 A. It operates in PWM mode for medium to heavy load conditions and in ECO mode for light load conditions to optimize for best efficiency , transient performance and output voltage ripple at varying load conditions. In PWM mode the LM3281 converter operates with nominal switching frequency of 6 MHz, thus enabling use of smaller size capacitors and inductor. The converter operates in ECO mode at lighter load conditions to maintain high efficiency. In this mode a period of switching burst charges the output capacitor to the regulation target. This is followed by a period of no switching where the output voltages coasts to a lower voltage threshold due to light load current consumption. Upon reaching this lower voltage threshold, the cycle repeats by starting a new switching burst. The LM3281 automatically transitions into Analog Bypass operation as input voltage approaches output voltage.

Figure 17 shows one of many application configurations for LM3281. A battery-connected system boost bypass (normally part of system PMU) provides input supply to LM3281 which in turn very efficiently converts this input to a fixed 3.3-V output with superior transient response and output noise, thereby saving the Wireless Connectivity Solution from having to operate from a higher supply voltage, such as a direct connection to a battery or a system boost/bypass. This results in significant power dissipation savings and consequently cooler operation for the connectivity solution without sacrificing its RF performance. In applications where low voltage battery operation is not a significant feature, system boost/bypass can be eliminated, and the LM3281 can be directly connected to a battery for high efficiency power conversion and excellent RF performance. These types of always-on applications are feasible because of very low I_Q of LM3281.

8.2 Typical Application

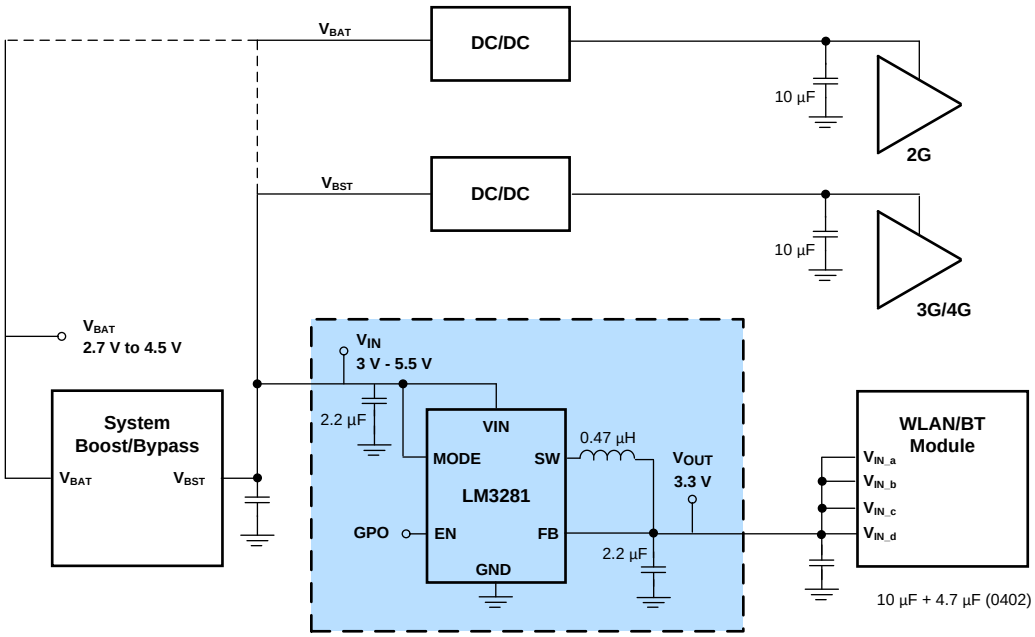


Figure 17. LM3281 Typical Application

Typical Application (continued)

8.2.1 Design Requirements

Design requirements for LM3281 pertain to the use of appropriate passive components. The recommended passive components (inductors and capacitors) are optimally selected to provide best performance for a typical application.

8.2.1.1 Suggested Passive Components

Referencing the *Simplified Schematic* on page 1, the *LM3281 Inductor Selection*, *Total Effective Output Capacitance (C_{OUT} + C_{LOAD1} + C_{LOAD2})*, *LM3281 Capacitor (C_{IN} and C_{OUT}) Selection*, *Recommended Load Bypass Capacitors (C_{LOAD1} and C_{LOAD2})*, and *Alternate Output Capacitor Configuration* sections provide suggested passive components. Please consult the TI applications team to select suitable alternatives.

8.2.1.1.1 LM3281 Inductor Selection

The solution inductor shown in the *Simplified Schematic* can be optimized for size or solution efficiency. The 2012-size inductor listed below will perform well but other suitable smaller size inductors may be available in the future.

Table 3. Suggested Inductor

	INDUCTANCE	DCR	ISAT	SIZE	PART NUMBER	VENDOR
LSW	0.47 µH ± 20%	40 mΩ	2.4 A	2.00 x 1.25 x 1.00 mm	LQM21PNR47MGH	Murata

The inductor used in LM3281 designs should have following characteristics over operating temperature range:

- DC resistance (DCR) ≤ 70 mΩ
- Inductance at 0-mA current = 0.47 µH ±20%
- Inductance at 1.4-A current ≥ 0.29 µH
- Inductance at 2-A current ≥ 0.26 µH

If an application requires less than 1.4A peak load current, it is possible to trade maximum load current for DCR of the inductor (hence smaller physical size) by using Equation 1:

$$DCR\_IND\_MAX = (0.217/I\_MAX) - 0.085 \quad (1)$$

where DCR_IND_MAX is the maximum DC resistance of inductor in Ohms and I_MAX is the maximum load current in Amperes.

8.2.1.1.2 Total Effective Output Capacitance (C_{OUT} + C_{LOAD1} + C_{LOAD2})

Total effective output capacitance including load capacitance (C_{LOAD1} and C_{LOAD2}) and solution capacitance (C_{OUT}), de-rated for 3.3-V DC bias, operating temperature range, aging, etc. **must be 3.4 µF to 9 µF**.

Table 4. Total Effective Output Capacitance

	MIN	TYP	MAX	UNIT
Effective C_{OUT} (capacitor placed closest to LM3281), de-rated for 3.3-V DC bias, operating temperature and aging	0.8		9	µF
Total effective output capacitance (C_{OUT} + C_{LOAD1} + C_{LOAD2}), de-rated for 3.3-V DC bias, operating temperature range, and aging	3.4	7	9	µF

8.2.1.1.3 LM3281 Capacitor (C_{IN} and C_{OUT}) Selection

The LM3281 is designed for use with ceramic capacitors for its input and output filters. Ceramic capacitors types such as X5R, X7R are recommended for both filters. Note that suggested LM3281 solution capacitors are de-rated by 50% to 65% at 3.3-V DC bias.

Table 5. Suggested Capacitors

	CAPACITANCE	CAPACITANCE @3.3V DC BIAS	SIZE (IMPERIAL)	PART NUMBER	VENDOR
C_{IN}	2.2 µF ± 10%	1.1 µF	0402, 0.50 mm height	CL05A225KQ5NNNC	Samsung
C_{OUT}					
C_{IN}	2.2 µF ± 20%	0.8 µF	0201, 0.30 mm height	CL03A225MQ3CRNC	Samsung
C_{OUT}					

8.2.1.1.4 Recommended Load Bypass Capacitors (C_{LOAD1} and C_{LOAD2})

Suggested load capacitors are de-rated by 55% to 60% at 3.3-V DC bias. Contact TI for additional recommendations regarding load bypass capacitor value and case sizes.

Table 6. Recommended Load Capacitors

	CAPACITANCE	CAPACITANCE @3.3V DC BIAS	SIZE (IMPERIAL)	PART NUMBER	VENDOR
C_{LOAD1}	10 µF ± 20%	4.2 µF	0402, 0.50 mm height	CL05A106MP5NUNC	Samsung
C_{LOAD1}	10 µF ± 10%	5.2 µF	0603, 0.80 mm height	CL10A106KP8NNNC	Samsung
C_{LOAD2}	4.7 µF ± 20%	2 µF	0402, 0.50 mm height	CL05A475MP5NRNC	Samsung

8.2.1.1.5 Alternate Output Capacitor Configuration

If only one output capacitor is desired for minimum system solution size components in Table 7 can be used. In this case components C_{OUT}, C_{LOAD1}, and C_{LOAD2} are absorbed into C_{OUT}; C_{LOAD1} and and C_{LOAD2} are eliminated. C_{OUT} must be placed very close to the LM3281.

Table 7. Other Recommended Capacitors

	CAPACITANCE	CAPACITANCE @3.3V DC BIAS	SIZE (IMPERIAL)	PART NUMBER	VENDOR
C_{OUT}	22 µF ± 20%	7.3 µF	0603, 0.80 mm height	GRM188R60J226MEA0D	Murata

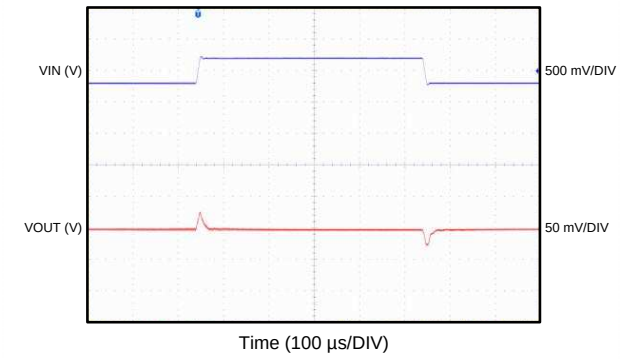
8.2.2 Detailed Design Procedure

The LM3281 is designed to use ceramic capacitors for its input and output filters. Use a 2.2-µF capacitor for input that provides a minimum of 0.8 µF effective capacitance under bias and worst-case temperature conditions. For output filter, combination of C_{OUT}, C_{LOAD1} and C_{LOAD2} should yield at least 3.4 µF (but not more than 9 µF) of effective capacitance under bias and worst-case temperature conditions. Please refer to Table 5, Table 6, and Table 7 for specific recommended components.

The input filter capacitor supplies AC current drawn by the PFET switch of the LM3281 in the first part of each cycle and reduces the voltage ripple imposed on the input power source. The output filter capacitor absorbs the AC inductor current, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficiently low ESR (Equivalent Series Resistance) to perform these functions. The ESR of the filter capacitors is generally a major factor in voltage ripple.

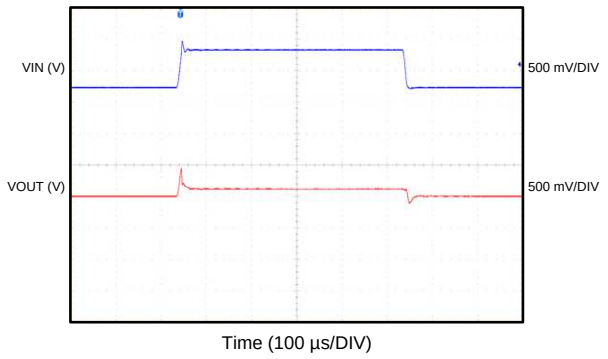
There are two main considerations when choosing an inductor: the inductor should not saturate (inductance should not drop significantly with current), and DC resistance of the inductor should not be excessively high. Different manufacturers follow different saturation current rating specifications, so attention must be given to details. Saturation current ratings are typically specified at 25°C so ratings over the ambient temperature range of the application should be requested from the manufacturer. Refer to *LM3281 Inductor Selection* for a recommendation about a specific part number and other useful guidelines about inductor selection.

8.2.3 Application Curves



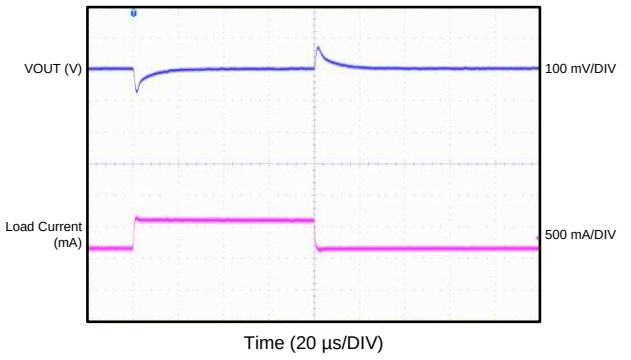
3.8 V → 4.2V → 3.8 V I_{OUT} = 600 mA

Figure 18. Line Transient Response



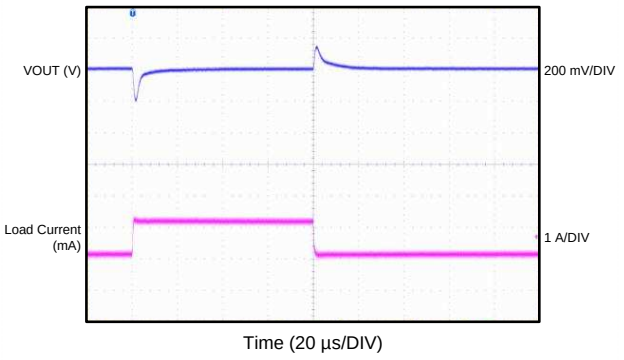
3.2 V → 3.8 V → 3.2 V I_{OUT} = 600 mA

Figure 19. Line Transient Response: Bypass Region



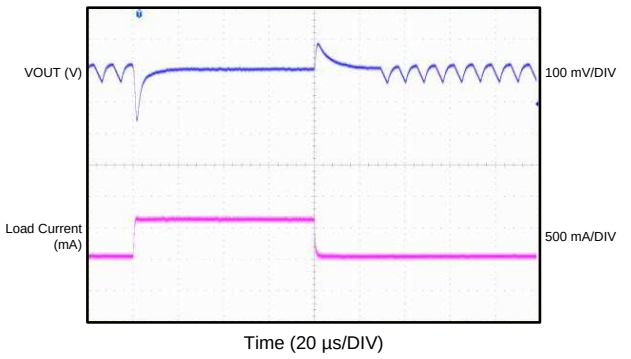
PWM-PWM 150 mA → 600 mA → 150 mA

Figure 20. Load Transient Response



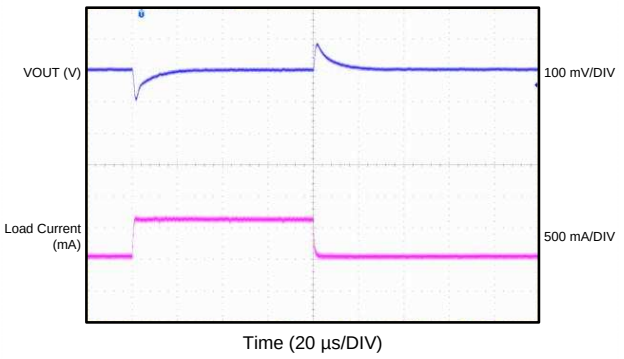
PWM-PWM Heavy Step 150 mA →1200 mA → 150 mA

Figure 21. Load Transient Response



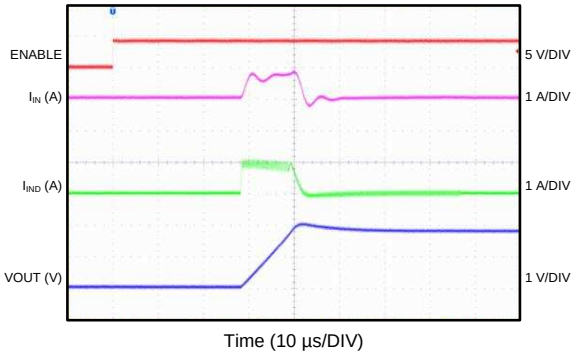
ECO-PWM-ECO 30 mA → 600 mA → 30 mA

Figure 22. Load Transient Response



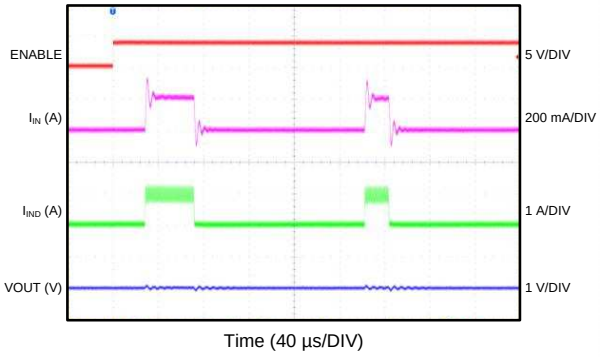
Forced PWM 30 mA → 600 mA → 30 mA

Figure 23. Load Transient Response



I_{OUT} = 1 mA

Figure 24. Start-Up Response



Output shorted to Ground

Figure 25. Start-Up into Short-Circuit Response

9 Power Supply Recommendations

The LM3281 device is designed to operate from a supply voltage range between 3 V and 5.5 V. This input supply should be well regulated. If the input supply is located more than a few inches from the LM3281 converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

10 Layout

10.1 Layout Guidelines

Optimal LM3281 performance is realized when two important layout considerations are observed. TI-provided layout guidance in this section illustrates best practices, and a customer layout review with the TI applications team will ensure best performance is achieved.

10.1.1 C_{OUT}-to-C_{LOAD} Inductance

Minimize inductance in the path between LM3281 C_{OUT} capacitor and the load bypass capacitors C_{LOAD1} and C_{LOAD2} for best performance. Total power path inductance from the LM3281 output to the load (including vias and traces) should target < 1 nH and must not exceed 2 nH.

10.1.2 LM3281-to-C_{IN} Inductance

Minimize inductance between LM3281 pins (VIN, GND) and the LM3281 input bypass capacitor C_{IN} for best performance. The LM3281 device and C_{IN} capacitor should be placed to permit shortest possible top-metal routing for these connections.

Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces resulting in poor regulation or instability. Poor layout can also result in re-flow problems leading to poor solder joints between the DSBGA package and board pads which can result in erratic or degraded performance of the converter. By its very nature, any switching converter generates electrical noise, and the circuit board designer's challenge is to minimize, contain, or attenuate such switcher-generated noise. A high-frequency switching converter, such as the LM3281, switches Ampere level currents within nanoseconds, and the traces interconnecting the associated components can act as radiating antennas. The following general guidelines are offered to help mitigate EMI and facilitate good layout design.

- Place the LM3281 switcher, its input capacitor, and output filter inductor and capacitor close together, and make the Inter-connecting traces as short as possible.
- Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle, current flows from the input filter capacitor, through the internal PFET of the LM3281 and the inductor, to the output filter capacitor, then back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground, through the internal synchronous NFET of the LM3281 by the

Layout Guidelines (continued)

inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.

- Make the current loop area(s) as small as possible.
- Reduce the amount of switching current that circulates through the ground plane: Connect the ground bump of the LM3281 and its input filter capacitor together using generous component-side copper fill as a pseudo-ground plane. Then connect this copper fill to the system ground-plane (if one is used) with multiple vias. These multiple vias help to minimize ground bounce at the LM3281 by giving it a low-impedance ground connection.
- Minimize resistive losses by using wide traces between the power components and doubling up traces on multiple layers when needed.
- Route noise sensitive traces, such as the voltage feedback path, as directly as possible from the switcher FB pad to the VOUT pad of the output capacitor, but keep it away from noisy traces between the power components.
- Take advantage of the inherent inductance of circuit traces to reduce coupling among various function blocks on the board, by way of the power supply traces.

10.2 Layout Example

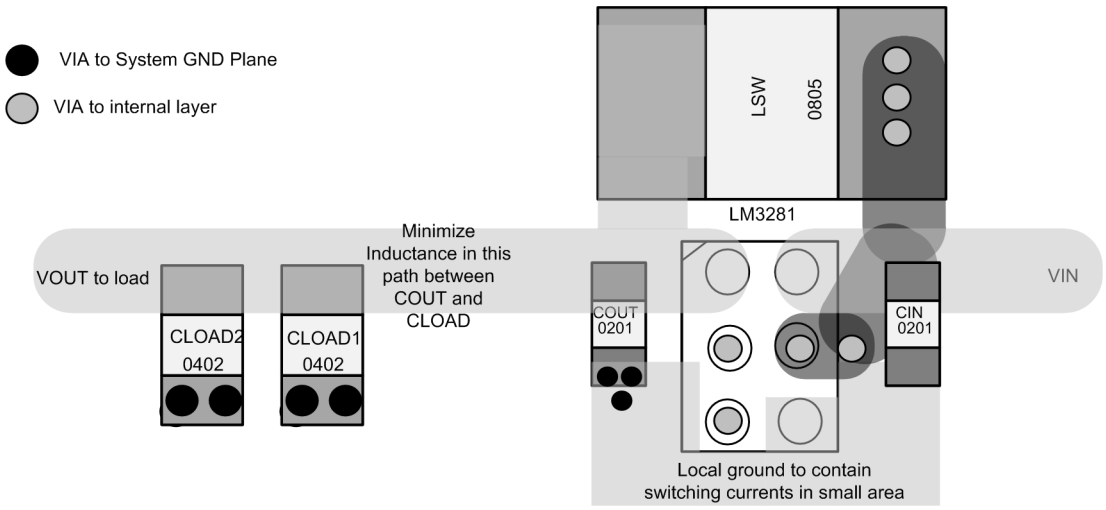


Figure 26. LM3281 Layout Example

10.3 DSBGA Package Assembly And Use

Use of the DSBGA package requires specialized board layout, precision mounting, and careful re-flow techniques, as detailed in Texas Instruments Application Note 1112 *DSBGA Wafer Level Chip Scale Package* (SNVA009). Refer to the section Surface Mount Technology (SMD) Assembly Considerations. For best results in assembly, alignment ordinals on the PC board should be used to facilitate placement of the device. The pad style used with DSBGA package should be the NSMD (non-solder mask defined) type. This means that the solder-mask opening is larger than the pad size. This prevents a lip that otherwise forms if the solder-mask and pad overlap from holding the device off the surface of the board and interfering with mounting. See Application Note 1112 for specific instructions how to do this.

The DSBGA package is optimized for the smallest possible size in applications with red or infrared opaque cases. Because the DSBGA package lacks the plastic encapsulation characteristic of larger devices, it is vulnerable to light. Backside metallization and/or epoxy coating, along with front-side shading by the printed circuit board, reduce this sensitivity. However, the package has exposed die edges. In particular, DSBGA devices are sensitive to light (in the red and infrared range) shining on the package's exposed die edges.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

Texas Instruments Application Note 1112 *DSBGA Wafer Level Chip Scale Package* (SNVA009).

11.3 Trademarks

All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3281YFQR	ACTIVE	DSBGA	YFQ	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-30 to 90	SN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

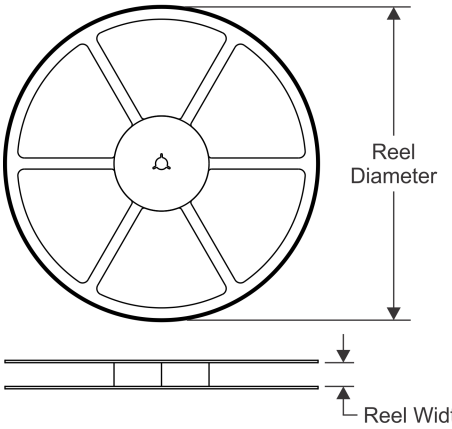
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

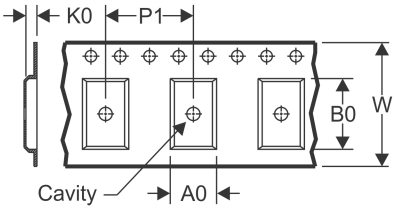
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

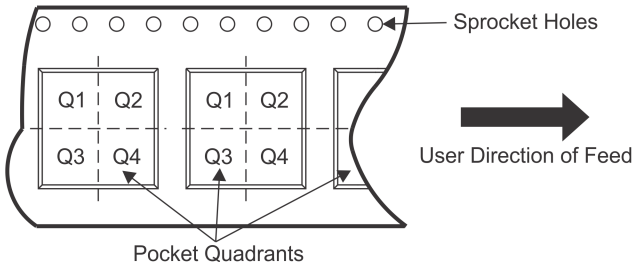


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

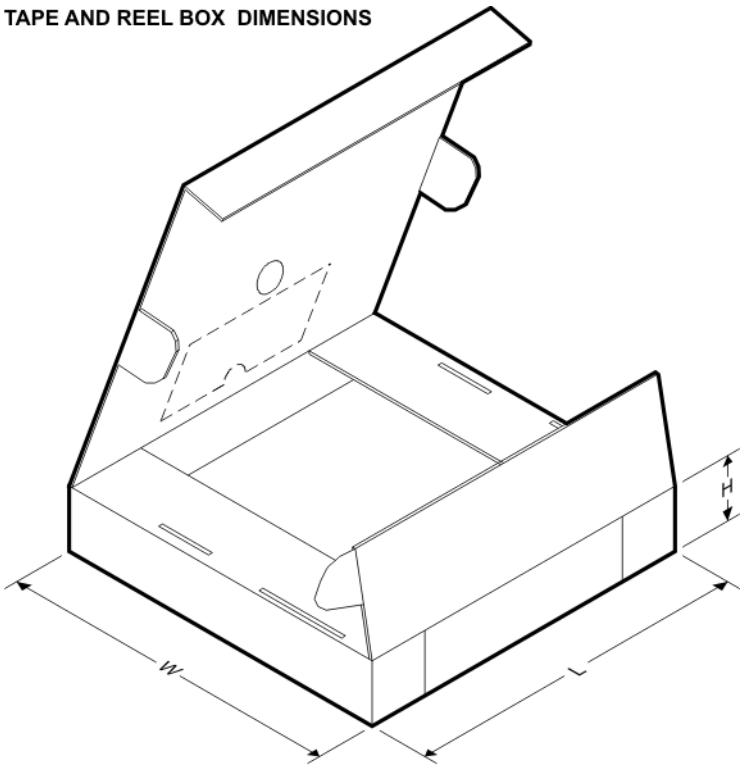
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3281YFQR	DSBGA	YFQ	6	3000	178.0	8.4	1.29	1.56	0.76	4.0	8.0	Q1

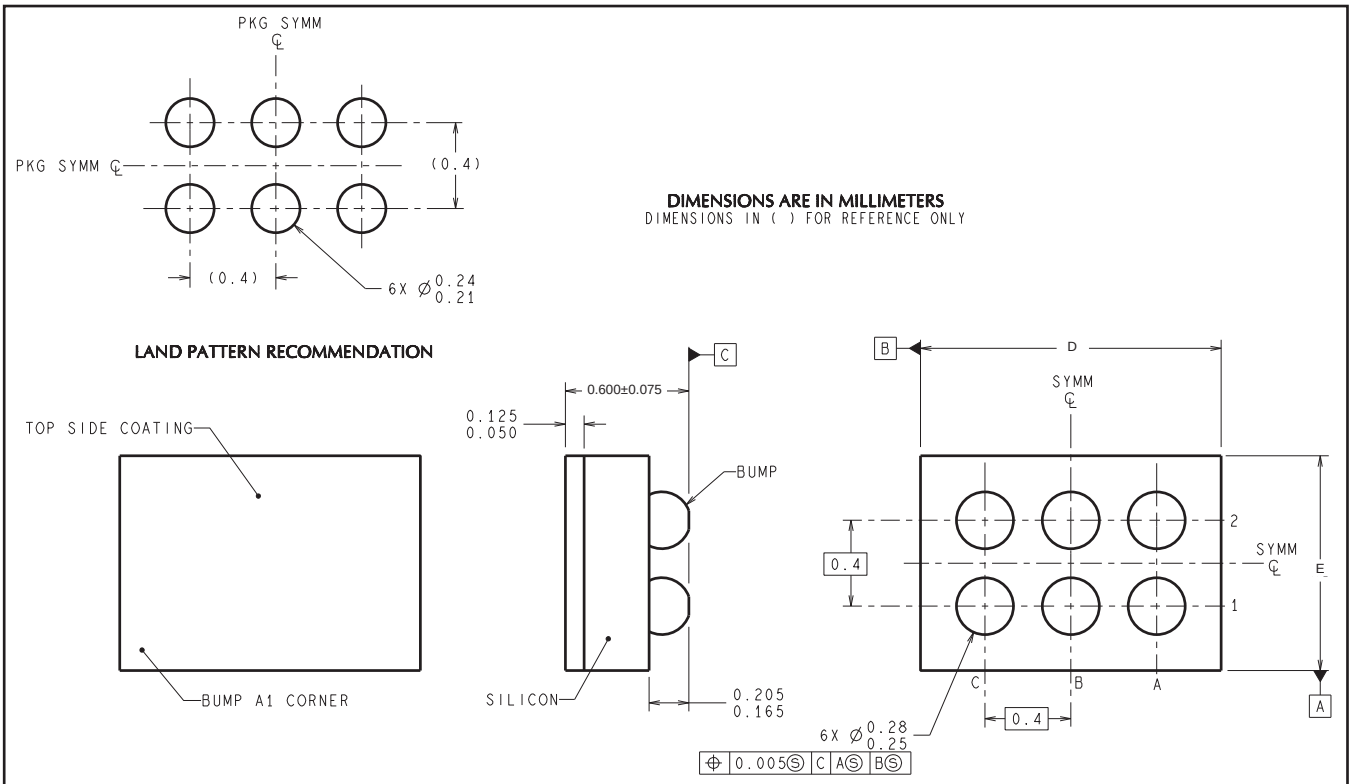
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3281YFQR	DSBGA	YFQ	6	3000	208.0	191.0	35.0

YFQ0006



D: Max = 1.465 mm, Min =1.405 mm

E: Max = 1.19 mm, Min = 1.13 mm

4215075/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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