TEXAS INSTRUMENTS

Linear Regulator Design Guide For LDOs

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ABSTRACT

This application report evaluates the thermal considerations for linear regulator design. The thermal equations governing a linear regulator and the evaluation and selection of a linear regulator for a particular design are presented.

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1   Purpose

The purpose of this application report is to explore the thermal considerations in using linear regulators. When finished, the reader will understand the following:

•   Why thermal considerations are important for every linear regulator design

•   The thermal equations governing a linear regulator

•   How to evaluate/choose linear regulators for a design

In addition, this document provides a *summary of approach and equations* in Chapter 6. This chapter is designed as a one page reference for the reader.

2   The Basics

The first considerations for choosing a linear regulator are input voltage (V_I), output voltage (V_O), and output current (I_O). These are necessary for selecting the appropriate linear regulator for an application. Other very necessary, although often over looked, considerations in linear regulator selection are the application specific thermal considerations. These thermal considerations are the topic of this application report.

For a short review on the theory of operation, a linear regulator has a pass element that is managed by the controller portion of the IC. The controller monitors the feedback and either opens or restricts the pass element to maintain a constant output voltage over variation in the input voltage and the output current required by the load. A helpful analogy is to think of the control portion of the regulator as a lamp dimmer switch or potentiometer.

Where altering a dimmer switch varies the amount of light, a linear regulator alters the pass element to maintain a constant output voltage. We know that Ohm's law states $V = I \times R$. If a linear regulator maintains a constant output voltage (V) over varying input voltage and output current into the load, it follows that R is what is being controlled by the regulator. So that is how we maintain the output voltage, but where does the heat come from?

The difference between the input voltage and output voltage with a fixed load current is energy that is dissipated by the linear regulator. Nearly all of this energy is converted to heat. How to calculate and manage this heat is the topic of this application report.

3 Power Dissipation in the Linear Regulator

To help us understand the power dissipation requirements at a high level, we use the potentiometer model shown in Figure 1.
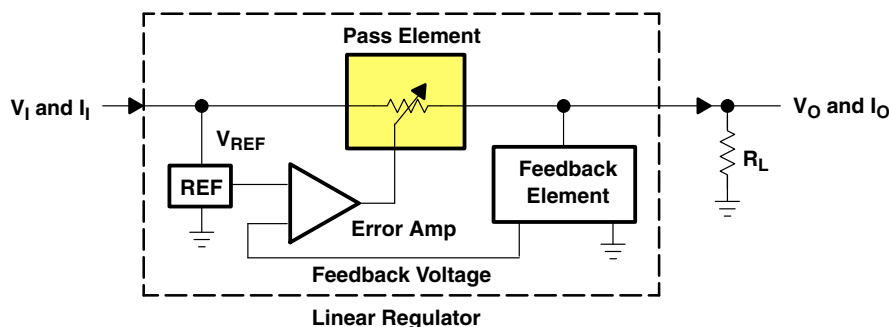

Figure 1. Potentiometer Model of a Linear Regulator

While regulating, the pass element is always on in a linear regulator. Using the potentiometer model as a guide and remembering Kirchoff's current law, we can see how the input current must be equal to the output current. Armed with that knowledge, we can look at power and power dissipation in our system.

Since our system must observe physics and the conservation of energy, we can use our knowledge of V_I, V_O, and current to identify how power is distributed in our model. We start with the power placed into our system:

$$P_I = I_I \times V_I \tag{1}$$

Following the same thought process, the power delivered to the load is:

$$P_O = I_O \times V_O \tag{2}$$

Now, looking back at Figure 1 we remember that I_I roughly equals I_O. The difference between P_I and P_O is the power that is burned or dissipated by the regulator. The quantity of dissipated power (P_D) can be extracted by the following equation:

$$P_D = P_I - P_O \tag{3}$$

P_D is almost entirely heat dissipated by the linear regulator thus P_D is precisely what we are concerned with thermally when selecting a package. If we use equation 3 to arrive at a maximum P_D for an application, we refer to that variable as $P_{D(max)}$. Making this distinction becomes useful in later equations.

Before moving on, we should take a moment to look at equation 3 in slightly more detail. Equation 3 can be rewritten from before as:

$$P_I = P_O + P_D \tag{4}$$

In most applications, the approximation of assuming $I_I = I_O$ is sufficient for thermal calculations. The model we have used up to now has ignored the quiescent current of the linear regulator. If we add the quiescent power (P_Q) required by the linear regulator, equation 4 changes to:

$$P_I = P_O + P_D + P_Q \tag{5}$$

P_Q is derived by multiplying the input voltage by the quiescent current of the regulator. Thermally, P_Q is usually insignificant, as it is orders of magnitude smaller than the output current. For example, the TPS789xx series of 100 mA (or 0.1 A) low dropout regulators (LDO) has a typical I_Q of 17 μA (or 0.000017 A). In an example where the TPS78925 is used with V_I = 3.3 V, V_O = 2.5 V, and I_O = 100 mA we can see how P_Q (56 μW) is substantially smaller than P_D (80 mW). Thus, out of practicality and for simplicity we examine the thermal considerations for linear regulators based on equation 4 ignoring quiescent current.

Quiescent current can have a significant impact on efficiency in power sensitive applications. This is covered briefly in *Other Useful Items* (Chapter 8) and in more detail in the *Efficiency* portion of TI application reports SLVA079 – *Understanding the Terms and Definitions of Low-Dropout Voltage Regulators* and SLVA072 – *Technical Review of Low Dropout Voltage Regulator Operation and Performance,* as listed in Appendix B.

Another topic that warrants a brief commentary is steady state verses transient or pulsed current demand of a load from its power supply. In many applications, an LDO supplies both steady-state and pulsed load current. A given design may have low duty cycle load transient currents in addition to the steady-state load. The current transients can approach the internal fixed current limit of the LDO, which is normally between 2 and 4 times the continuous current rating of the device. However, if we have an excessive junction temperature rise, thermal shutdown is activated. The thermal shutdown junction temperature typically occurs at 150°C. Whether the thermal design is based upon the average load current or designed to handle the maximum peak current depends upon the duration and frequency of occurrence of the load transient. In either case we are safe if we do not exceed the absolute maximum junction temperature rating of the device.

Returning to P_D, the power ratings of LDOs are normally based upon steady state operating conditions. Steady-state conditions between junction and case are typically achieved in less than 10 seconds where several minutes may be required to achieve steady-state junction to ambient. Transient thermal impedance illustrates the thermal response to a step change in power. This information is provided for discrete power devices and normally not for integrated circuits. The transient thermal response is a function of die size, die attach, and package. We limit the scope of our discussion to steady-state thermal resistance.

By utilizing the thermal equations that follow in Chapter 4, we ensure that the junction temperature of our linear regulator remains within acceptable limits. A semiconductor's long term reliability is affected by its operating junction temperature; therefore, it is important to maintain a junction temperature that falls below the manufacturers absolute maximum operating junction temperature. This restriction limits the device's power dissipation capability. To do this, we need to calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$. How to make these calculations is what we explore next.

Factors which influence thermal performance include PCB design, component placement, interaction with other components on the board, airflow, and altitude. There is no substitute for a system level thermal analysis to ensure a successful design.

4   Thermal Equations—Will My Part Work?

With an understanding of P_D, now we can examine the thermal considerations P_D generates. The following equation links P_D to the thermal specifications for a linear regulator:

$$P_D = (T_J - T_A)/\theta_{JA} \tag{6}$$

Where

θ_{JA} = theta ja (junction to ambient) – °C/W

T_J = junction temperature rating – °C

T_A = ambient temperature – °C

P_D = power dissipated in watts – W

Equation 6 enables us to relate power dissipation with the thermal characteristics of the die/package combination and ambient temperature. It is useful to manipulate equation 6 to:

$$\theta_{JA} = (T_J - T_A)/P_D \tag{7}$$

Equation 7 is useful as T_J, T_A, and $P_{D(max)}$ (see equation 3) are often known quantities in an application. By using these three known values, equation 7 will tell us what value of θ_{JA} is necessary in order to have enough thermal conductance or thermal dissipation capability for our linear regulator in a particular application. Having the appropriate thermal conductance ensures that the $P_{D(max)}$ does not exceed the P_D that the linear regulator is capable of supporting. Exceeding the P_D that the regulator can support creates extreme junction temperatures which in turn impact the reliability of the design. For the remainder of this application note, if we use $P_{D(max)}$ in equation 7 to determine a maximum θ_{JA} for an application, we are referring to it as $\theta_{JA(max)}$.

In looking at equation 7, θ_{JA} decreases with an increase in T_A or P_D. It follows that the lower θ_{JA} is from equation 7, the more challenging the thermal requirements. Additionally, the lower a θ_{JA} is specified in a data sheet, the better thermal conductance a device exhibits.

Most vendors specify θ_{JA} in a linear regulator data sheet as the thermal specification. At TI, this was the case until recently and is still the case for higher power, higher output current linear regulators. To make regulator selection easier, TI has moved to a different way of representing the same information. As an example, data sheet examples have been provided below. (NOTE: xx is the voltage option. For example: TPS77618 is the 1.8 V option in the family). Figure 2 and Figure 3 show power dissipation ratings based on package, airflow, ambient temperature, and in the case of the PowerPAD™ package, copper area underneath the device. In this case, instead of looking for a θ_{JA}, we can simply compare $P_{D(max)}$ from equation 3 to these tables so long as we cross-reference the appropriate package, ambient temperature, copper area, and airflow. Figure 4 is from page 13, of the REG103 data sheet. It demonstrates how drastically factors such as airflow or copper area, as in this case, can alter the thermal properties of a linear regulator.

PowerPAD is a trademark of Texas Instruments.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range (see Note 1) .... −0.3 V to 10 V
Voltage range at EN .... −0.3 V to V$_I$ + 0.3 V
Voltage on OUT, FB .... 7 V
Peak output current .... Internally limited
ESD rating, HBM .... 2 kV
Continuous total power dissipation .... See Dissipation Rating Tables
Operating virtual junction temperature range, T$_J$ .... −40°C to 150°C
Storage temperature range, T$_{stg}$ .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1:   All voltage values are with respect to network ground terminal.

Pdmax table

DISSIPATION RATING TABLE

	PACKAGE	T$_A$ ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T$_A$ = 25°C	T$_A$ = 70°C POWER RATING	T$_A$ = 85°C POWER RATING
Recommended	DBV	350 mW	3.5 mW/°C	192 mW	140 mW
Maximum	DBV	437 mW	3.5 mW/°C	280 mW	227 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Input voltage, V$_I$†	2.7		10	V
Continuous output current, I$_O$	0		150	mA
Operating junction temperature, T$_J$	−40		125	°C

† To calculate the minimum input voltage for your maximum output current, use the following equation:

$$V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$$

Tj specification

Figure 2. Power Dissipation Table From the TPS763xx Data Sheet (April 00)

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	$T_A < 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	0	568.18 mW	5.6818 mW/°C	312.5 mW	227.27 mW
	250	904.15 mW	9.0415 mW/°C	497.28 mW	361.66 mW

DISSIPATION RATING TABLE 2 – FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	$T_A < 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
PWP#	0	2.9 W	23.5 mW/°C	1.9 W	1.5 W
	300	4.3 W	34.6 mW/°C	2.8 W	2.2 W
PWP‖	0	3 W	23.8 mW/°C	1.9 W	1.5 W
	300	7.2 W	57.9 mW/°C	4.6 W	3.8 W

\# This parameter is measured with the recommended copper heat sink pattern on a 1-layer PCB, 5-in × 5-in PCB, 1 oz. copper, 2-in × 2-in coverage (4 in^2).

‖ This parameter is measured with the recommended copper heat sink pattern on a 8-layer PCB, 1.5-in × 2-in PCB, 1 oz. copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in^2) and layers 3 and 6 at 100% coverage (6 in^2). For more information, refer to TI technical brief SLMA002.

Note: different Pdmax with different copper & airflow!

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I ★	2.7	10	V
Output voltage range, V_O	1.2	5.5	V
Output current, I_O (Note 1)	0	1.0	A
Operating virtual junction temperature, T_J (Note 1)	−40	125	°C

★ To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(min)} = V_{O(max)} + V_{DO(max load)}$.
NOTE 1: Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

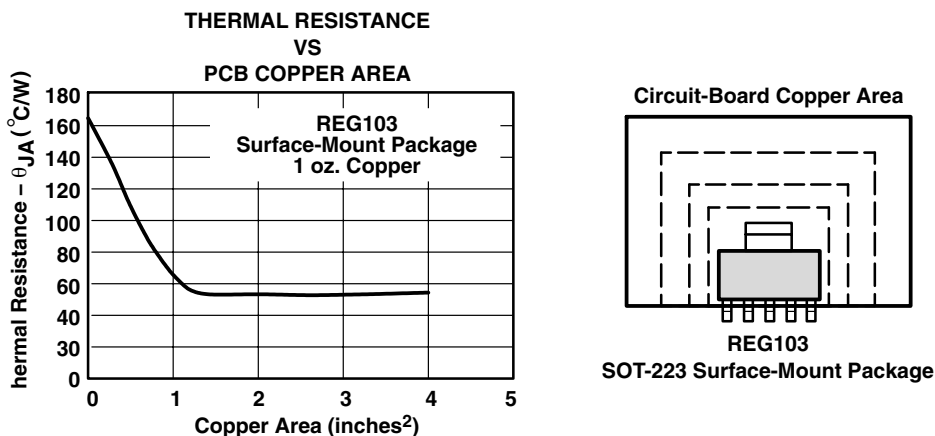**Figure 3. Power Dissipation Table From the TPS768xx Data Sheet (July 99)**

Figure 4. Thermal Resistance vs PCB Area for 5 Leaded SOT223

Depending on the data sheet, either $\theta_{JA(max)}$ or $P_{D(max)}$ can be used as a reference to determine which package meets the thermal requirements in an application. If the θ_{JA} on the data sheet is lower than the calculated $\theta_{JA(max)}$ from equation 7 or $P_{D(max)}$ from equation 3 is lower than the power dissipation tables provided, then our linear regulator is appropriate for the thermal requirements of an application. If we do not meet these criterions we must take additional steps to accommodate the thermal dissipation required by the application. Failure to do so potentially impacts the reliability of the design.

5 Thermal Equations—What to Do if My Part Does not Work?

In situations where a device or package is thermally insufficient, the first step is to look at other package options. This is one significant reason why vendors often offer linear regulators in multiple package options and why the smallest package is not always the appropriate choice. It is also possible that, if the original device does not have an appropriate package option, an engineer needs to look at a linear regulator with higher output current than is required by the application to obtain the necessary θ_{JA} to ensure reliable operation. Linear regulators with higher output current generally have a larger die and come in larger, more thermally efficient, packages. Both of these items lead to better, lower θ_{JA} or higher $P_{D(max)}$, ratings. The following figure shows a list of packages relative to thermal efficiency.

Package - # Pins	SC70 (SOT323)	SOT23-5	Chipscale 4-1 bump	MSOP-8	TSSOP 14-20	SOIC-8	PowerPad MSOP-8	PowerPad SOIC-8	SOT223	U*BGA-24	PowerPad TSSOP-24	DDPAK	TO263	TO220
Suffix	DCK	DBV	YEA/YZA	DGK	PW	D	DGK	D	DCQ	GQE	PW	KTP	KTE/KTG	KC
θ_{JA} (°C/W)	314-478	9.00	154-330	160-235	148-172	97-178	58-83	55	53-175	48	42-48	28-65	23-38	22-58
Area (mmsq)	4.94	9.00	0.81-3.20	15.18	33.96-43.95	31.00	15.18	31.00	47.55	10.24	52.14	59.72	101.58	196.54
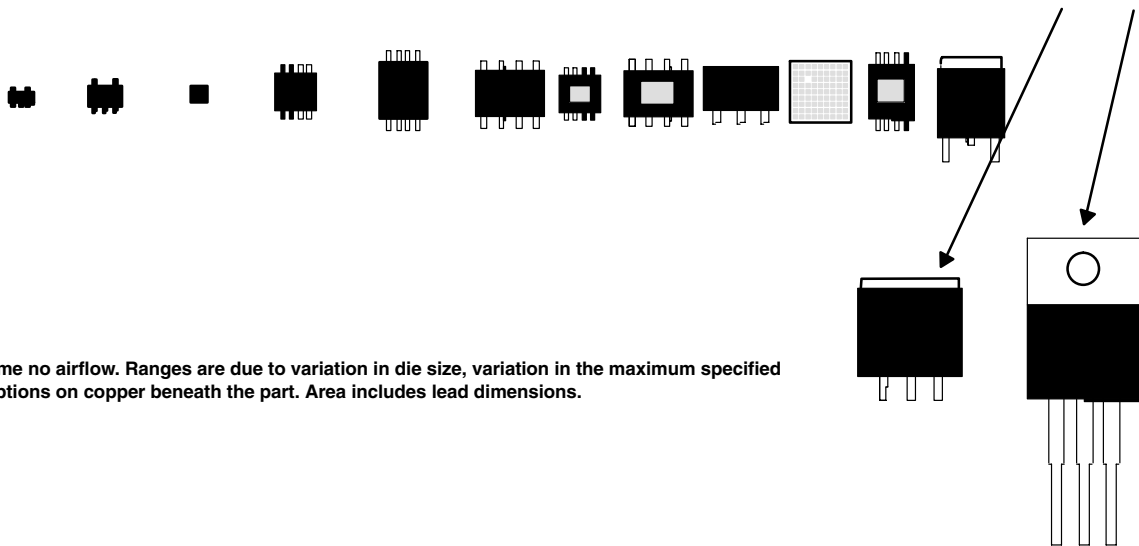
Numbers assume no airflow. Ranges are due to variation in die size, variation in the maximum specified T_J, and assumptions on copper beneath the part. Area includes lead dimensions.

Figure 5. Thermal and Area Comparison of Packages

θ_{JA} for a package varies between different parts and different vendors. Variables that affect θ_{JA} include the copper properties of a board, the number of layers of a board, the airflow over a board, and whether a high K or low K model was used (see TI application note SCAA022A – *K–Factor Test Board Design Impact on Thermal Impedance Measurements*), etc. Figure 5 is an estimate for comparison purposes only. Always consult the data sheet to obtain θ_{JA} or $P_{D(max)}$ for a given device and package option.

There is some overlap and minor variation in packages depending on pin count and die size, but Figure 5 is a starting point for comparison of common packages. Also included in the list is TI's patented PowerPAD™ packaging technology. PowerPAD footprints and dimensions remain standard while the exposed thermal pad greatly enhances the thermal capabilities of the PowerPAD MSOP, TSSOP, and SOIC packages. For more information about PowerPAD, see TI application brief (http://www−s.ti/com/sc/techlit/slma004), *PowerPAD Made Easy*, and/or application note, (http://www−s.ti/com/sc/techlit/slma002), *PowerPAD Thermally Enhanced Package*. Both of these documents are listed in Appendix B.

Where thermal considerations are challenging, another approach is to look at a switching regulator. Often, the additional efficiency that can be possible with a switching design can alleviate thermal issues faced when using a linear regulator approach. There are many considerations in migrating from a linear to a switching design that are beyond the scope of this application report.

Continuing with linear regulators, if by using equation 7 we arrive at a θ_{JA} that indicates that we have no package options to meet the thermal dissipation, the addition of a heatsink is an alternative. While often a last resort, a heatsink adds thermal mass that improves the thermal conductivity of a regulator. This effectively lowers θ_{JA} of the system and enables the linear regulator to dissipate a higher $P_{D(max)}$. A helpful analogy is to think of our thermal system in terms of resistance as shown in Figure 6.
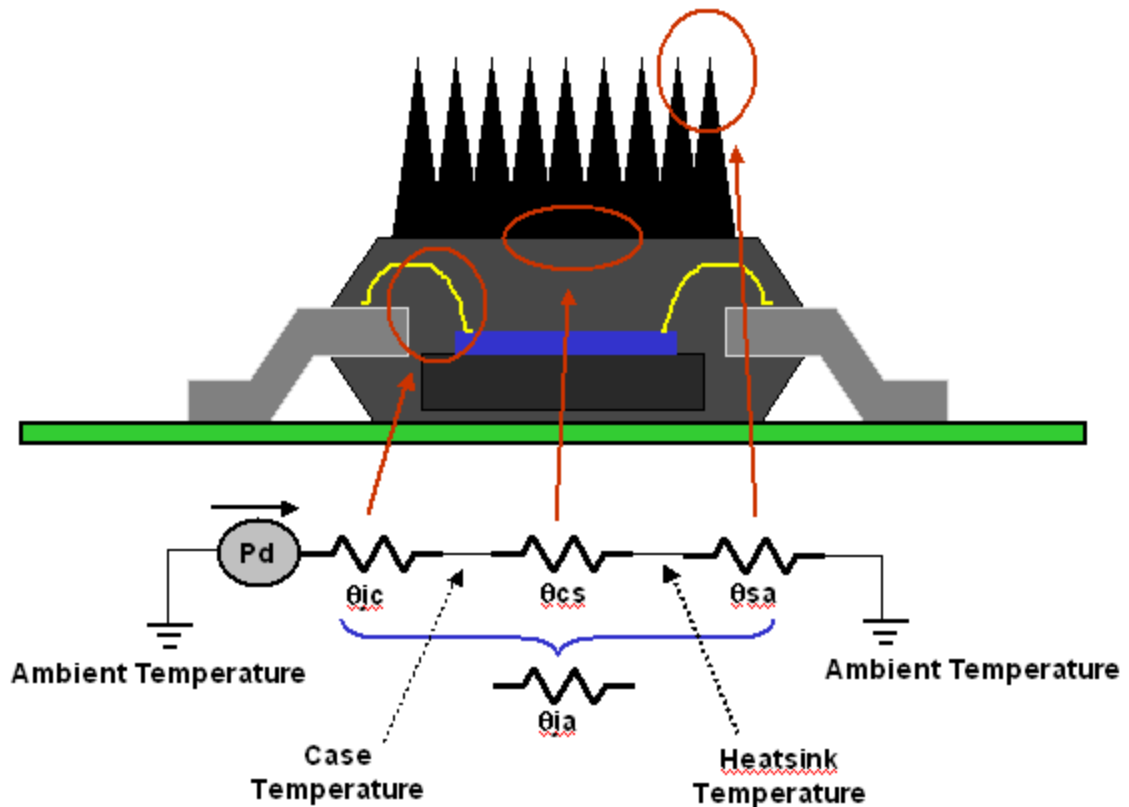

Figure 6. Steady State Thermal Equivalent Model

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In this example, we are referring to:

θ_{JA} = theta JA (junction to ambient) – °C/W
θ_{JC} = theta JC (junction to case) – °C/W
θ_{CS} = theta CS (case to heatsink) – °C/W
θ_{SA} = theta SA (heatsink to ambient) – °C/W

NOTE: θ_{CS} is the thermal interface between the device case and the sink whether it is air, PCB/solder, or any other kind of heatsink.

Our simplified steady state heat transfer model is analogous to Ohm's law. Power dissipation is analogous to current, θ is analogous to electrical resistance, and ambient temperature is analogous to ground potential or our reference point. We have used θ_{JA} up to now as we were depending on the package for a complete thermal system from junction to ambient. Since a heatsink has been added, it is necessary to break the system down into more granular components.

Adding a heatsink achieves a system θ junction to ambient low enough to meet the system thermal requirements. A heatsink accomplishes this by offering a better thermal interface to air versus the package alone. Thus, we require the following to be met:

$$\theta_{JA(max)} \geq \theta_{JC} + \theta_{CS} + \theta_{SA} \tag{8}$$

Where $\theta_{JA(max)}$ is the max acceptable thermal rating that meets the system requirements. This equation can be manipulated to:

$$\theta_{SA} \leq \theta_{JA(max)} - \theta_{JC} - \theta_{CS} \tag{9}$$

If we refer back to equation 7, we can substitute $(T_J - T_A)/P_D$ for θ_{JA} to obtain a $\theta_{JA(max)}$ and arrive at:

$$\theta_{SA} \leq [(T_J - T_A)/P_{D(max)}] - \theta_{JC} - \theta_{CS} \tag{10}$$

Equation 10 gives the designer one equation of what are normally known variables and yields the maximum allowable value for a heatsink in an application.

The value of θ_{CS} depends upon the interface material and device mounting. In the case of a PowerPAD or a TO-263 package where the exposed pad is soldered directly to the bare printed-circuit board copper, θ_{CS} is essentially 0°C/W. For a TO-220 package, which is mounted to a heatsink with a bolt or clip, a thermal interface material is used to fill voids between the tab and heat sink. The interface thermal resistance depends upon the material used and is effected by the mounting pressure, material thickness, and flatness of each surface. Typical values of common interface material range between 0.1°C/W and 1°C/W and if no interface material is used could be as high as 5°C/W.

The user should consult the interface or heat sink vender to determine a suitable material to meet the desired design goals.

By solving equation 10, we arrive at the required thermal impedance of the heatsink. Some packages, such as the TO-220, TO-263, or DDPAK better lend themselves to using heatsinks. Packages such as the SC70 and SOT23 due to their physical size, are not generally considered for use with heatsinks. Appendix A has a short list of some thermal management vendors. The vendors listed do offer various solutions for different package types. TI does not endorse one vendor over another and there are many other thermal management vendors not listed.

Having read this far, the reader should have a basic understanding of the following:

• Why thermal considerations are important in linear regulator design
• Thermal equations for a linear regulator
• How to thermally evaluate different regulators for a design

The subsequent chapters of this applications report include a summary, real world examples, items to look out for, and appendixes including reference material, and additional useful information on linear regulators and TI PowerPAD packaging technology.

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6 Summary of Approach and Equations

This chapter is a one page summary engineers can use to quickly evaluate a linear regulator.

With V_I, V_O, and $I_{O\,(max)}$ in hand, calculate $P_{D(max)}$ with:

$$P_{D(max)} = P_I - P_O \tag{3}$$
$$= (V_I - V_O) \times I_O \tag{11}$$

NOTE: The I_Q of the linear regulator is ignored due to its relative small size to I_O. Thus, we assume $I_I = I_O$.

Then, take $P_{D(max)}$ and consult the data sheets of all perspective linear regulators. If the data sheet has power dissipation tables in watts, use $P_{D(max)}$ and compare the package with the rating associated with the appropriate ambient temperature, copper area, and airflow. If the data sheet only offers a θ_{JA} for the package, calculate $\theta_{JA(max)}$ using:

$$\theta_{JA(max)} = (T_J - T_A)/P_{D(max)} \tag{7}$$

If $P_{D(max)}$ is less than the power noted in the power dissipation table or θ_{JA} in the data sheet is less than the $\theta_{JA(max)}$ calculated in equation 7, the package is thermally acceptable. Otherwise, the package is not acceptable and an alternative should be found. Also, always be sure to reference θ_{JA} or $P_{D(max)}$ with the appropriate copper area and airflow for the application when reading a data sheet.

In the case where the initial linear regulator is thermally insufficient, the easiest alternative is to look for a different package. Figure 5 is a reasonable reference to help start such a search. It is possible a linear regulator with more output current capability than required by the application may be necessary to obtain the appropriate thermal properties.

If no package can be found to meet the thermal needs for the application, the next step is to consider the addition of a heatsink or move to a switching power solution. When looking for a heatsink, use θ_{JA} calculated in equation 7 and substitute it into equation 9:

$$\theta_{SA} \le \theta_{JA(max)} - \theta_{JC} - \theta_{CS} \tag{9}$$

This yields the θ_{SA} required for the heatsink. The other major considerations in choosing a heatsink are form factor and mounting options for the linear regulator package.

7   Things Often Overlooked

Included in this chapter are answers to common questions and items that are often overlooked.

7.1   Differences Between Vendors

In making a thermal comparison between linear regulator vendors, always check the data sheet. Different manufacturers are more or less aggressive in specifying θ_{JA} and the maximum recommended junction temperature for a given package type. In addition, different vendors make different assumptions on things such as airflow or copper area under a device. Lead frame options such as TI's PowerPAD can also drastically alter the thermal capabilities of a package.

Never assume similar parts have similar thermal capabilities, particularly when they come from different vendors, and always be aware of what assumptions or conditions the specifications assume.

7.2   The Math Does Not Work... But the Part Does

It is not uncommon to find situations where the thermal equations indicate a potential problem but a part seems to work. Recall equation 7:

$$\theta_{JA} = (T_J - T_A)/P_D \tag{7}$$

does not take into account airflow or the potential benefits of heatsinking into the PCB copper. In addition, manufacturers build headroom into their specifications. The cumulative headroom this provides could allow a part to work outside what is covered in the data sheet and this document.

If additional factors such as heatsinking into the PCB copper cannot account for why a part works, it is not advised to continue to use it in a design. Violating the thermal ratings on a device can reduce the long-term reliability of the design.

The flip side to this is the situation where the original circuit was over-engineered for prototyping and exceeds what current the application requires. While the temptation is to leave the circuit as is, technically and financially it is often worth re-examining an over-engineered LDO. It can be possible to obtain advantages in both cost and space with a minimal amount of work to populate the function with a properly sized LDO.

7.3   Derating

Often, in demanding applications, companies have a policy of derating the integrated circuits they use. Depending on the project or end equipment this can be done in a variety of ways. From a thermal perspective, one often derates the absolute maximum junction temperature (T_J) for specific system reliability considerations when derating is necessary. This, in turn, decreases $\theta_{JA(max)}$ in equation 6, which causes the application's thermal design to be more demanding and operation more robust.

It is up to the user to determine device suitability for a given application. It is important that the device operate within the manufacturers operating conditions stated in the data sheet. Device operation at or above the absolute maximum ratings, which includes temperature, voltage, and current causes premature device failure.

Several reliability prediction standards are used to assess product life such as MIL-HDBK-217F and Bellcore TR-NWT-000332. Mil-HDBK-217F defines two prediction methods; a part stress analysis and parts count reliability prediction.

Common stresses that are known to accelerate device failure mechanisms include temperature, voltage, current, humidity, and temperature cycling. Temperature accelerates many chemical or physical processes that may shorten the usable life of a semiconductor device.

The Arrhenius model is commonly used for semiconductor reliability prediction. The model assumes that device failure rate is linear with time and that the acceleration factor is a function of device junction temperature. The mean time between failure (MTBF) is defined as the inverse of the acceleration factor (f). Equation 12 shows the acceleration factor expressed as the ratio of a time to fail at one temperature to a time to fail at a different temperature.

$$\text{Acceleration factor } f \; = \; \frac{t1}{t2} \; = \; \exp\left[\frac{Ea}{K}\left(\frac{1}{T1} - \frac{1}{T2}\right)\right] \tag{12}$$

Where:

Ea = Activation energy (ev)
K = Boltzmans constant 8.6 x 10E−5 ev/°K
t1 = Time between failure at temperature T1
t2 = Time between failure at temperature T2
T1 = Junction temperature (°K) at time t1
T2 = Junction temperature (°K) at time t2 where T2 >T1

We can use this equation to illustrate the effect on the MTBF by derating the maximum allowable junction temperature of the device. For this exercise we assume an activation energy of 0.9 ev. The manufacturers maximum operating junction temperature is found in the absolute maximum ratings table in the data sheet. Many low dropout regulators are specified with an absolute maximum rating of 125°C. If we reduce the maximum allowable junction temperature by 10°C for a given design we see that the MTBF approximately doubles.

In many applications it is unnecessary to derate components. This discussion was provided as an example of one common way to derate components when necessary.

8   Other Useful Items

Included in this chapter are quick references to a few useful items regarding linear regulators.

8.1   Linear Regulator Efficiency

Efficiency of any power regulator is:

$$\text{Eff} = P_O/P_I \times 100\% = (V_O \times I_O)/(V_I \times I_I) \times 100\% \tag{13}$$

If we make the assumption as we did before that $I_I = I_O$ for a linear regulator discounting I_Q due to its relative size compared with I_O, this can be simplified to:

$$\text{Eff} = V_O/V_I \times 100\% \tag{14}$$

This is a good rule of thumb, but remember, this only holds for a linear regulator design. Switching power supplies cannot be analyzed in this way.

There are applications that need to take into account the I_Q of the linear regulator. To consider I_Q, I_O no longer equals I_I and thus equation 14 is invalid. To consider I_Q, we examine equation 5:

$$P_I = P_O + P_D + P_Q \qquad (5)$$

Since quiescent power dissipation, P_Q, is also derived from the input voltage, equation 13 can be manipulated to:

$$Eff = (V_O \times I_O)/[(V_I \times I_I) + (V_I \times I_Q)] \times 100\% \qquad (15)$$

Assuming I_Q comes from the same source, V_I, as does I_I. An example where this is not the case is the UC382 as it has a bias supply input, V_B, which draws I_Q. The UC382 aside and assuming both I_I and I_Q come from the same source, we return to our potentiometer module from Chapter 3, and we conclude that:

$$Eff = (V_O \times I_O)/[V_I \times (I_O + I_Q)] \times 100\% \qquad (16)$$

Again, remember these equations only apply to a linear regulator design. One example of an application where this granularity could be important is in portable end equipments where the load is *asleep* for the majority of the time. With a very small load current for a significant amount of time, I_Q can become a significant factor in efficiency and product run time. This is why companies such as TI have low I_Q families of linear regulators. For comparison, the TPS761xx family of LDO's has a typical quiescent current of 2.6 mA where the TPS769xx family has a typical quiescent current of 0.017 mA. Both are 100-mA LDOs, but the TPS769xx was designed for power sensitive applications as are other TI LDOs which offer even lower I_Q than the TPS769xx.

With regard to I_Q, we must also keep in mind what the relationship is between I_Q and output current. PMOS linear regulators are generally load independent.
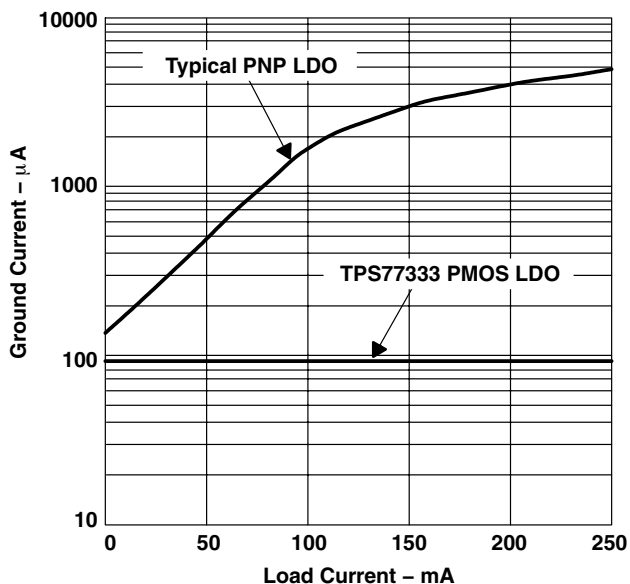

Figure 7. Comparison of 100-μA I_Q PMOS and PNP LDOs

As illustrated in Figure 7, the PMOS linear regulators I_Q is essentially constant as a function of load current. In contrast, bipolar linear regulators have I_Q characteristics that are load dependent. This can be important to take into account before deciding that I_Q is negligible. Particularly for bipolar linear regulators, it is good practice to consult the graphs in the data sheet if they are provided.

TEXAS
INSTRUMENTS

8.2   Input Voltage, Dropout Voltage (V_{DO}), and Low Dropout Regulators (LDO's)

Dropout voltage for linear regulators is often misunderstood. As discussed previously, the difference between V_I and V_O is the voltage drop across the linear regulator. The lower the difference between the input and output voltage, the lower the power dissipation for a given load current. The dropout voltage is defined as the minimum difference required between V_I and V_O for the regulator to operate within specification. A subset of linear regulators called *low dropout regulators* (or *LDO*) exhibits small dropout specifications. This can be an advantage when:

* V_I and V_O are close in value

* V_I can be manipulated to be close to V_O thus reducing P_D and increasing efficiency

*   A battery is the V_I source, thus allowing the regulator to draw voltage from the battery and regulate over a wider range

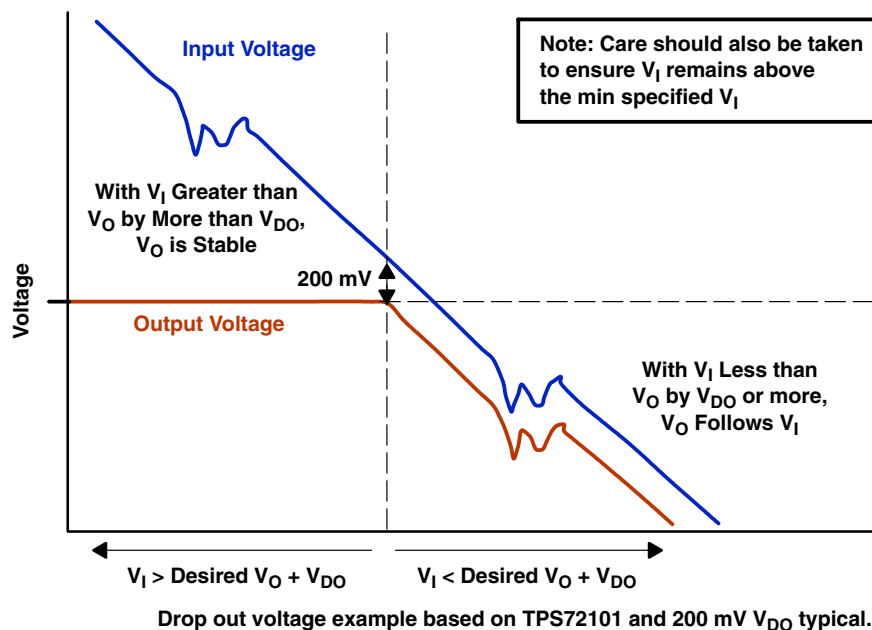Figure 8 demonstrates what a dropout voltage specification means visually.

Drop out voltage example based on TPS72101 and 200 mV V_{DO} typical.

Figure 8. Dropout Voltage Example

To highlight the difference between a standard linear regulator and what is considered an LDO, look at the V_{DO} specification on both the TPS77601 and the LM317M. TI considers anything with a $V_{DO} < 1$ V to be an LDO and anything with $V_{DO} > 1$ V to be a *standard* linear regulator. In summary, the minimum input voltage as shown in Figure 8 is the greater value of either V_O + V_{DO} or the minimum specified input voltage.

The ultimate combination is an LDO that has both a low dropout and an input voltage range that extends to relatively low voltages. An example of this is the TPS721xx (150 mA), TPS722xx (50 mA), and TPS725xx (1 A) series. This series is the first LDO in the industry to allow V_I down to 1.8 V and a very small V_{DO} which allows these parts to run directly off batteries in portable applications or off other core voltages for point-of-use needs. As a side note, this family of LDOs also features stability with any output capacitor providing even more flexibility in designs.

9 Real World Examples

Included in this chapter are four real world examples to further illustrate the thermal concepts presented in this application report.

Example 1:

We need to power a C5409 DSP core with a small amount of additional logic at 1.8 V. The application calls for a 100 mA solution at 1.8 V and this rail needs to be created from 5 V. The maximum ambient temperature is 70°C, and we assume zero airflow. The TPS76318 and REG101-A linear regulators are under consideration. Which device(s) and package options are acceptable?

Answer:

As a side note, if we take a quick look at efficiency with equation 14:

$$Eff = V_O/V_I \times 100\%$$
$$Eff = 1.8 \text{ V}/5 \text{ V} \times 100\% = \sim36\%$$

Obviously, a linear regulator is not the optimal solution for efficiency in this case but we assume efficiency is not a primary design goal in this application.

Both the TPS76318 and REG101-A have an acceptable input voltage range, output voltage range, and output current capability. The potential pitfall in this application are the thermal considerations.

Ignoring the I_Q of the linear regulator, at 100 mA output current we calculate the input and output power:

Output Power: $P = I \times V = 100 \text{ mA} \times 1.8 \text{ V} = 180 \text{ mW}$
Input Power: $P = I \times V = 100 \text{ mA} \times 5 \text{ V} = 500 \text{ mW}$

$$P_D = P_I - P_O$$
$$P_{D(max)} = 500 \text{ mW} - 180 \text{ mW} = 320 \text{ mW}$$

With the TPS76318 data sheet, we cross reference $P_{D(max)}$ with our ambient temperature in the thermal tables.

DISSIPATION RATING TABLE

BOARD	PACKAGE	R$_{\theta JC}$	R$_{\theta JA}$	DERATING FACTOR ABOVE T$_A$ = 25°C	T$_A \leq 25$°C POWER RATING	T$_A$ = 70°C POWER RATING	T$_A$ = 85°C POWER RATING
Low K‡	DBV	65.8 °C/W	259 °C/W	3.9 mW/°C	386 mW	212 mW	154 mW
High K§	DBV	65.8 °C/W	180 °C/W	5.6 mW/°C	555 mW	305 mW	222 mW

‡ The JEDEC Low K (1s) board design used to derive this data was a 3 inch x 3 inch, two layer board with 2 ounce copper traces on top of the board.
§ The JEDEC High K (2s2p) board design used to derive this data was a 3 inch x 3 inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Input voltage, V$_I$¶	2.7		10	V
Continuous output current, I$_O$	0		150	mA
Operating junction temperature, T$_J$	−40		125	°C

Figure 9. Power Dissipation Table From the TPS76318 Data Sheet (May 01)

We see that 320 mW at 70°C is a problem and that the SOT23 package is not suitable for this application. The REG101-A data sheet addresses thermal considerations in terms of θ_{JA}. Using equation 7, T_A, and $P_{D(max)}$ we can evaluate the REG101-A:

$\theta_{JA} = (T_J - T_A)/P_D$
$\theta_{JA} = (125°C - 70°C)/0.320 \text{ W} = \sim 171°C/W$

In looking at the θ_{JA} ratings shown in Figure 10 for the REG101–A we see that the SOT23 package option is still unacceptable. However the SO-8 package option is suitable having a θ_{JA} less than 171°C/W.

TEMPERATURE RANGE								
Specified Range	T_J			−40		+85		°C
Operating Range	T_J			−55		+125		°C
Storage Range	T_A			−65		+150		°C
Thermal Resistance								
SOT23-5 Surface Mount	θ_{JA}	Junction-to-Ambient			200			°C/W
SO-8 Surface Mount	θ_{JA}	Junction-to-Ambient			150			°C/W

Figure 10. From the REG101 Data Sheet (July 01)

In this example, we see quickly how thermal considerations can impact component selection with linear regulators.

To take this example a step further:

• *What would happen if the output current increased to 150 mA?*
    – $P_{D(max)}$ increases to 580 mW, θ_{JA} decreases to 95°C/W, and Eff is the same. Neither part is an option as neither has an acceptable package. 150 mA is beyond the REG101-A specification for output current also. A more appropriate part may be the 250 mA REG102-A in a SOT223 package with a θ_{JA} close to 60°C/W among other choices from TI.

• *What would happen if V_I were lowered to 3.3 V with 100-mA output current?*
    – $P_{D(max)}$ becomes 190 mW, θ_{JA} becomes to 289°C/W, and Eff is ~54%. Now, both of our original parts would work in the smaller SOT23 package option.

These basic changes produce drastic differences to our thermal considerations.

Example 2:

The TPS76833 linear regulator is available in an 8-pin SO and a 20-pin TSSOP package. Determine which package option will meet the following criteria:

$V_I = 5.0 \text{ V} + 5\%$
$V_O = 3.3 \text{ V} \pm 2\%$
I_O: 0.95 A
$T_A = 50°C$, natural convection air flow

Answer:

First, determine the required worst case power dissipation.

$P_{D(max)} = (V_I - V_O) \times I_O$
$\qquad\quad = [(V_I \times 1.05) - (V_O \times 0.98)] \times I_O$
$\qquad\quad = (5.25 - 3.234) \times 0.95$
$\qquad\quad = 1.915 \text{ W}$

Now determine the maximum package thermal impedance requirement given the above criteria.

$P_{D(max)} = (T_{J(max)} - T_A)/\theta_{JA}$ Rearranging and solving for θ_{JA}

$\theta_{JA} \leq (T_{J(max)} - T_A)/P_{D(max)}$

From the TPS76815 data sheet we see that the absolute maximum junction temperature is 125°C. In this application, your company mandates that all components have derated $T_{J(max)}$. For this example we derate by 10°C.

Let $T_{J(max)}$ = 115°C

Therefore the required $\theta_{JA} \leq (115 - 50)°C/1.915$ W = 33.9°C/W

From the data sheet we see that the 8-pin SOIC package (D) does not meet the requirement since it has a θ_{JA} of 172°C/W. The 20-pin TSSOP PowerPAD package (PWP) meets the requirement having a θ_{JA} of 32.6°C/W if it is mounted on a board having a copper heat sink area of at least four square inches (1 oz. copper).

Example 3:

The REG104 linear regulator is available in a SOT223 and TO-263 surface mount packaging. Determine which package option meets the following criteria:

V_I = 5.0 V + 5%

V_O = 2.5 V ±2%

I_O: 1.0 A

T_A = 50°C, natural convection air flow

Answer:

First, determine the required worst case power dissipation:

$P_{D(max)} = (V_I - V_O) \times I_O$

$= [(V_I \times 1.05) - (V_O \times 0.98)] \times I_O$

$= (5.25 - 2.45) \times 1 = 2.8$ W

Now determine the maximum package thermal impedance requirement given the above criteria.

$P_{D(max)} = (T_{J(max)} - T_A)/\theta_{JA}$ Rearrange and solving for θ_{JA}

$\theta_{JA} \leq (T_{J(max)} - T_A)/P_{D(max)}$

From the REG104 data sheet we see that the absolute maximum junction temperature is 150°C. Thus,

Let $T_{J(max)}$ = 150°C

Therefore the required $\theta_{JA} \leq (150 - 50)°C/2.8$ W = 35.7°C/W

From Figure 10 of the REG104 data sheet we see that a TO-263 mounted on 1.5 square inches of 1 oz. copper has a θ_{JA} of 32°C/W. Since the mounting tab is at ground potential, the entire ground plane can be used to further reduce the thermal impedance.

Example 4:

Given that a TMS320C6201 DSP has the following system requirements:

Core: 1.8 V ±3% at 1.0 W

I/O: 3.3 V ±5% at 0.2 W

V_I = 5.0 V ±5%

T_A = 50°C

Find a suitable power solution using a dual LDO regulator to power the DSP system.

We must first determine the total power dissipation required for the dual regulator.

$$P_{D(core)} = (V_I - V_{core})) \times I_{(core)}$$
$$= (V_I(1.05) - V_{core}(0.97)) P_{core}/V_{core}(0.97)$$
$$= (5.25 - 1.75) (1.0)/1.75 = 2.0 \text{ W}$$

$$P_{D(I/O)} = (V_I - V_{O(I/O)}) \times I_{(I/O)}$$
$$= (V_I(1.05) - V_{I/O}(0.95)) P_{I/O}/V_{I/O}(0.95)$$
$$= (5.25 - 3.14) (0.2)/3.14 = 0.134 \text{ W}$$

Total regulator dissipation = $P_{D(core)}$ + $P_{D(I/O)}$ = 2.0 W + 0.124 W = 2.124 W

Next, determine the required maximum package thermal impedance.

Maximum allowable dissipation:

$$P_{D(max)} = (T_{J(max)} - T_A)/\theta_{JA}$$
$$\theta_{JA} \leq (T_{J(max)} - T_A)/P_{D(max)}$$

Most of the TI LDO data sheets list an absolute maximum junction temperature rating of 125°C. Thus,

Let $T_{J(max)}$ = 125°C

Therefore $\theta_{JA} \leq (125 - 50)/2.124 = 35.3$°C

The DSP power selection matrix table (page 35) of the *Power Management Selection Guide*, literature number SLVT145 recommends the TPS767D318 as a possible product to meet the system requirements. From the TPS767D318 data sheet we find that it meets the voltage and tolerance requirements as well as thermal. It features a θ_{JA} of 32.6°C/W if at least four square inches of 1 oz. copper heat sink area is used. Since the thermal pad is at ground potential, the entire ground plane could be used to further reduce the thermal impedance.

Appendix A   Thermal Managment Vendors

- Aavid Thermal Technologies   http://www.aavidthermalloy.com/
- Bergquest Company   http://www.bergquistcompany.com/
- IERC   http://www.ctscorp.com/ierc/
- Wakefield Engineering   http://www.wakefield.com/

Appendix B Additional TI Documentation on Thermal Topics, Packaging, and Linerar Regulators

1. Fundamental Theory of PMOS Low-Dropout Voltage Regulators

    http://www−s.ti.com/sc/psheets/slva068/slva068.pdf

    Covers the basics of how a linear regulator, specifically a PMOS Low-Dropout regulator, functions.

2. Understanding the Terms and Definitions of Low-Dropout Voltage Regulators

    http://www−s.ti.com/sc/psheets/slva079/slva079.pdf

    Briefly defines common terms associated with Low-Dropout regulators including Quiescent Current, Efficiency, Dropout Voltage, Line and Load Regulation, and more.

3. Technical Review of Low Dropout Voltage Regulator Operation and Performance

    http://www−s.ti.com/sc/psheets/slva072/slva072.pdf

    A more in depth discussion of common Low-Dropout regulator specifications including Quiescent Current, Efficiency, Dropout Voltage, Line and Load Regulation, Stability, and more.

4. PowerFLEX™ Surface Mount Power Packaging

    http://www−s.ti.com/sc/psheets/slit115a/slit115a.pdf

    This document could be particularly helpful with TI's surface mount alternatives to TO-220 packages.

5. Thermal Characteristics of SLL (Standard Linear Logic) Package and Devices

    http://www−s.ti.com/sc/psheets/scza005b/scza005b.pdf

    This document has an exhaustive list of packages covered and runs though some of the same calculations covered in this paper.

6. K-Factor Test-Board Design Impact on Thermal Impedance Measurements

    http://www−s.ti.com/sc/psheets/scaa022a/scaa022a.pdf

7. PowerPAD Made Easy

    http://www−s.ti.com/sc/psheets/slma004/slma004.pdf

    This application note is a quick reference explaining what is TI's PowerPAD thermal enhancement and how does one use a part in this package.

8. PowerPAD Thermally Enhanced Package

    http://www−s.ti.com/sc/techlit//slma002

    This application note is a more extensive review of the PowerPAD technology and equations behind and implementation of products using this package.

9. MicroStar BGA Packaging Reference Guide

    http://www−s.ti.com/sc/psheets/ssyz015b/ssyz015b.pdf

    This contains 6x6 – 16x16 BGA thermal information.

10. Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs

    http://www−s.ti.com/sc/psheets/szza017a/szza017a.pdf

11. Thermal Derating Curves for Logic-Products Packages

http://www−s.ti.com/sc/psheets/szza013a/szza013a.pdf

12. PT3100/4100 Series Application note revised 5/15/98.

13. TI external website for packaging information

http://www.ti.com/sc/docs/package/pkg_thermal_db.htm

As an example, if looking for TSSOP information: *Enter packaging group = all, package type TSSOP,   JEDEC design guidelines = all,   Then SEARCH.*

NOTE: *urls are provided for quick reference, but as the web is always changing please be aware that these links may change as well! If you have trouble finding one of these documents, please contact your local TI representative or your regional TI Product Information Center.*

Appendix C   Other References

1. S. M. Sze, VLSI Technology, McGraw-Hill, New York, 1988.

2. AN1029 Fairchild, April, 1996
   Maximum Power Enhancement Techniques for SO-8 Power MOSFETs
   Alan Li, Brij Mohan, Steve Sapp, Izak Bencuya, Linh Hong
   Note: Related documents include AN1028, AN1025, AN1026 for other packages.

3. AN–569, Motorola, 1973
   Transient Thermal Resistance—General Data and Its Use
   Bill Roehr and Bryce Shiner

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DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
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