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## Power Supply Design Considerations for Modern FPGAs

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### Introduction

Today's FPGAs tend to operate at lower voltages and higher currents than their predecessors. Consequently, power supply requirements may be more demanding, requiring special attention to features deemed less important in past generations. Failure to consider the output voltage, sequencing, power-on, and soft-start requirements can result in unreliable power-up or potential damage to FPGAs.

### Output Voltage Requirements

The first criteria to consider when designing power supplies for FPGAs are the voltage requirements for the different supply rails. Most FPGAs have specifications for the CORE and IO voltage rails and many require additional auxiliary rails that may power internal clocks, phase-lock loops or transceivers. *Table 1* provides the voltage levels and tolerances for some of the newest FPGAs.

**Table 1. Voltage Requirements for Common Modern FPGAs**

FPGA	Core	Core Tolerance	Auxiliary Power	Auxiliary Tolerance	IO Voltage*	IO Tolerance*
Spartan-6	1.2	5%	2.5 or 3.3	5%	1.2 to 3.3	1.1 to 3.45
Spartan-6 (-1L)	1.0	5%	2.5 or 3.3	5%	1.2 to 3.3	1.1 to 3.45
Virtex-6	1.0	5%	2.5	5%	1.2 to 2.5	1.14 to 2.625
Virtex-6 (-1L)	0.9	30 mV	2.5	5%	1.2 to 2.5	1.14 to 2.625
Stratix-IV (GX and E)	0.9	30 mV	2.5 (VCCA_PLL)	5%	1.2 to 3.0	5%
			0.90 (VCCD_PLL)	30 mV		
Stratix-IV (GT)	0.95	30 mV	2.5 (VCCA_PLL)	5%	1.2 to 3.0	5%
			0.95 (VCCD_PLL)	30 mV		
Cyclone-IV (GX)	1.2	40 mV	2.5	5%	1.2 to 3.3	5%
Cyclone-IV (E)	1.0	*	2.5	5%	1.2 to 3.3	5%
Arria-II	0.9	30 mV	2.5 (VCCA_PLL)	5%	1.2 to 3.3	5%
			0.90 (VCCD_PLL)	30 mV		

\* Some values may differ slightly from those listed. Please consult your FPGA's associated documentation for details.

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Since FPGAs generally specify several permissible voltage levels for the IO, the voltage selected is dictated by the external digital circuitry. To provide flexibility, FPGAs will generally provide multiple IO banks that can be powered separately, allowing FPGAs to interface with various logic families. For simplicity, the solutions illustrated in this article will assume all IO banks are powered off of a single power supply rail. The core voltage supplies the internal logic configuration blocks of FPGAs and is where many of the internal digital path processes occur. As such, the current demanded by the core will vary greatly depending on the percent utilization of FPGAs. Vendors of the FPGAs described herein provide design tools that estimate core current requirements based on the internal blocks utilized.

Over time, the voltages used to power the core have steadily dropped. Modern cores utilize 65 nm, 45 nm or even 40 nm geometry silicon processes and may operate from voltages as low as 0.9V. These lower voltages are valuable to reduce power dissipation in FPGAs. The trade off, however, is that keeping within the voltage tolerance requirements becomes more challenging for the power supply designer.

### Output Capacitance and Transient Considerations

A good power supply design will keep the core voltage within tolerance at all times. Most of the power supply transient concerns can be managed by properly selecting the bypass and bulk capacitances for the power supply. In general, every core ball or pin connection should be bypassed directly under FPGAs with high-quality X5R or X7R ceramic capacitors. The values recommended for each of these capacitors range from 1  $\mu\text{F}$  to 10  $\mu\text{F}$  and will generally be specified by FPGA manufacturers. These capacitors provide a charge when FPGAs need to rapidly draw large spikes of current during high speed operations. Likewise, the bulk capacitance should be selected to provide charge during large steps of current, which tend to occur during power-on, application-start, or a change in application state. Before increasing the amount of output capacitance to solve transient droop issues, changes to the power supply should be made that do not involve an increase in PCB area or component count.

The response to a load transient is dictated by the large signal response time that consists of ramping the inductor current to the correct operating level and the small signal response of the control loop.

### Transient Response Optimizations

To optimize the transient response, ensure the supply is switching at the highest possible frequency. This will allow use of a small inductor and reduce the large signal response time. Typical high performance power supply solutions can be designed to have crossover frequencies as high as one-tenth to one-fifth the switching frequency. Pushing the crossover frequency too high may result in ringing at the output during a load transient indicating poor phase margin. Any ringing in the output should be avoided as this may result in instability with external component variation or when operating at temperature extremes.

### AUX Voltage Considerations

Many FPGAs require a third power supply commonly referred to as the auxiliary rail or AUX. Since the AUX rail may power internal clocks, phase-lock loops, or transceivers, the amount of output voltage ripple on this rail should be minimized. In some cases, additional ferrite beads and capacitors filtering may be needed to meet the application or FPGA noise requirements. In applications where noise is extremely important, a low noise, high PSRR LDO, like the LP3878, should be considered instead of a switching converter.

### Sequencing Requirements

The sequencing requirements vary depending on the particular FPGA being used and many newer FPGAs specify that no sequencing is required. While this is technically true for the FPGA, it is not the optimal way to design a power solution. National Semiconductor offers several devices to address sequencing requirements. The LM3880 is designed to address sequential sequencing of multiple supply rails. This device is available in a small SOT-23 package and can sequence up to three supply rails. Many options are available to control the up and down, three-flag outputs sequencing timing. National also provides devices to support customized flag order and timing.

Figure 1 illustrates a typical application circuit for the LM3880.

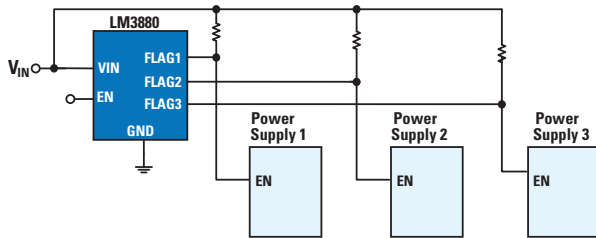


Figure 1. Simplified Buck Converter Schematic

Voltage tracking is another method of sequencing power supplies applicable to FPGAs and many processors. The most common and generally recommended method to power up FPGAs and other processors is to have the CORE voltage track the I/O voltage during startup as shown in Figure 2.

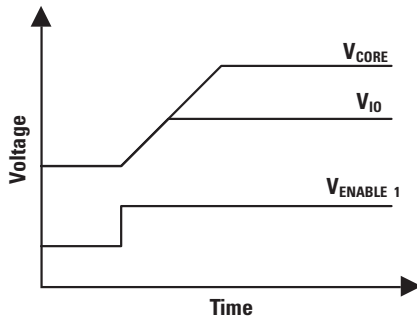


Figure 2. Startup voltage tracking

This power-up technique is known as simultaneous startup, and its primary advantage is that it avoids turning on any parasitic conduction paths that may exist between the CORE and IO supply rails. Turning on a parasitic conduction path may lead to unreliable startup or even damage to FPGAs or DSPs. Some of National's devices that feature voltage tracking include the LMZ14203 and LMZ10504 SIMPLE SWITCHER® Power Modules, the LM20k family of high performance synchronous DC/DC converters, as well as the LM3743 controller.

Figure 3 illustrates a typical voltage tracking configuration for these devices.

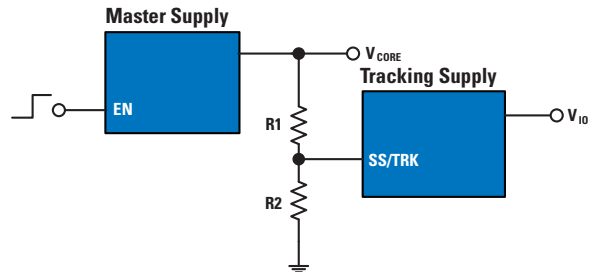


Figure 3. Typical voltage tracking configuration

## Startup / Power-on Requirements

When sequential sequencing is used in systems with multiple voltage rails, as is the case with many FPGA solutions, it is likely that an output of one of the power supplies could be pre-biased through various parasitic conduction paths. In this situation, how the power supply handles this pre-biased state can have an impact on long term system reliability, or even the ability of the power supply or FPGAs to start successfully. To avoid the pitfalls associated with a pre-biased startup, the power supply should not pull the output low if a pre-biased condition exists. Figure 4 illustrates how a pre-biased condition should be handled when the output is pre-biased to three different voltage levels. All power solutions featured in this publication are capable of properly handling a pre-biased start up. Power supplies used to power both the CORE and IO must be monotonic during power-on to avoid FPGA startup problems. A monotonic startup continuously increases until the output reaches the final value.

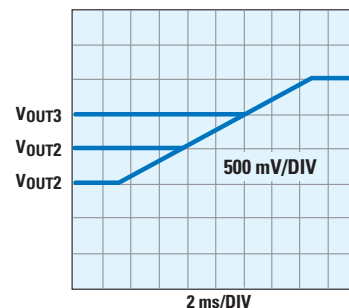


Figure 4. Pre-biased startup of the LM3743

## Power Supply Design Considerations for Modern FPGAs

The critical area for monotonicity for most modern core voltage rails occurs between 0.5V to 0.9V. This is when FPGAs initialize the internal logic blocks to valid operating states.

### Soft-start Requirements

Using soft-start is highly recommended, even if not specified by the FPGA manufacturer. Slowly ramping the input voltage reduces the inrush currents seen in some FPGAs. Using soft-start also reduces the current needed to charge the output capacitance of the power supply and will decrease the voltage droop on the input bus during startup.

The startup or soft-start requirements for several FPGAs are summarized in *Table 2*.

**Table 2. Required Startup/Soft-start Times**

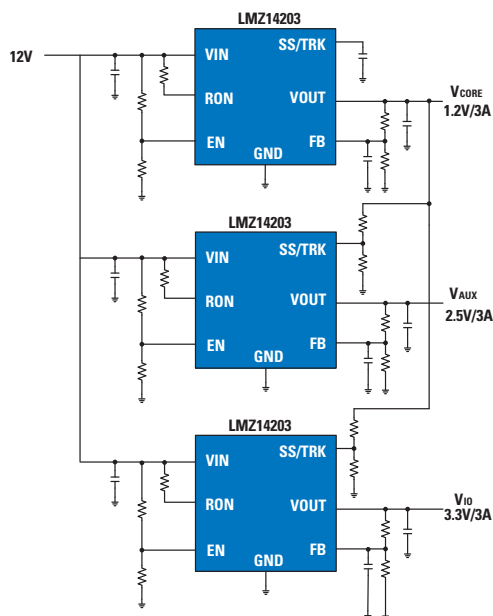
FPGA	Min	Max
Spartan-6 (-3 & -2 Speeds)	0.20 ms	50 ms
Spartan-6 (-1L speed grade)	0.20 ms	40 ms
Virtex-6	0.20 ms	50 ms
Cyclone IV (Normal POR)	0.050 ms	50 ms
Cyclone IV (Fast POR)	0.050 ms	3 ms
Stratix-IV (Normal POR)	0.050 ms	100 ms
Stratix-IV (Fast POR)	0.050 ms	4 ms
Arria-II GX (Normal POR)	0.050 ms	100 ms
Arria-II GX (Fast POR)	0.050 ms	4 ms

A startup time of 10 ms generally limits the capacitive inrush currents to an acceptable level while meeting the requirements for most FPGAs and DSPs.

### Application Examples

The application examples shown to the right implement requirements previously discussed for powering FPGAs. These solutions are meant to be guidelines for selecting the correct devices and circuit topologies to meet FPGA power requirements.

*Figure 5* uses the synchronous LMZ14203 SIMPLE SWITCHER Power Module, capable of supplying 3A of output current. This newly-released device not only includes the power switches, but also the inductor inside the package. This reduces the component design and procurement process to just a few capacitors and resistors. The inductor's inclusion in the package also simplifies layout complexities because of the reduced loop area with large di/dT transitions. This, coupled with the inductor's shielded design, reduces EMI and National Semiconductor tested its evaluation boards to comply with the EN55022 Class B specification.



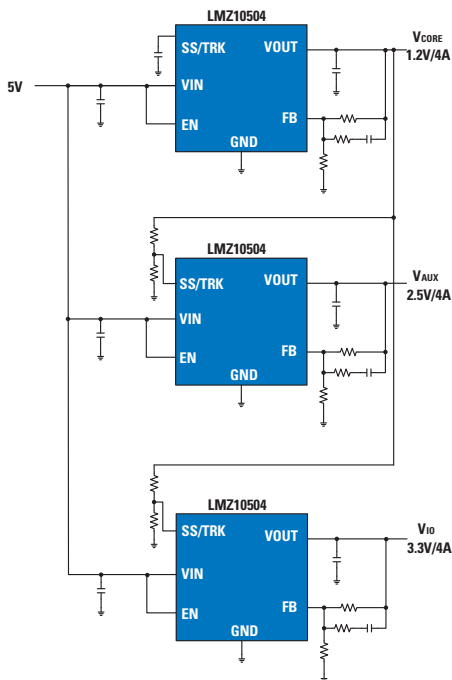
**Figure 5. 3A Core and I/O Solution from 12V Bus**

As an added benefit, the SIMPLE SWITCHER power module families use a 7 lead TO-263-like package and each family is pin-to-pin compatible, providing an easy path to support different current levels. The packaging lends itself very well to hand-soldered prototypes while the exposed pad on the bottom conducts heat out of the package and enables a very low  $\theta_{JA}$  of 20°C per watt.

This solution is ideal for lower output current FPGAs and features a monotonic startup with voltage tracking.

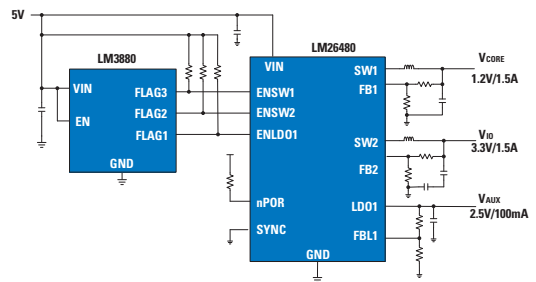
The LMZ14203 includes many fault protection features such as over-voltage protection (OVP), under-voltage protection (UVP), thermal shutdown, and an accurate current limit. The synchronous operation of the LMZ14203 offers improved efficiency over non-synchronous devices resulting in cooler operation and increased reliability.

*Figure 6* illustrates the LMZ10504 SIMPLE SWITCHER Power Module being used to power an FPGA for load currents up to 4A. Similar to the LMZ14203, this newly-released device includes the power switches and inductor inside the package, thus sharing the same easy design-in process. This full-featured device operates at a fixed 1 MHz switching frequency and offers voltage tracking, programmable soft-start, and 1.5% voltage accuracy at the feedback pin. The LMZ10504 achieves efficiencies as high as 96% and features the same protection features as the LMZ14203 while also sharing its 7 lead TO-263-like package. Both devices are fully supported by WEBENCH® Power Designer.



**Figure 6. 4A Core and I/O Solution from 5V Bus**

*Figure 7* features the LM26480 PMIC to provide the CORE, IO and AUX voltages from a single device. This device integrates dual switching regulators with a current capability of up to 1.5A each and dual LDOs with a current capability of up to 300 mA each. This high degree of integration makes the LM26480 an ideal solution for use with the Cyclone and Spartan families of FPGAs. This solution provides a monotonic startup with internal soft-start to limit inrush startup currents. Sequencing is performed with the LM3880. The startup sequence will be the CORE followed by the IO, and then by the AUX rails. The LM3880 features an integrated precision enable circuit that allows the user to set the turn on voltage with two external resistors.

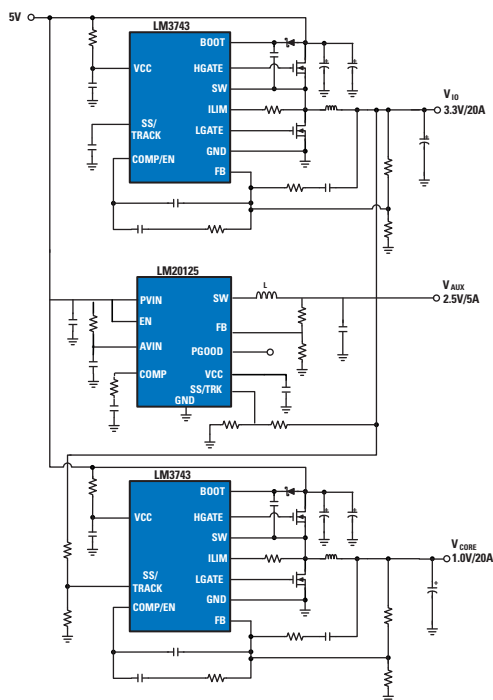


**Figure 7. Externally-Sequenced Single Chip FPGA Power Supply**

The circuit shown in *Figure 8* utilizes the LM3743 for powering both the CORE and IO. This controller is capable of supporting designs up to 20A and features a SS/TRACK pin to provide a monotonic simultaneous startup. The LM3743 provides increased system reliability by offering both high- and low-side current limit as well as output under-voltage protection. The device also features a hiccup mode protection that eliminates thermal runaway during fault conditions.

The LM20125 is used to power the auxiliary voltage rail and has a compatible SS/TRK pin. This synchronous buck regulator utilizes emulated current mode control and uses nonlinear slope compensation to ease design-in. The LM20125 is a 5A-capable device with efficiencies as high as 97% due to the 35 mΩ integrated FETs.

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**Figure 8. High current LM3743-based power supply solution.**

The LM201xx family of devices shares the same pin-out so higher or lower currents can be obtained by interchanging devices. The LM20125 is offered in a small TSSOP-16 package and is fully supported by WEBENCH Power Designer.

National offers a wide range of products that support the power requirements of the latest generation of FPGAs. These power solutions can support the sequencing, soft-start, and voltage tolerance requirements for the newest families of FPGAs, as well as handle challenges such as pre-biased outputs and demanding transient response needs. For your complete FPGA power supply needs, please visit [www.national.com](http://www.national.com). ■

### References

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