Compensation Made SIMPLE with LM4360x, LM4600x

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ABSTRACT

Compensating a DC-DC buck converter is challenging if the designer is not familiar with the loop control theory. To achieve a stable design under all corner and adverse conditions, the user must properly compensate the regulator. While DC-DC converters with external compensation provide flexibility, they increase complexity. The LM43600/1/2/3 and LM46000/1/2 are a family of Wide V_{IN}, fully-synchronous SIMPLE SWITCHER® regulators with fully-integrated compensation, making BOM selection and stabilizing a design easy. The addition of an external feed-forward capacitor further enhances the response to a sudden load transient. The value of the C_{FF} capacitor is calculated with a simple equation discussed in Section 3.

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1 Buck Converter Control Methods Overview

Two of the most commonly-used control methods in buck converters are Current Mode Control (C-M) and Voltage Mode Control (V-M).
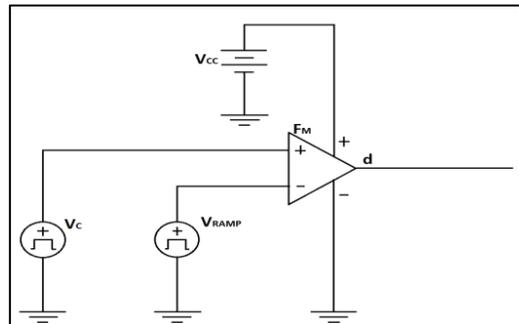
1.1 Voltage Mode Control

Figure 1. Voltage Mode Control

The voltage mode architecture is more complex due to difficulty in stabilizing the design. As shown in Figure 1, the V-M architecture relies on a fixed voltage ramp (V_{RAMP}), generated internal to the IC, presented to the comparator to generate the PWM signal. The other input of the comparator is the output of the compensated error amplifier (V_C). Longer delays to control the PWM signal result due to the fixed internal ramp. For example, if there were a sudden increase in the input voltage, the V-M control would not realize it immediately and it would maintain the same switching duty cycle for the next few cycles. With the same duty cycle and higher input voltage, the output would then increase. This would result in a feedback error. The error amplifier would react to it and adjust the V_C voltage. This will eventually lead to the reduction in duty cycle. This delay causes a large overshoot at the output voltage. If the slew rate of the rise in input voltage is higher, the overshoot is also higher. If there is no over voltage protection (OVP) designed in the system, this could result in the load being put under stress. A similar problem occurs when there is a sudden change in the load levels. For the output to maintain smaller overshoots and undershoots during a fast load transient, it is important to have the error amplifier well compensated. A poorly compensated design will result in longer delays to react to a load change and result in larger overshoots and undershoots. In V-M control, the inductor and capacitor at the output create a complex double pole in the frequency domain, causing a sharp phase loss. To nullify this, two compensating zeroes are necessary and their placement is very important to have a good phase boost and a faster reaction time. The compensation is L-C_{OUT} dependant and, almost always, a Type-III compensation method with time-consuming fine tuning is required. To integrate a Type-III compensation inside the IC is further challenging and if the compensation is left external to the IC, then the BOM count increases.
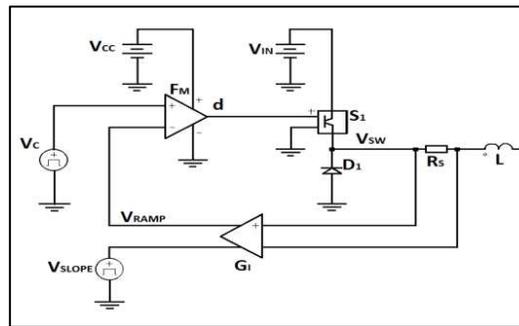
1.2   Current Mode Control

Figure 2. Current Mode Control

The C-M control, as the name implies, uses the current through the inductor to create the comparing ramp. As shown in Figure 2, the sensed inductor current is scaled and then summed with a slope compensation ramp (V_{SLOPE}) and then presented to the comparator. The V_{SLOPE} is a ramp that is a function of the frequency. Addition of V_{SLOPE} helps subdue any sub-harmonic oscillations caused in the C-M control over 50% duty cycles. The V_{SLOPE} is usually integrated and hence makes designing simpler. The other input of the comparator (V_C) is the output of the compensated error amplifier. The sensed inductor ramp replaces the fixed internal voltage ramp and therefore reaction to any sudden change in the input line voltage is immediate. As in the previous example mentioned, if the input experiences a sudden voltage surge, then the ripple current through the inductor will change too. This change in the ripple current is also realized at the comparator, and the duty cycle quickly adjust before the output overshoots considerably. This results in a considerably smaller delay to correct the behavior compared to V-M control. Because of the introduction of the internal current loop to sense the inductor current, the inductor is now de-coupled from the output capacitor. This results in the breaking up of the complex double pole of L and C_{OUT} in to two real poles, with the capacitor pole caused by the interaction of the load resistance and C_{OUT} existing at lower frequencies and the inductor pole at higher frequencies. Due to this, the compensation becomes much simpler, because only the capacitor pole is required to be compensated and at most a Type-II compensation technique is used. This typically requires only one zero. Integrating the compensation also helps reduce the BOM count. For more versatile operation over a wide operating range, a second zero is added by introducing a feed-forward capacitor (C_{FF}) in parallel with the upper feedback resistor. An additional zero can also be achieved by using aluminum electrolytic capacitors at the output. The electrolytic capacitors have higher ESR than their ceramic counterparts, and bring the zero caused by the output cap and ESR to lower frequencies. The downside is that the output has a slightly larger ripple.

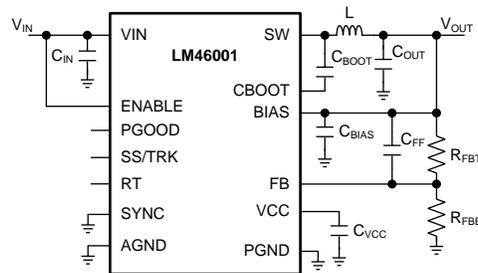## 2 Introduction to the LM4360x and LM4600x control loop

Figure 3. Typical Application Schematic using the LM46001

An internally-compensated buck converter makes designing the DC-DC power supply easy. The internal compensation components for the devices in the LM4360x and LM4600x family are Rc = 400 kΩ and Cc = 50 pF. The internal slope compensation ramp is scaled to the switching frequency and, between different devices of the family, it is scaled to the max peak current. It is designed to cover the corners and the entire range of 1 V to 28 V of output voltage is supported. The overall compensation of the LM4360x and the LM4600x is designed to allow a wide range of inductor and capacitor values. Inductor values are chosen so that the resulting ripple current through the inductor is between 20% to 50% of the load current and any chemistry of capacitors can be used. The external components contributing to the overall stability of the design include the inductor, the output capacitor and, if necessary, the feed-forward capacitor (C_{FF}). Refer to the datasheet for a detailed description and typical values table to select the L and C_{OUT} values. This leaves just the feed-forward cap to be selected.

3 Feed-forward Capacitor and Optimization

The value of the C_{FF} capacitor should be calculated so that the resulting phase margin of the overall system is improved. The addition of the C_{FF} capacitor does not change the response of the system at the DC level or at lower frequencies. At higher frequencies, the capacitor helps reduce the impedance from V_{OUT} to FB. This helps propagate any high frequency change due to a fast load transient at the output to the feedback, and allows the error amplifier to correct for this.

In the frequency domain, the addition of the C_{FF} capacitor creates an additional zero and a pole. The zero is caused by the interaction of C_{FF} with the upper feedback resistor (R_{FBT}). This helps increase the gain by 20 dB/decade, and gives the necessary phase boost. The zero frequency is as follows:

$$f_Z = \frac{1}{2 \times \pi \times R_{FBT} \times C_{FF}}$$

(1)

The pole is caused by the interaction of C_{FF} with the parallel combination of the upper feedback resistors (R_{FBT}) and the lower feedback resistor (R_{FBB}). The pole decreases the gain by 20 dB/dec, and helps to roll off the gain after the system crossover. Gain margin is also increased. The pole frequency is as follows:

$$f_p = \frac{1}{2 \times \pi \times (R_{FBT} \| R_{FBB}) \times C_{FF}}$$

(2)

From the above equations, if the C_{FF} increases, the zero moves to lower frequencies. The pole also moves to lower frequencies and if the value of C_{FF} is not optimized, the actions of the zero and the pole nearly cancel each other out. This is exacerbated at relatively lower outputs, where the pole and zero frequencies are very close. To obtain the best performance from the C_{FF} cap, its value should be optimized.

The C_{FF} cap optimization relies on the idea that if the zero and pole frequencies are aligned so that the system crossover frequency without the use of C_{FF} ($f_{X\_NO\_CFF}$) is exactly in the middle of the pole and zero frequencies caused by the C_{FF}, then the most optimum phase boost is obtained at the crossover frequency. The C_{FF} pole follows after the crossover frequency and assists the gain roll off for better gain margin. The equation is as follows:

$$f_{X\_NO\_CFF} = \sqrt{f_Z \times f_P}$$

(3)

Substituting the Equation 1 and Equation 2 in Equation 3, solve for the value of the C_{FF} capacitor. The final equation is then:

$$C_{FF} = \frac{\sqrt{R_{FBB} + R_{FBT}}}{2 \times \pi \times f_{X\_NO\_CFF} \times R_{FBT} \times \sqrt{R_{FBB}}}$$

(4)

Where,

- C_{FF} = Feed-forward capacitor
- R_{FBT} = Upper feedback resistor
- R_{FBB} = Lower feedback resistor
- $f_{X\_NO\_CFF}$ = System crossover frequency without the use of C_{FF}

The first and easiest method for C_{FF} optimization is to use the simplified linear equation that estimates the value of $f_{X\_NO\_CFF}$. The linear approximation assumes that the output capacitor is of a ceramic type with very low ESR. The effect of ESR is not taken into consideration, and does not assume any parasitic pole frequencies occurring at higher frequencies. The linear approximation is different for every part in the LM4xx family of devices. The following equation applies to every device in the family:

$$f_{X\_NO\_CFF} = \frac{K}{V_{OUT} \times C_{OUT}}$$

(5)

The corresponding values of the constant K for all the devices in the family can be obtained from the Table 1 as follows:

Table 1. Device specific constant values

DEVICE	CONSTANT VALUE (K)
LM43603	5.3
LM43602	4.35
LM43601	2.73
LM43600	1.5
LM46002	4.35
LM46001	2.73
LM46000	1.5

The result of the Equation 5 could then be used in Equation 4 to obtain the required C_{FF} value. The second method to estimate the value of the parameter $f_{X\_NO\_CFF}$ is to use the downloadable PSPICE bode plot model. The model has been previously correlated against bench data for accuracy, and can plot the loop response.

The third method of C_{FF} optimization can be used if the total output capacitance is not solely of ceramic type or if a frequency response analyzer (FRA) is available. In case where the output capacitor is not strictly ceramic the linear approximation may not generate good results. To use the FRA, the connection between V_{OUT} and R_{FBT} should be broken to allow the injection of an AC voltage signal that acts as a perturbation, as shown in Figure 4. The signal is injected across the R_{FRA} resistor, and the transfer function of CH B/CH A is measured and plotted on the bode plot.
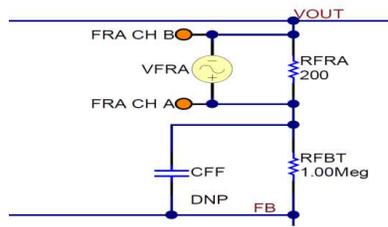
Figure 4. Frequency Response Analyzer (FRA) on the FB path of the EVM

The first step is to plot the system response without the use of C_{FF}. Then from this measurement, note the crossover frequency of the system as $f_{x\_NO\_CFF}$. This then can be used in Equation 4 to obtain the value of the C_{FF}. The following examples use the FRA approach to obtain the optimized value for C_{FF}

3.1 *Example 1*

- V_{IN} = 24 V
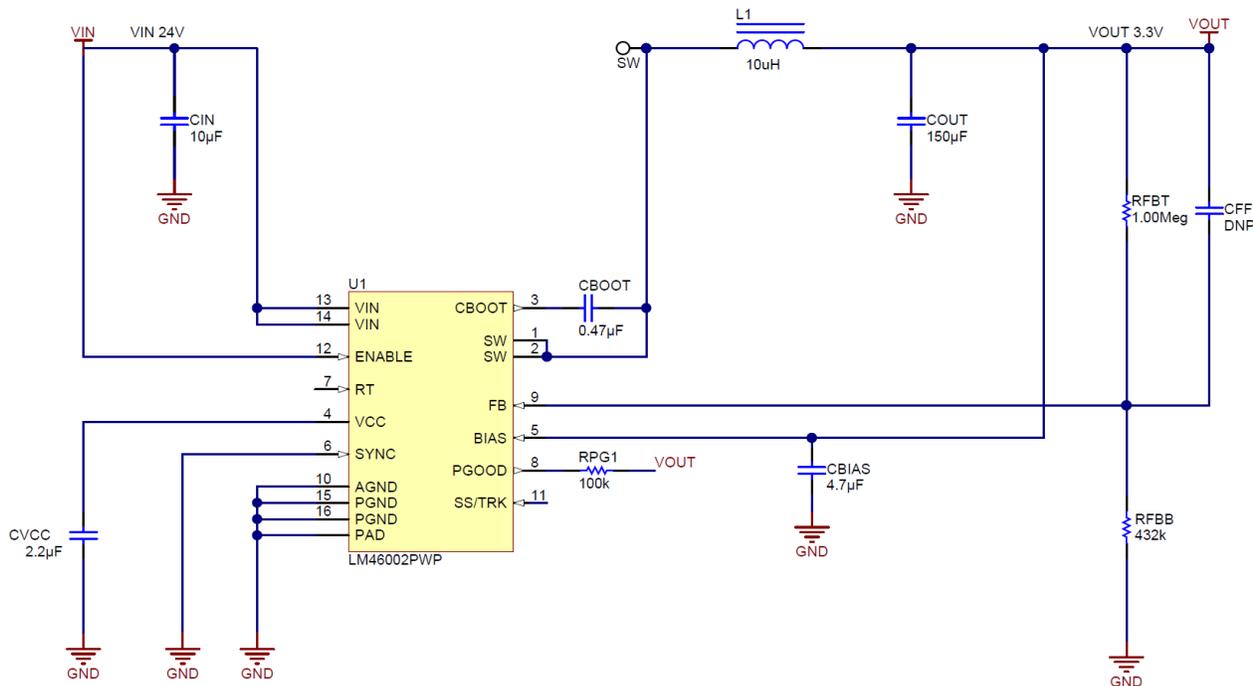- V_{OUT} = 3.3 V
- I_{OUT} = 2 A
- F_{SW} = 500 kHz
- IC = LM46002

Figure 5. Schematic for V_{OUT} = 3.3 V, F_{SW} = 500 kHz

For the above schematic, a total of about 150 µF in ceramic capacitors is used. Inductor value is selected to be 10 µH for 30% inductor ripple. The top feedback resistor is 1 MΩ and the lower is 432 kΩ. The feed-forward cap (C_{FF}) is not populated for the basic design. The load transient of 200 mA to 2 A (10% to 100% levels) and a bode plot taken at 2 A load yield the following results:
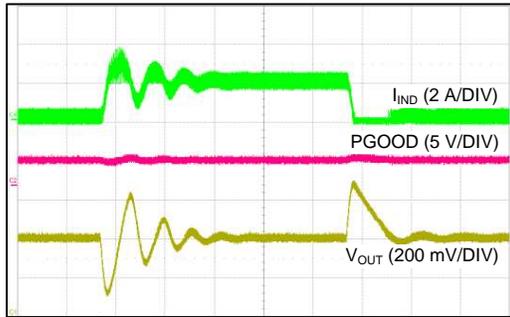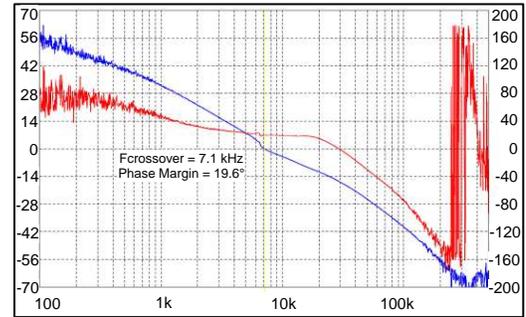
Figure 6. Load Transient between 200 mA and 2 A

Fcrossover = 7.1 kHz
Phase Margin = 19.6°

Figure 7. Bode Plot for I_OUT = 2 A

The bode plot shows a marginal phase margin of 19.6°. The load transient shows ringing with about 250 mV of undershoot on the output voltage at the transient. If the desired application experiences fast load transients, the ringing could get worse and cause instabilities. Adding the feed-forward cap to applications susceptible to fast load transients, helps improve the load transient response.

From the C_{FF} optimization equation, use the $f_{X\_NO\_CFF}$ and the values of the feedback resistors. From the bode plot $f_{X\_NO\_CFF}$ is about 7.1 kHz, and from the BOM the R_{FBT} = 1 MΩ and R_{FBB} = 432 kΩ. Using these numbers in the equation results in a value of 40 pF. Using the next standard value of 47 pF results in the following responses:
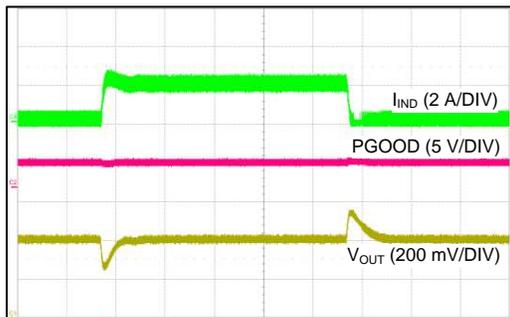

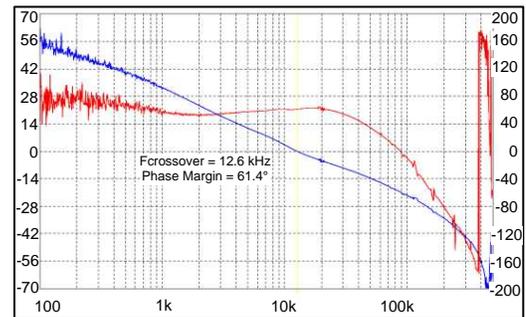**Figure 8. Load Transient between 200 mA and 2 A**

Fcrossover = 12.6 kHz
Phase Margin = 61.4°

Figure 9. Bode Plot for I_OUT = 2 A

Figure 9 shows that addition of the 47 pF C_{FF} greatly improves the response. The load transient no longer shows the ringing at the output, the undershoot is now less than 200 mV and the bode plot shows 61.4° of phase margin with a slight increase in the crossover frequency to 12.6 kHz.

3.2 *Example 2*

- V_{IN} = 24 V
- V_{OUT} = 5 V
- I_{OUT} = 2 A
- F_{SW} = 500 kHz
- IC = LM46002

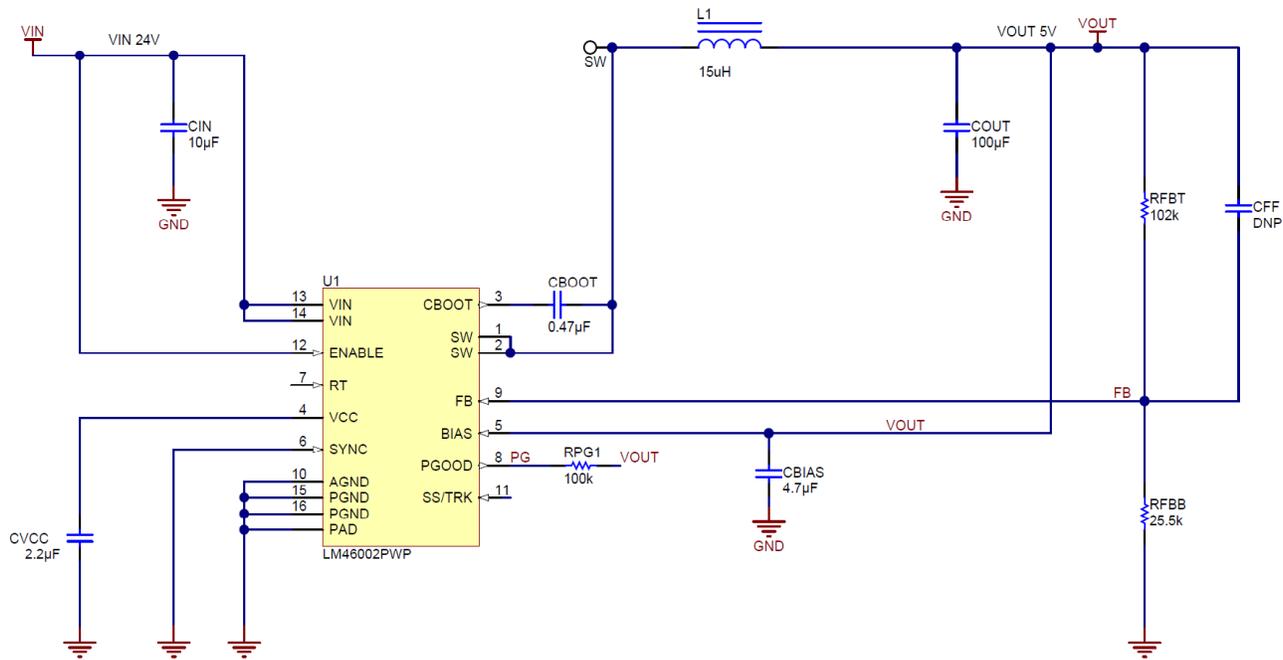**Figure 10. Schematic for V_{OUT} = 5 V, F_{SW} = 500 kHz**

For the above schematic, a total of about 100 µF ceramic capacitors are used at the output. Inductor value is selected to be 15 µH for 30% inductor ripple. The feed-forward cap (C_{FF}) is not populated for the basic design. The top feedback resistor is at 102 kΩ, and the lower is 25.5 kΩ. The load transient test of 200 mA to 2 A and a bode plot taken at 2A load yield the following results:

Time (200 µs/DIV)

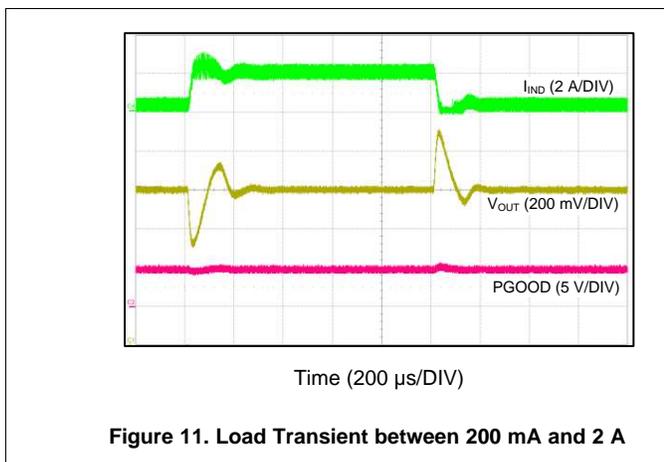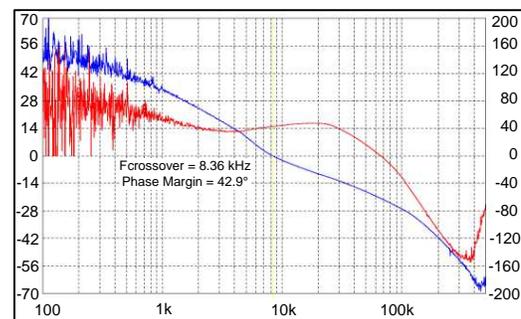**Figure 11. Load Transient between 200 mA and 2 A**

Figure 12. Bode Plot for I_{OUT} = 2 A

These results show that the basic design is stable with slightly less than 300 mV of undershoot at the output. The bode plot shows about 43° of phase margin, which is good, but the crossover frequency is low. For applications not targeted towards a faster transient response, this design is stable and works well.

If further optimization is required, adding a C_{FF} should help. From the bode plot, the $f_{X\_NO\_CFF}$ is about 8.3 kHz, R_{FBT} is 102 kΩ and R_{FBB} is 25.5 kΩ. Using the equation results in about 420 pF for C_{FF}. A standard value of 470 pF was used. The resulting responses are as follows:
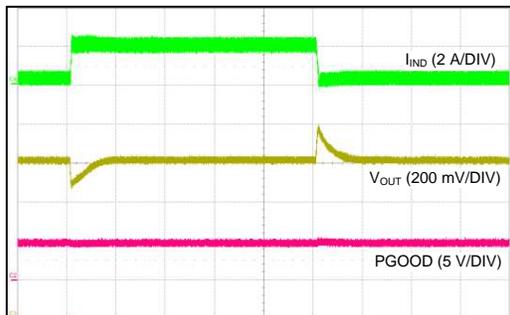

Figure 13. Load Transient between 200 mA and 2 A
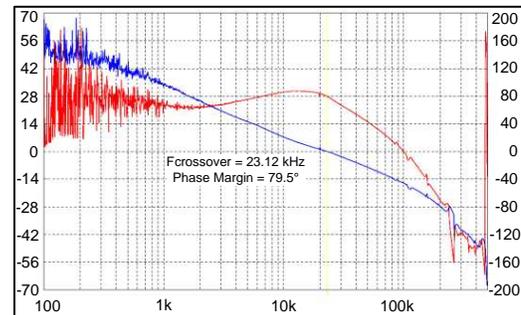
Figure 14. Bode Plot for I_{OUT} = 2 A

The crossover frequency increased to 23 kHz with about 80° of phase margin. The response to fast load transient is quick with low overshoots and undershoots.

4   Conclusion

The new family of Wide V_{IN}, fully-synchronous SIMPLE SWITCHER® regulators with internal compensation are easy to use, and result in stable designs with a minimal BOM while allowing a wide range of external filter selection. Further optimization of the design is also easily possible with the addition of just one component as discussed.

5   References

1. Understanding And Applying Current-Mode Control Theory (SNVA555)
2. Optimizing Transient Response of Internally Compensated dc-dc Converters With Feed-forward Capacitor (SLVA289)

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