Active Clamp Transformer Reset: High Side or Low Side?

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ABSTRACT

The active clamp transformer reset technique offers many well documented advantages over traditional single-ended reset techniques, including lower voltage stress on the main MOSFET, the ability to switch at zero voltage, reduced EMI and duty cycle operation above 50 percent. The single-ended forward converter is by far the most popular power topology using the active clamp, but the same advantages can be applied to flyback converters. Numerous publications have compared the performance advantages of the active clamp over the more widely used RCD clamp, third winding and resonant reset techniques. There are, however, application specific design considerations of how to best apply the active clamp for optimal circuit performance.

1   Introduction

All of the papers written on the active clamp technique show the clamp circuit applied to either the high side directly across the transformer primary, or the low side directly across the drain-to-source of the main MOSFET switch. Even more interesting is the fact that authors seem to be equally divided as to which application, high side or low side, is best while offering little or no explanation as to why.

There are subtle but noteworthy differences between applying the active clamp transformer reset technique to the high side and applying it to the low side. Each application results in a different transfer function, which in turn results in different voltages applied to the clamp circuit during reset. The value and voltage rating of the clamp capacitor is directly affected, as well as distinct considerations between gate drive circuitry for each case.

TEXAS
INSTRUMENTS

2   Low-Side Clamp

Figure 1 shows a low-side clamp applied to a basic single-ended forward converter with a standard full-wave rectified output and LC filter.
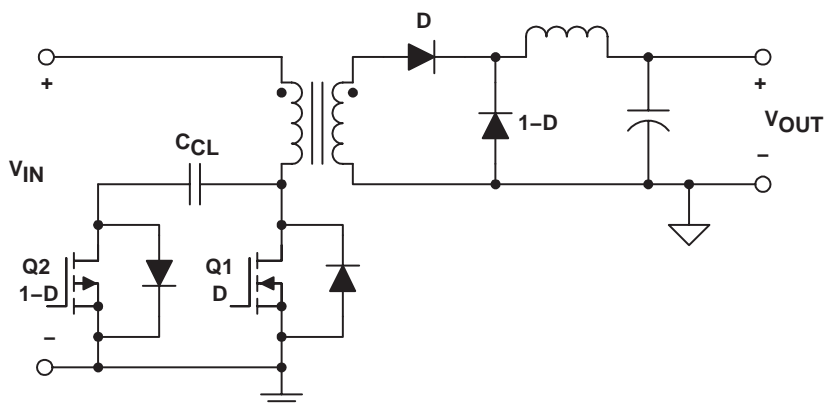
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Figure 1.   Low-Side Active Clamp Circuit

Whenever the main MOSFET, Q1, is conducting, the full input voltage is applied across the transformer magnetizing inductance, and this is referred to as the power transfer mode.

Conversely, whenever the auxiliary (AUX) MOSFET, Q2, is conducting, the difference between the clamp voltage and the input voltage is applied across the transformer magnetizing inductance, and this is referred to as the transformer reset period. Specific to the low-side clamp is the fact that the auxiliary MOSFET, Q2, must be a P-channel device only because of the direction of the body-diode. It is also worthy to note that Q2 carries only the transformer magnetizing current, which has a very small average value compared to the reflected load current. For this reason, specifying a low gate charge MOSFET should be a primary consideration with low $R_{DS(on)}$ being only a secondary concern.

There is also an additional dead-time period introduced between the time when Q1 is turning off and Q2 is turning on. During the dead-time, primary current flow remains continuous through the body-diode of either the P-channel AUX MOSFET, Q2, or the main MOSFET, Q1. This is commonly known as the resonant period in which the conditions are set for zero voltage switching (ZVS). This is an important and unique characteristic of the active clamp topology but it bears little importance for this comparison, other than to briefly mention that it always exists whether the active clamp is applied to the low side or the high side.

Neglecting the effect of leakage inductance, the transfer function for the low-side clamp can be derived by applying the principle of volt-seconds balance across the transformer magnetizing inductance.

$$D \times V_{IN} = (1 - D) \times V_{C(LS)} - (1 - D) \times V_{IN} \tag{1}$$

Simplifying equation (1) for the clamp voltage, $V_{C(LS)}$, gives:

$$V_{C(LS)} = \left[\frac{1}{1 - D}\right] \times V_{IN} \tag{2}$$

It is interesting to note that the transfer function given in (2) is also the same transfer function for a non-isolated boost converter and this is why the low-side clamp is commonly referred to as a boost type clamp.

The result of (2) gives an expression for the transfer function between the input voltage and the clamp voltage. However, notice from Figure 1 that whenever Q2 is conducting, the clamp voltage is applied directly across the drain-to-source junction of Q1, and not the transformer primary magnetizing inductance. Therefore (2) can be extended and written to include an expression for determining the drain-to-source voltage stress on the main MOSFET, Q1:

$$V_{DS(LS)} = V_{C(LS)} = \left[\frac{1}{1 - D}\right] \times V_{IN} \tag{3}$$

During the transformer reset period, the dot polarity on the transformer primary reverses, so the voltage applied to the primary is now defined as:

$$V_{RESET(LS)} = V_{C(LS)} - V_{IN} \tag{4}$$

If the expression for $V_{C(LS)}$ from (2) is substituted into (4) and simplified, a transfer function relating the input voltage to the reset voltage can be shown as:

$$V_{RESET(LS)} = \left[\frac{D}{1 - D}\right] \times V_{IN} \tag{5}$$

Furthermore, the duty cycle, D, of a single-ended forward converter is defined as the ratio of the output voltage to the input voltage multiplied by the transformer turns ratio, $N = \frac{N_p}{N_s}$.

$$D = \left[\frac{V_O}{V_{IN}}\right] \times N \tag{6}$$

Substituting (6) into (3) and (5) and simplifying gives expressions for $V_{C(LS)}$ and $V_{RESET(LS)}$ in terms of V_{IN}, V_O and N, as shown in (7) and (8).

$$V_{DS(LS)} = V_{C(LS)} = \frac{V_{IN}^2}{V_{IN} - N \times V_O} \tag{7}$$

$$V_{RESET(LS)} = \frac{V_O \times V_{IN} \times N}{V_{IN} - N \times V_O} \tag{8}$$

The results of (7) and (8) can now be used to graphically show how the clamp voltage and transformer reset voltage vary with input voltage for a fixed value of V_O and a fixed transformer turns ratio, N. Using a value of 4 V for V_O (3.3 V plus some additional voltage drop), the graphical results of (7) are first plotted in Figure 2 and shown for various transformer ratios, N.
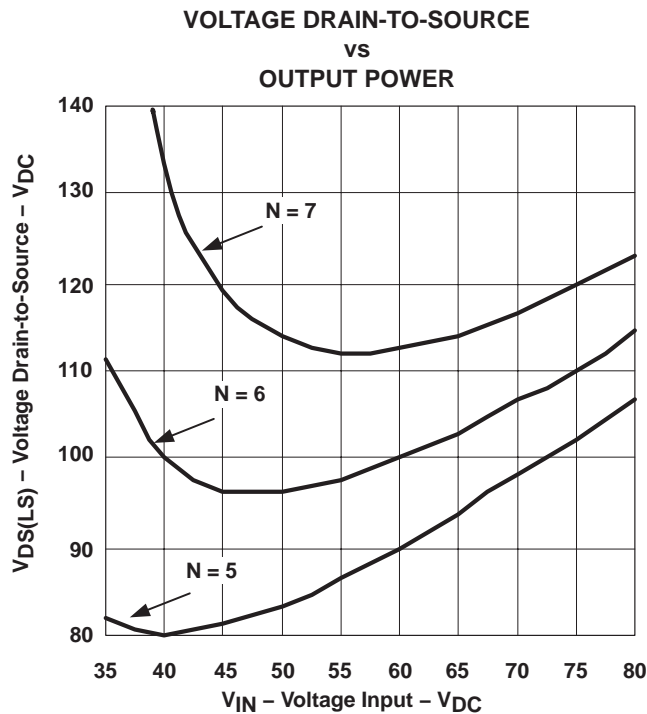
**VOLTAGE DRAIN-TO-SOURCE
vs
OUTPUT POWER**

Figure 2.

From Figure 2, notice the drastic variation in MOSFET voltage stress during minimum input voltage (maximum duty cycle, D). For this reason a PWM controller, such as the UCC2891 shown in Figure 4, must provide the capability of precisely limiting the maximum duty cycle. The consequence could be destructive voltage levels applied to the MOSFET or having to over specify the maximum MOSFET voltage rating. From an active clamp design standpoint, it can be helpful to begin the power stage design by plotting the graph shown in Figure 2. A transformer turns ratio can then be selected to yield a relatively constant $V_{DS(LS)}$ at each of the input voltage extremes. Figure 2 shows that for a typical forward converter operating over the full telecom input voltage (36 V < V_{IN} < 75 V), a turns ratio of N = 6 results in 110 V of applied drain-to-source voltage at V_{IN} = 36 V and V_{IN} = 75 V. The MOSFET voltage shown in Figure 2 is also the voltage seen by the clamp capacitor, C_{cl}. As such, the clamp capacitor must be appropriately chosen to withstand the full clamp voltage plus any additional de-rating voltage. Having chosen a turns ratio of 6, the transformer reset voltage, $V_{RESET(LS)}$, given by (8) can also be plotted against varying input voltage and is shown in Figure 3.
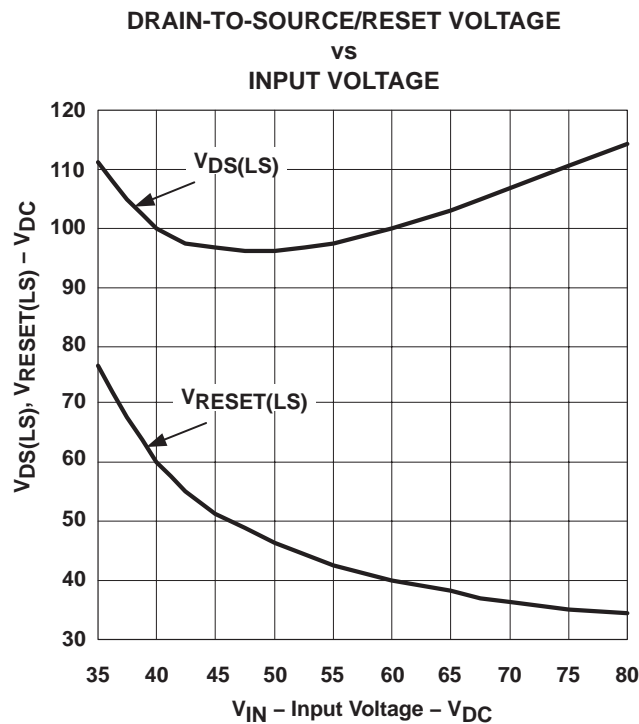
DRAIN-TO-SOURCE/RESET VOLTAGE
vs
INPUT VOLTAGE

Figure 3.

3 Gate Drive Considerations for Low-Side Clamp

Since it has already been established that the auxiliary MOSFET of a low-side clamp circuit must be a P-channel device, a negative gate drive voltage is required to fully turn this device on. However, most pulse width modulator (PWM) controllers or gate drivers do not produce output voltage levels below ground reference. Using a gate drive circuit applied to a low-side clamp such as the one shown in Figure 4, the P-channel MOSFET can be directly driven from a low-side referenced driver or PWM gate drive signal. Whether derived directly from a PWM or from a gate driver, the gate-to-source voltage of Q1, V_{OUT}, must be synchronously in phase with V_{AUX}, as shown in the timing diagram (dead-time delays not shown) of Figure 4. Using an advanced PWM controller such as the UCC2891, greatly simplifies the task of driving both MOSFET switches. Along with an internal ±2-A drive, user programmable dead-time and a precise maximum duty cycle clamp, the UCC2891 provides the exact phasing and control specifically intended for low-side active clamp applications.
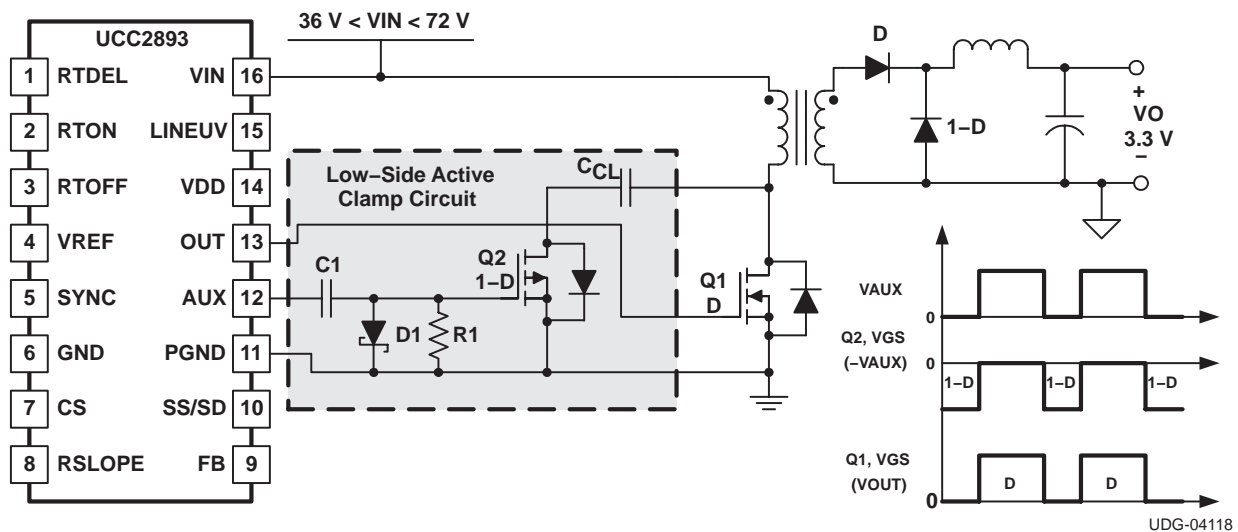

Figure 4. Low-Side Clamp and Gate Drive Circuit

The first time the PWM gate voltage, V_{AUX}, goes positive, the diode, D1, will be forward biased and the capacitor, C1, is charged to $-V_{AUX}$ volts. The capacitor voltage then discharges through R1. If the time constant of R1 and C1 equation (9) is much greater than the PWM period, then the voltage across C1 remains relatively constant and the resultant gate to source voltage seen at Q2 is $-V_{AUX}$ with a peak positive value of zero volts. Therefore, V_{AUX} is effectively shifted below ground and is now adequate for driving the gate of the P-channel MOSFET, Q2.

$$R1 \times C1 \cong \frac{100}{F_{PWM}}$$

(9)

4   High-Side Clamp

Figure 5 shows a high-side clamp applied to the same basic single-ended forward converter shown in Figure 1.
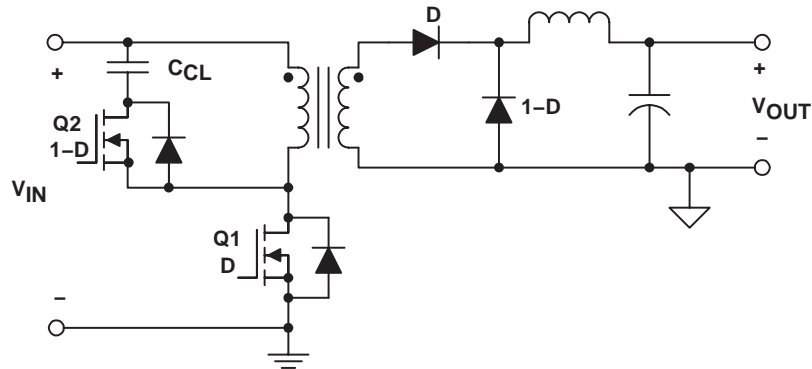
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Figure 5. High-Side Active Clamp Circuit

Similar to the low-side clamp, whenever the main MOSFET, Q1, is conducting, the full input voltage is applied across the transformer magnetizing inductance, and this is referred to as the power transfer mode. Whenever the auxiliary MOSFET, Q2, is conducting, the clamp voltage, $V_{C(HS)}$ is applied directly across the transformer magnetizing inductance and this is referred to as the transformer reset period. This is quite different than the low-side case where the clamp voltage, $V_{C(LS)}$, was applied directly across the drain-to-source junction of the main MOSFET.

The high-side clamp auxiliary MOSFET, Q2, must be an N-channel device only because of the direction of the body-diode. Similar to the low-side clamp circuit, the dominant losses in Q2 are gate charge losses, so a MOSFET is chosen with the same low gate charge considerations in mind.

Neglecting the effect of leakage inductance, the transfer function for the high-side clamp can be derived by once again applying the principle of volt-seconds balance across the transformer magnetizing inductance.

$$D \times V_{IN} = (1 - D) \times V_{C(HS)} \tag{10}$$

Simplifying (10) for the clamp voltage, $V_{C(HS)}$, gives:

$$V_{C(HS)} = \left[\frac{D}{1 - D}\right] \times V_{IN} \tag{11}$$

It is interesting to note that the transfer function given in (11) is also the same transfer function for a non-isolated flyback converter. This is why the high-side clamp is commonly referred to as a flyback-type clamp.

The result of (11) gives an expression for the transfer function between the input voltage and the clamp voltage. However, notice from Figure 5 that whenever Q2 is conducting, the clamp voltage is applied directly across the transformer primary magnetizing inductance. Therefore (11) can be extended and written to include an expression for determining the reset voltage:

$$V_{RESET(HS)} = V_{C(HS)} = \left[\frac{D}{1 - D}\right] \times V_{IN} \tag{12}$$

During the transformer reset period, the dot polarity on the transformer primary reverses, so the voltage applied to drain-to-source of the main MOSFET, Q1, can be written as:

$$V_{DS(HS)} = V_{IN} + V_{C(HS)} \tag{13}$$

If the expression for $V_{C(HS)}$ from (11) is substituted into (13) and simplified, a transfer function relating the input voltage to the main MOSFET drain-to-source voltage can be shown as:

$$V_{DS(HS)} = \left[\frac{1}{1-D}\right] \times V_{IN} \tag{14}$$

Substituting (6) into (12) and (14) and simplifying gives expressions for $V_{RESET(HS)}$ and $V_{C(HS)}$ in terms of V_{IN}, V_O and N, as shown in (15) and (16).

$$V_{RESET(HS)} = V_{C(HS)} = \frac{V_O \times V_{IN} \times N}{V_{IN} - N \times V_O} \tag{15}$$

$$V_{DS(HS)} = \frac{V_{IN}{}^2}{V_{IN} - N \times V_O} \tag{16}$$

The results of (15) can now be used to graphically show how the clamp voltage and transformer reset voltage vary with input voltage for a fixed value of V_O and a fixed transformer turns ratio, N. Using the same previous value of 4 V for V_O (3.3 V plus some additional voltage drop), the graphical results of (15) are plotted in Figure 6 and shown for various transformer ratios, N.

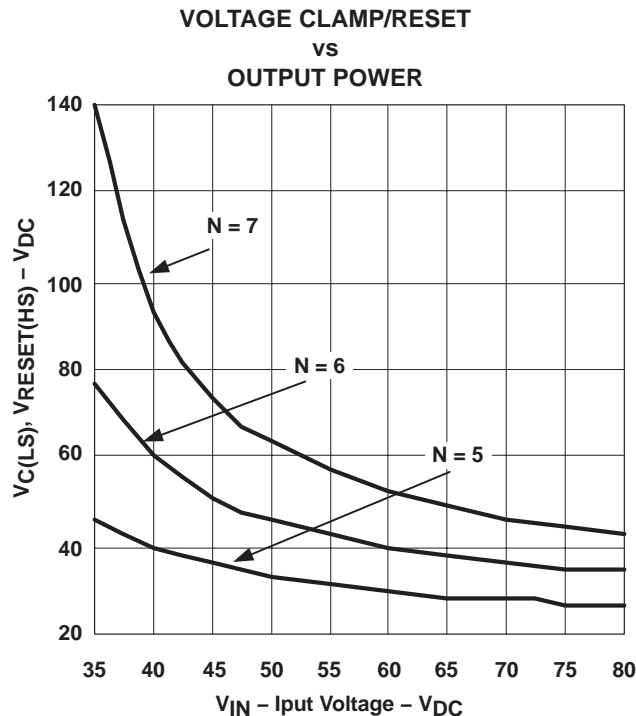**VOLTAGE CLAMP/RESET**
vs
OUTPUT POWER

Figure 6.

Since the MOSFET drain-to-source voltage given by (16) is identical to the low-side clamp, $V_{DS(LS)}$, given by (7), the graphical result for (16) can also be represented by Figure 2.

5 Gate Drive Considerations for High-Side Clamp

Unlike the low-side clamp circuit of Figure 4, the high-side clamp makes use of an N-channel auxiliary MOSFET. Assuming that the PWM controller does not have an internal high-side driver stage, a one-to-one gate drive transformer configured as shown in Figure 7 can be used. For high-side active clamp circuits, the gate-to-source voltage of Q1, V_{OUT}, must be asynchronously out of phase with V_{AUX}, as shown in the timing diagram (dead-time delays not shown) of Figure 7.

The UCC2893 Active Clamp PWM Controller is electrically and functionally equivalent to the UCC2891 shown in Figure 4, with one exception, where the UCC2891 is intended for low-side active clamp circuits, the UCC2893 provides the exact phasing and control specifically intended for high-side active clamp applications. Therefore the V_{AUX} output of the UCC2893 is out of phase with the V_{OUT} output, as shown in the timing diagram of Figure 7.
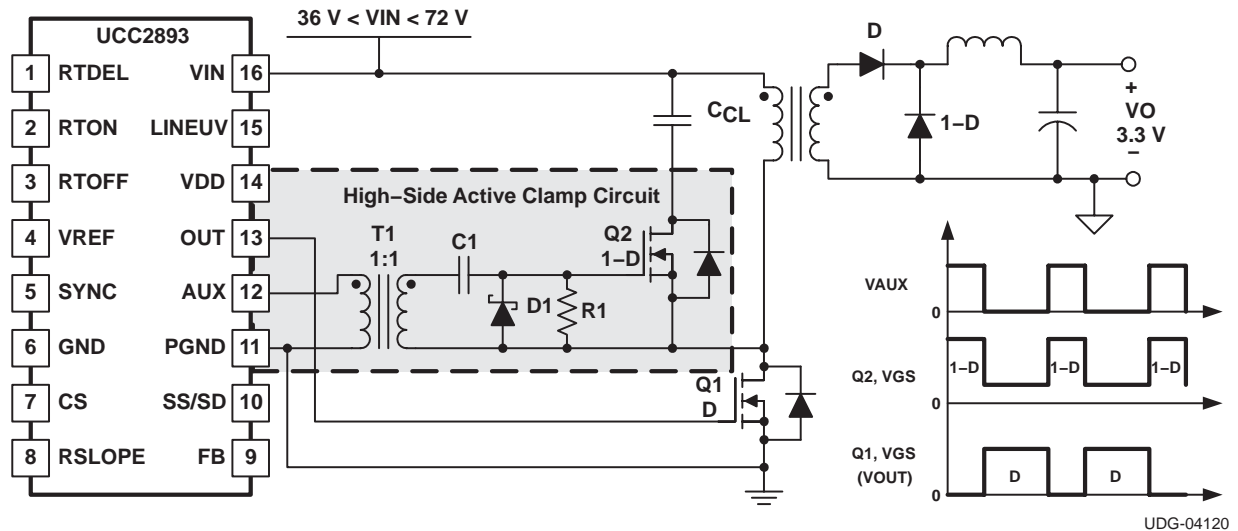

Figure 7. High-Side Clamp and Gate Drive Circuit

6   Choosing the Clamp Capacitor

Whether using a high-side or low-side active clamp circuit, the volt-seconds applied to the transformer primary must balance making the transformer reset voltage equal for each case. And since the primary MOSFET drain-to-source voltage stress and transformer reset voltage are the same for each circuit, it is the varying clamp voltage applied to across the clamp capacitor, C_{cl}, that must be considered. The details of the clamp capacitor voltage variations can be seen by comparing the difference between the clamp voltage transfer functions for each case.

$$\Delta V_C = V_{C(LS)} - V_{C(HS)} \tag{17}$$

Substituting (2) and (11) into (17), ΔV_C can be written as:

$$\Delta V_C = \left[\frac{1}{1-D}\right] \times V_{IN} - \left[\frac{D}{1-D}\right] \times V_{IN} = V_{IN} \tag{18}$$

The result of (18) shows that $V_{C(LS)}$ is greater than $V_{C(HS)}$ by V_{IN} volts. Considering the range of V_{IN} to be 36 V < V_{IN} < 72 V, a graphical comparison of $V_{C(HS)}$, $V_{C(LS)}$ and ΔV_C is shown in Figure 8.
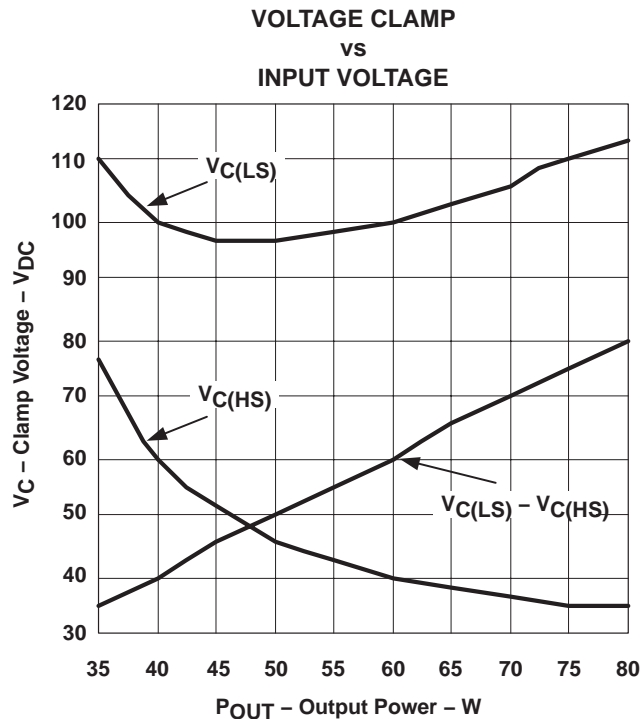

**VOLTAGE CLAMP
vs
INPUT VOLTAGE**

Figure 8.

Therefore, the first consideration for sizing the clamp capacitor is to know what the appropriate voltage rating should be over a given range of V_{IN}. The graph of Figure 8 shows that ΔV_C linearly increases with V_{IN}. For higher values of V_{IN}, the high-side clamp offers the lowest voltage stress. However the capacitor must still be selected based upon the rising clamp voltage seen at minimum V_{IN}, maximum D, which is about 80 V for this example.

The value of the clamp capacitor is primarily chosen based on the amount of allowable ripple voltage that can be tolerated. Also, it is assumed that the value of the capacitor is large enough to approximate the clamp voltage as a constant voltage source. However, according to (2) and (11) V_{cl} changes with input voltage. Whenever a line transient or sudden change in duty cycle is commanded, it will take some finite amount of time for the clamp voltage, and therefore the transformer reset voltage, to adapt. Larger capacitor values result in less voltage ripple but also introduce a transient response limitation. Smaller capacitor values result in faster transient response, at the cost of higher voltage ripple. Ideally the clamp capacitor should be selected to allow some voltage ripple, but not so much as to add excessive drain-to-source voltage stress to the main MOSFET, Q1. Allow approximately 20 percent voltage ripple while paying close attention to V_{DS} of Q1.

A simplified method for approximating C_{cl}, is to solve for C_{cl} such that the resonant time constant is much greater than the maximum off-time. While additional factors such as the power stage time constant and control loop bandwidth will also affect transient response, this approach, stated in (19), will assure that transient performance is not compromised, at least from the active clamp circuit point of view.

$$2 \times \pi \times \sqrt{L_{mag} \times C_{cl}} > 10 \times t_{OFF(max)} \tag{19}$$

By dividing both sides of (19) by the total period, T, and solving for C_{cl}, (19) can be rewritten as (20), expressing C_{cl} in terms of known design parameters:

$$C_{cl} > \frac{10 \times \left(1 - D_{MIN}\right)^2}{L_{mag} \times (2 \times \pi \times F)^2} \tag{20}$$

Once C_{cl} is calculated by (20), the final design value may vary slightly after the clamp capacitor ripple voltage is measured in circuit. Furthermore (20) is valid for the high-side and low-side active clamp circuit, so for a desired clamp ripple voltage, the clamp capacitor component value will be the same for each case.

7   Conclusion

There are similarities as well as subtle but important differences between applying the active clamp circuit to the high side verses the low side. A direct comparison between the differences and similarities are summarized for each circuit in Table 1.

The drain-to-source voltage stress, V_{DS}, on the main MOSFET, and the transformer reset voltage, V_{RESET}, are the same for both circuits. The differences between the clamp voltage transfer functions may seem minor, but each has a significant effect on the clamp capacitor selection and transformer turns ratio.

For single-ended power converter applications requiring the absolute lowest voltage stress on the clamp circuit, the high-side clamp would be the best choice. Even though the high-side clamp produces a lower overall clamp voltage, the voltage tends to rise more sharply at minimum V_{IN}, maximum duty cycle. Therefore specific attention must be paid to accurately limit the maximum allowable duty cycle so that the maximum V_{DS} of the main MOSFET is not exceeded. The high-side clamp uses an N-channel AUX MOSFET, so there are more component choices available than the low-side clamp using a P-channel device. However, the high-side clamp circuit also requires a gate drive transformer, which may come into play when absolute low cost is a primary concern.

Table 1. High/Low-Side Clamp Comparison

PARAMETER	HIGH-SIDE CLAMP	LOW-SIDE CLAMP
v_{DS}	$\left(\frac{1}{1-D}\right) \times V_{IN}$	$\left(\frac{1}{1-D}\right) \times V_{IN}$
v_{RESET}	$\left(\frac{D}{1-D}\right) \times V_{IN}$	$\left(\frac{D}{1-D}\right) \times V_{IN}$
v_C	$\left(\frac{D}{1-D}\right) \times V_{IN}$	$\left(\frac{1}{1-D}\right) \times V_{IN}$
C_{cl} (applied voltage)	Lower voltage by V_{IN} Volts Highest V_{cl} occurs at D_{MAX} Careful attention for wide V_{IN} applications	Higher voltage by V_{IN} Volts Transformer turns ratio critical at for limiting V_{cl} Careful attention for off-line, high voltage applications
C_{cl} (component value)	Same value as low side for given ripple voltage	Same value as high side for given ripple voltage
AUX MOSFET	N-Channel Must be used for 400-V (off–line) input applications	P-Channel Can't be used for 400V applications due to limited VDS rating of available devices
Gate drive	Gate drive transformer required AUX MOSFET V_{GS} out of phase with main MOSFET V_{GS} – UCC2893 PWM Controller	Simple RCD clamp gate drive AUX MOSFET V_{GS} in phase with main MOSFET V_{GS} – UCC2891 PWM Controller

Compared to the high-side counterpart, the low-side clamp yields a slightly higher but better controlled clamp voltage when the transformer turns ratio is properly selected according to Figure 2. The gate drive circuit for the low-side clamp AUX MOSFET is also simpler, since a gate drive transformer is not required. When the input voltage range is two to one or greater, the low-side clamp is a good choice since a higher duty cycle can be tolerated with less variation in clamp voltage.

Whether a high-side or low-side clamp is applied, the efficiency and performance benefits are huge compared to the better known RCD clamp and resonant reset techniques. With the advantage and flexibility of advanced PWM controllers such as the UCC2891 family, the complexities normally associated with implementing active clamp transformer reset are greatly simplified.

8   References

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