Application Report
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How to Design a Boost Converter Using LM5155

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ABSTRACT

The LM5155 is a versatile non-synchronous low-side N-FET controller for switching regulators. The common configurations for the LM5155 include boost, flyback and SEPIC regulators. This design guide focuses on how to configure and design the LM5155 as a boost regulator. This procedure is generic and focuses on selecting the correct components for boost operation. The design example was used to create the LM5155EVM-BST evaluation model and the results are presented in *LM5155EVM-BST User's Guide*. For typical applications, the LM5155 Boost Controller Quick Start Calculator can be used to efficiently complete the calculations described in this report.

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1 LM5155 Design Example

This design guide follows typical design procedures and calculations to implement a non-synchronous boost controller. The design example uses an unregulated 12V rail (6V - 18V) to produce a regulated 24V of up to 2A load current. A switching frequency of 440kHz is selected to avoid interference in the AM band (530kHz to 1.8MHz). The minimum supply voltage is selected to be 6V, which is similar to many automotive start-stop applications. Section 3 details the component selection based on the general design parameters shown in Table 1.

2 Example Application

Table 1 indicates the parameters for the example application.

Table 1. Design Parameters

PARAMETER	SPECIFICATIONS
V_{SUPPLY}	6V to 18 V
V_{LOAD}	24V
I_{LOAD}	2A
f_{SW}	440kHz
η (estimated efficiency)	90%

3 Calculations and Component Selection

This section covers the equations specific to the LM5155 to implement a boost controller that operates in continuous conduction mode. Component selection is based on the example application described in Table 1.

3.1 Switching frequency

Selecting the proper switching frequency is the first step in the design process. Higher switching frequencies yield a smaller total solution size. However, the small size comes at the cost of increased switching losses, decreasing the total efficiency regulator. Higher efficiency is achieved by selecting a relatively lower switching frequency but requires physically larger components. Harmonics of the switching frequency should be considered in designs that have strict EMC requirements. Equation 1 is used to set the frequency of the oscillator in the LM5155. The example application is selected to have a switching frequency of 440kHz

$$R_T = \frac{2.21\times10^{10}}{f_{SW}} - 955 = \frac{2.21\times10^{10}}{440kHz} - 955 = 49.2k\Omega \quad (1)$$

A standard value of 49.9kΩ is chosen for R_T.

Note that the internal oscillator of the LM5155 can be synchronized to an external clock as described in the datasheet. The LM5155 has a maximum duty cycle limit that is frequency dependent. See the LM5155 datasheet for details on step-up ratio limitations.

3.2 Inductor Calculation

Three main parameters are considered when selecting the inductance value: inductor current ripple ratio (RR), falling slope of the inductor current and the right-half plane zero frequency (ω_{Z_RHP}) of the control loop. Finding a balance between these three parameters helps simplify the rest of the design process.

- • The inductor current ripple ratio is selected to balance the copper loss and core loss of the inductor. As the relative ripple current increases; the core loss increases and the copper loss decreases
- The falling slope of the inductor current should be small enough to prevent sub-harmonic oscillation. A relatively larger inductance value results in a smaller falling slope of the inductor current. This increases the impact internal slope compensation provided by the LM5155.
- The right-half plane zero should be placed at high frequency, allowing a higher crossover frequency of the control loop. As the relative inductance value decrease the right-half plane zero frequency

increases.

A maximum ripple ratio between 30% and 70% results in a good balance between the power loss of the inductor, the down slope of the inductor current and the right-half plane zero frequency. The maximum ripple ratio of the inductor current is set to 60%. In continuos conduction mode (CCM) operation, the maximum ripple ratio occurs at a duty cycle of 33% ($D_{max\Delta IL}$=0.33). In the case that the application specification does not result in a duty cycle of 33% the maximum supply voltage is used to calculate the maximum ripple ratio. Use Equation 2 to calculate the supply voltage that results in a duty cycle of 33% (D=0.33).

$$V_{SUPPLY\_max\,\Delta IL} = V_{LOAD} \cdot \left(1 - D_{max\,\Delta IL}\right) = 24V \cdot \left(1 - 0.33\right) = 16.08V \quad (2)$$

where

- $D_{max\Delta IL}$ is the duty cycle where the maximum inductor ripple current occurs

Knowing $V_{SUPPLY\_max\Delta IL}$ the desired ripple ratio and the switching frequency, use Equation 3 to calculate the inductor value.

$$L_{M\_calc} = \frac{V_{SUPPLY}}{I_{SUPPLY} \cdot RR \cdot f_{SW}} \cdot D = \frac{16.08V}{2.985A \cdot 0.6 \cdot 440kHz} \cdot 0.33 = 6.734\mu H \quad (3)$$

where

- D is the duty cycle where the maximum inductor ripple current occurs
- RR is the ripple ratio of inductor ripple current to average supply current

A standard value of 6.8µH is selected for the value of L_M. The maximum peak inductor current occurs when the supply voltage is at the minimum value, V_{SUPPLY_min}, and the maximum load current I_{LOAD_max}. The peak inductor current is calculated using Equation 4.

$$IL_{PEAK\_MAX} = \frac{V_{LOAD} \cdot I_{OUT}}{V_{SUPPLY} \cdot \eta} + \frac{1}{2} \cdot \frac{V_{SUPPLY} \cdot D}{L_M \cdot f_{SW}} = \frac{24V \cdot 2A}{6V \cdot 0.9} + \frac{1}{2} \cdot \frac{6V \cdot 0.75}{6.8\mu H \cdot 440kHz} = 9.641A \quad (4)$$

where

- η is the estimated efficiency at the minimum supply voltage and maximum load current

The peak inductor current is used to properly size the current sense resistor, R_S.

3.3 Current Sense Resistor Calculation

Selecting the switch current sense network components is described in the following section. Figure 1 shows the four components that make up the current sense network of the LM5155. R_S is the current sense resistor. This resistor senses the switch current, and also sets the peak current limit of the inductor current. R_F and C_F form a low pass filter. This filter helps minimize high frequency noise on the current sense signal. R_{SL} sets the external slope compensation and is optional. In some applications where the internal slope compensation is not large enough R_{SL} will be required.

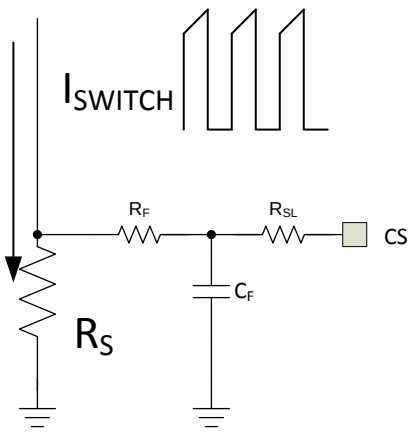

Figure 1. LM5155 Current Sense Network

3.3.1 Current Sense Resistor and Slope Compensation Resistor Selection

The current sense resistor is selected to avoid current limiting during the minimum supply voltage, V_{SUPPLY_min}, and the maximum load current, I_{LOAD_max}. Due to component tolerances and power loss of the regulator, the peak current limit should be set some margin above the calculate peak inductor current. A margin of 20% (M_{I_LIMIT}=0.2) is a good starting point. Equation 5 is used to calculate the desired peak inductor current limit value. In this design example, M_{I_LIMIT} is selected to be 20%.

$$IL_{PEAK\_LIMIT\_SET} = \left(1 + M_{I\_LIMIT}\right) \cdot IL_{PEAK\_MAX} = \left(1 + 0.2\right) \cdot 9.641A = 11.569A \tag{5}$$

where

- IL_{PEAK_MAX} is the maximum peak inductor current

Selecting the correct current sense resistor is an iterative process. The first step is to calculate the maximum current sense resistor, assuming that no external slope compensation is required (R_{SL} = 0Ω), using Equation 6.

$$R_{S\_MAX} = 1.66 \frac{V_{SL} \cdot L_M \cdot f_{SW}}{V_{LOAD} - V_{SUPPLY\_MIN}} = 1.66 \frac{40mV \cdot 6.8\mu H \cdot 440kHz}{24V - 6V} = 11.08m\Omega \tag{6}$$

where

- V_{SL} is the internal fixed internal slope compensation of the LM5155

Assuming that no external slope compensation is required, the current sense resistor value is calculated using Equation 7.

$$R_{S\_wo\_sl} = \frac{V_{CLTH}}{IL_{PEAK\_LIMIT\_SET}} = \frac{100mV}{11.569A} = 8.644m\Omega \tag{7}$$

where

- V_{CLTH} is the current limit threshold of the LM5155

If the calculated $R_{S\_wo\_sl}$ resistance value is less than the R_{S_MAX} resistance value, the $R_{S\_wo\_sl}$ is selected for the current sense resistor value (R_S). If the calculated $R_{S\_wo\_sl}$ resistance value is greater than the calculated R_{S_MAX} resistance value, there are two approaches to take; decrease the current sense resistor value or add external slope compensation.

- Decreasing the current sense resistor increases the effectiveness of the internal slope compensation. With no external slope compensation the peak inductor current limit will be constant regardless of the duty cycle. A lower current sense resistor results in a larger inductor peak current limit value, which increases the required saturation current rating of the inductor.
- Adding external slope compensation. The peak inductor current limit varies with supply voltage when external slope compensation is added.

External slope compensation is added by setting R_{SL} to a non-zero value less than 1kΩ. In applications where external slope compensation is added, R_S is calculated using Equation 8.

$$R_{S\_w\_sl} = \frac{L_M \cdot f_{sw} \cdot \left(V_{CLTH} + D \cdot V_{SLOPE}\right)}{D \cdot 0.833 \cdot \left(V_{LOAD} - V_{SUPPLY\_min}\right) + IL_{PEAK\_LIMIT\_SET} \cdot L_M \cdot f_{SW}}$$

$$R_{S\_w\_sl} = \frac{6.8\mu H \cdot 440kHz \cdot \left(100mV + 0.75 \cdot 40mV\right)}{0.75 \cdot 0.833 \cdot \left(24V - 6V\right) + 11.569A \cdot 6.8\mu H \cdot 440kHz} = 8.481m\Omega \tag{8}$$

R_{SL} is calculated using Equation 9.

$$R_{SL} = \frac{V_{CLTH} - IL_{PEAK\_LIMIT\_SET} \cdot R_{S\_w\_sl}}{I_{SLOPE} \cdot D} = \frac{100mV - 11.569A \cdot 8.481m\Omega}{30\mu A \cdot 0.75} = 83.452\Omega \tag{9}$$

where

- I_{SLOPE} is the slope compensation source of the LM5155
- D is the duty cycle at the minimum supply voltage

If the calculated R_{SL} value exceeds the maximum value of the 1kΩ, the down slope of the sensed inductor current needs to be reduce. To reduce the down slope of the inductor current, the inductance value of L_M must be increased. If the L_M inductance value is changed the current sense resistor calculations must be recalculated.

For this design example a current sense resistor value is selected to be 8mΩ (R_S), which is the nearest standard resistor value to the calculated value in Equation 7. This value is selected to keep from triggering current limit protection during load transients. No external slope compensation is required and R_{SL} is selected to be 0Ω. The peak inductor current limit is calculated using Equation 10

$$IL_{PEAK\_LIMIT} = \frac{V_{CLTH} - I_{SLOPE} \cdot R_{SL} \cdot D}{R_S} = IL_{PEAK\_LIMIT} = \frac{100mV - 30\mu A \cdot 0\Omega \cdot 0.75}{8m\Omega} = 12.5A \quad (10)$$

The peak inductor current limit is constant, regardless of the supply voltage, because there is no external slope compensation. For this design the inductor saturation current rating must be greater than 12.5A.

3.3.2 Current Sense Resistor Filter Calculation

For all designs is it recommended to add the low pass filter to the current sense signal. R_F and C_F implement this low pass filter as shown in Figure 1. The filter is added to help mitigate the impact of the leading edge spike on the current sense signal. R_F is selected to be between 10Ω and 200Ω. For this design R_F is selected to be 100Ω. C_F must be less than the value specified in Equation 11 to ensure proper operation.

$$C_F < \frac{1-D}{3 \cdot R_F \cdot f_{SW}} = \frac{1-.75}{3 \cdot 100 \cdot 440kHz} = 1.89nF \quad (11)$$

C_F is selected to be 100pF. Due to the delay of the low pass filter, the current limit is not valid when V_{SUPPLY} is greater than a given voltage calculated in. For this design the current limit is valid for the entire supply voltage range. Equation 12 is used to calculate this value.

$$V_{SUPPLY\_IL\_MAX} = V_{LOAD} \cdot \left(1 - 2 \cdot C_F \cdot R_F \cdot f_{SW}\right) = 24V \cdot \left(1 - 2 \cdot 100pF \cdot 100\Omega \cdot 440kHz\right) = 23.78V \quad (12)$$

3.4 Inductor Selection

R_S, the inductor must be selected according to three parameters; calculated inductance value (L_M), RMS inductor current at the minimum supply voltage and the peak inductor current limit (I_{LPEAK_LIMIT}) set by the current sense resistor (R_S).

- The inductance value is selected to be 6.8µH. This is a standard value that is produced by most magnetic vendors.
- The RMS current of the inductor can be estimated by calculating the average inductor current (I_{LAVG}) and is approximately equal to the average supply current. The average inductor current is estimated to be 8.89A when V_{SUPPLY} = 6V. The inductor RMS current rating should be higher than calculated average inductor current and keep the inductor temperature rise to a reasonable level based on the application.
- The saturation current rating of the inductor should be larger than the calculated I_{LPEAK_LIMIT} value, 12.5A. If the inductor becomes saturated, proper operation of the regulator is not guaranteed.

For this design example, the inductor is selected to have an inductance value of 6.8µH, 20°C component temperature rise at an RMS of 14A , and a saturation current limit of 21.8A.

3.5 Diode Selection

The diode must be rated to handle the average load current, plus some margin, while being able to dissipate the conduction losses. The voltage rating of the diode must be greater than the load voltage, V_{LOAD}. Selecting a schottky diode is recommended due to the small reverse recovery time and smaller forward voltage drop with respect to a standard fast recovery diode. For this design a 60V reverse voltage, 10A average forward current schottky diode is selected. The conducted power loss of this diode is calculated in Equation 13.

$$P_{D\_con} = V_F \cdot (1-D) \cdot I_{SUPPLY} = 480mV \cdot (1-0.75) \cdot \frac{24V \cdot 2A}{6V} = 0.96W$$

where

- V_F is the forward voltage drop of the diode (13)

3.6 MOSFET Selection

MOSFET selection focuses on power dissipation and voltage rating. Power dissipation of MOSFET is composed of two different parts, conduction losses and switching losses. Conduction losses are dominated by the $R_{DS(ON)}$ parameter of the MOSFET. Switching losses occur during the rise and fall time of the switch node, when the N-channel MOSFET is turning on and turning off. During the rise time and fall time, current and voltage are present in the channel of the MOSFET. The longer the rise and fall time of the switch node the higher the switching losses. Selecting a MOSFET with minimal parasitic capacitances lowers the switching losses. Ideally, conduction losses and switching losses should be equal during maximum load current and minimum supply voltage. details how to calculate the conduction and switching losses of the MOSFET.

The total gate charge (Q_{G_total}) must not be large enough to place the internal VCC regulator into current limit. The Q_{G_total} for a given MOSFET should be known. Equation 14 provides the maximum Q_{G_total} of the MOSFET.

$$Q_{G\_total} < \frac{35mA}{f_{SW}} \quad (14)$$

The drain to source break down voltage rating on the MOSFET needs to be higher than the load voltage, plus some margin, due to voltage spike on the switch node. The break down voltage rating should be at least 10V higher than V_{LOAD} plus V_F . V_F is the forward voltage of the rectifying diode.

For this design, a 40V MOSFET with low $R_{DS(ON)}$ low threshold voltage is selected.

3.7 Output Capacitor Selection

The output capacitor is required to smooth the load voltage ripple, provides an energy source during load transients and provides energy to the load during the on-time of the MOSFET. During the on time of the switch, the voltage across the output capacitor bank decreases. The output capacitor is appropriately sized based on the required capacitive voltage ripple during the on-time of the MOSFET.

Using the required V_{LOAD} ripple requirement, 100mV, Equation 15 is used to calculate the minimum output capacitance. The maximum on-time of the switch occurs at the minimum supply voltage. In practice, ceramic capacitors are added to reduce the total output capacitor bank ESR, reducing the high frequency load voltage ripple . Electrolytic capacitors provide bulk capacitance the is relatively constant over DC voltage ranges when compared to ceramic capacitors.

$$C_{OUT\_min} = \frac{I_{LOAD} \cdot D}{f_{SW} \cdot \Delta V_{LOAD}} = \frac{2A \cdot 0.75}{440kHz \cdot 100mV} = 14.206\mu F \quad (15)$$

The output capacitor must be rated to handle the ripple current with out being damaged or significantly reducing operating life. The maximum output ripple current is estimated using Equation 16. Ceramic capacitors generally have a relatively high RMS ripple current rating and are used to increase the total RMS current rating of the output capacitor bank.

$$I_{RMS\_COUT} = \sqrt{(1-D) \cdot \left[{I_{LOAD}}^2 \cdot \frac{D}{(1-D)^2} + \frac{\Delta IL^2}{3} \right]} = \sqrt{(1-0.75) \cdot \left[2A^2 \cdot \frac{0.75}{(1-0.75)^2} + \frac{1.504A^2}{3} \right]} = 3.49A \quad (16)$$

For this design, a total output capacitance of 200µF is selected. The capacitor bank ESR (R_{ESR}) is estimated to be around 2mΩ. The output capacitance and low R_{ESR} value help minimize the voltage drop during load transients.

3.8 Input Capacitor Selection

The input capacitors smooth the supply ripple voltage during operation. For this design and input capacitance of 100µF is selected. Assuming that low ESR, high quality ceramic capacitor are used, Equation 17 is used to calculate the maximum supply voltage ripple based on input capacitance of 100µF

$$\Delta V_{SUPPLY} = \frac{V_{LOAD}}{32 \cdot L_M \cdot C_{IN} \cdot f_{SW}^2} = \frac{24V}{32 \cdot 6.8\mu H \cdot 100\mu F \cdot 440kHz^2} = 5.6mV \quad (17)$$

The supply voltage ripple is a function of the load impedance of the supply voltage power supply. If the impedance of the input supply is large more input capacitance is required to minimize the ripple.

3.9 UVLO Resistor Selection

The external under voltage lockout (UVLO) resistors set the minimum operating voltage of the regulator. Two levels must be specified; the voltage the LM5155 starts operation ($V_{SUPPLY(ON)}$) and the voltage the LM5155 enters stand-by mode ($V_{SUPPLY(OFF)}$). In this example, $V_{SUPPLY(ON)}$ voltage is 5.8V and the $V_{SUPPLY(OFF)}$ is 5.4V. Using Equation 18, the top UVLO resistor (R_{UVLOT}) is calculated.

$$R_{UVLOT} = \frac{0.967 \cdot V_{SUPPLY(ON)} - V_{SUPPLY(OFF)}}{5\mu A} = \frac{0.967 \cdot 5.8V - 5.5V}{5\mu A} = 21.33k\Omega \quad (18)$$

A standard value of 21kΩ is selected for R_{UVLOT}. Using Equation 19 the top UVLO resistor (R_{UVLOB}) is calculated

$$R_{UVLOB} = \frac{1.5V \cdot R_{UVLOT}}{V_{SUPPLY(ON)} - 1.5V} = \frac{1.5V \cdot 21k\Omega}{5.8V - 1.5V} = 7.32k\Omega \quad (19)$$

A standard value of 7.3kΩ is selected for R_{UVLOB}

3.10 Soft-Start Capacitor Selection.

The soft-start capacitor is used to minimize and overshoot on the load voltage during the start-up of the regulator. Equation 20 is used to calculate the minimum recommended soft-start capacitor value.

$$C_{SS} > \frac{10\mu A \cdot V_{LOAD} \cdot C_{OUT}}{I_{LOAD}} = \frac{10\mu A \cdot 24V \cdot 200\mu F}{2A} = 24nF \quad (20)$$

For this design a CSS value of 100nF is selected to minimize any overshoot on the load voltage during start-up. .

3.11 Feedback Resistor Selection

The feedback resistors (R_{FBT}, R_{FBB}) set the regulated load voltage by comparing the scaled voltage to the internal voltage reference. To help limit the bias current of the feedback resistor divider, R_{FBT} is selected to be 47kΩ. Equation 21 is used to calculate the value of R_{FBB}.

$$R_{FBB} = \frac{R_{FBT}}{\frac{V_{LOAD}}{V_{REF}} - 1} = \frac{47k\Omega}{\frac{24V}{1V} - 1} = 2.04k\Omega \quad (21)$$

R_{FBB} is selected to be 2kΩ

3.12 Control Loop Compensation

There are many different strategies to set the crossover frequency of the control loop, and placing the pole and zero of the error amplifier. In this section a general technique is described to adequately stabilize the control loop for a peak current mode controlled boost regulator in continuos conduction mode operation. A type II compensation network is implemented as show in Figure 2. Type II compensation provides a programable low frequency zero and programable high frequency pole. For a detailed model of the control loop see Section 5. The loop compensation selection process is broken down into a number of distinct steps described in the following sections.

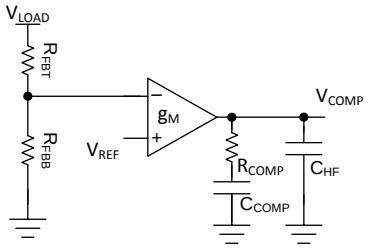

Figure 2. Type II Compensation Network

3.12.1 Select the Loop Crossover Frequency (f_{CROSS})

The crossover frequency of the loop is either selected to be 1/10th the switching frequency or 1/5th the right-half plane zero frequency, which ever is lower. Equation 22 shows the calculation for 1/10th the switching frequency. Equation 23 shows how to calculate the 1/5th the right half plane zero frequency.

$$f_{CROSS} = \frac{f_{SW}}{10} = \frac{440kHz}{10} = 44kHz \tag{22}$$

$$f_{CROSS} = \frac{f_{Z\_RHP}}{5} = \frac{R_{LOAD}\left(D'\right)^2}{5 \cdot 2 \cdot \pi \cdot L_M} = \frac{12\Omega\left(0.25\right)^2}{5 \cdot 2 \cdot \pi \cdot 6.8\mu H} = 3.5kHz \tag{23}$$

where

- D' is (1 -D) a the minimum supply voltage
- R_{LOAD} is the load resistance equal to V_{LOAD}/I_{LOAD}

The crossover frequency is selected to be 1/5th the right half plane zero frequency, 3.5kHz

3.12.2 Determine Required R_{COMP}

The R_{COMP} value directly affects the crossover frequency of the control loop. The higher the crossover frequency, the faster the control loop reacts to transient conditions. Knowing the desired loop crossover frequency, 3.5kHz, R_{COMP} is calculate using Equation 24.

$$R_{COMP} = \frac{2 \cdot \pi \cdot C_{OUT} \cdot R_{CS} \cdot {V_{LOAD}}^2 \cdot f_{CROSS}}{G_{COMP} \cdot g_m \cdot V_{SUPPLY\_min}} = \frac{2 \cdot \pi \cdot 200\mu F \cdot 8m\Omega \cdot 24V^2 \cdot 3.5kHz}{G_{COMP} \cdot g_m \cdot 6V} = 11.93k\Omega \tag{24}$$

where

- g_m is the transconductance of the error amplifier, 2mA/V
- G_{COMP} is COMP to PWM gain, 0.142V/V

R_{COMP} is selected to be 11.3kΩ. Decreasing the R_{COMP} resistance value lowers the crossover frequency but helps ensure the control loop remains stable over the specified supply voltage range.

3.12.3 Determine Required C_{COMP}

The R_{COMP} resistor and C_{COMP} capacitor set the low frequency zero of the compensation network resulting in a phase boost. Placement of this zero frequency largely impacts the transient response of the control loop. A good strategy is placing the zero directly in between the crossover frequency (f_{CROSS}) and the low frequency pole of the plant. Equation 25 places the low frequency zero of error amplifier a the geometric mean of f_{CROSS} and low frequency pole of the plant (ω_{P_LF}). For this design the desired zero location is 682 Hz.

$$f_{Z\_EA} = \sqrt{f_{CROSS} \cdot \frac{2}{2\pi \cdot C_{OUT} \cdot R_{LOAD}}} = \sqrt{3.5kHz \cdot \frac{2}{2\pi \cdot 200\mu F \cdot 12\Omega}} = 682Hz \tag{25}$$

With the zero frequency selected, Equation 26 produces the value of C_{COMP}.

$$C_{COMP} = \sqrt{\frac{C_{OUT} \cdot R_{LOAD}}{4 \cdot \pi \cdot {R_{COMP}}^2 \cdot f_{CROSS}}} = \sqrt{\frac{200\mu F \cdot 12\Omega}{4 \cdot \pi \cdot 11.3k\Omega^2 \cdot 3.5kHz}} = 20.64nF \quad (26)$$

C_{COMP} is chosen to be 22nF.

3.12.4 Determine Required C_{HF}

The C_{HF} capacitor sets the high frequency pole of the compensation network. The high frequency pole aids in attenuating high frequency noise due to the switching frequency and assuring enough gain margin achieved. It is recommended to set the pole frequency between or between the RHP zero (ω_{Z_RHP}) and half the switching frequency. Equation 27 is used to calculate the value of C_{HF}.

$$C_{HF} = \frac{C_{COMP} \cdot L_M}{C_{COMP} \cdot D'^2 \cdot R_{OUT} \cdot R_{COMP} - L_M} = \frac{22nF \cdot 6.8\mu H}{22nF \cdot 0.5^2 \cdot 12\Omega \cdot 11.3k\Omega - 6.8\mu H} = 200pF \quad (27)$$

C_{HF} is chosen to be 220pF.

3.13 Efficiency Estimation

The total loss of the boost converter (P_{TOTAL}) can be expressed as the sum of the losses in the device (P_{IC}), MOSFET power losses (P_Q), diode power losses (P_D), inductor power losses (P_L), and the loss in the sense resistor (P_{RS}).

$$P_{TOTAL} = P_{IC} + P_Q + P_D + P_L + P_{RS}[W] \quad (28)$$

P_{IC} can be separated into gate driving loss (P_G) and the losses caused by quiescent current (P_{IQ}).

$$P_{IC} = P_G + P_{IQ}[W] \quad (29)$$

Each power loss is approximately calculated as follows:

$$P_G = Q_{G(@VCC)} \times V_{BIAS} \times F_{SW}[W] \quad (30)$$

$$P_{IO} = V_{BIAS} \times I_{BIAS}[W] \quad (31)$$

I_{BIAS} values in each mode can be found in the LM5155 datasheet.

P_Q can be separated into switching loss ($P_{Q(SW)}$) and conduction loss ($P_{Q(COND)}$).

$$P_Q = P_{Q(SW)} + P_{Q(COND)}[W] \quad (32)$$

Each power loss is approximately calculated as follows:

$$P_{Q(SW)} = 0.5 \times (V_{LOAD} + V_F) \times I_{SUPPLY} \times (t_R + t_F) \times F_{SW} \quad (33)$$

t_R and t_F are the rise and fall times of the low-side N-channel MOSFET device. I_{SUPPLY} is the input supply current of the boost converter.

$$P_{Q(COND)} = D \times {I_{SUPPLY}}^2 \times R_{DS(ON)}[W] \quad (34)$$

$R_{DS(ON)}$ is the on-resistance of the MOSFET and is specified in the MOSFET data sheet. Consider the $R_{DS(ON)}$ increase due to self-heating.

P_D can be separated into diode conduction loss (P_{VF}) and reverse recovery loss (P_{RR}).

$$P_D = P_{VF} + P_{RR}[W] \quad (35)$$

Each power loss is approximately calculated as follows:

$$P_{VF} = (1 - D) \times V_F \times I_{SUPPLY}[W] \quad (36)$$

$$P_{RR} = V_{LOAD} \times Q_{RR} \times F_{SW}[W] \quad (37)$$

Q_{RR} is the reverse recovery charge of the diode and is specified in the diode datasheet. Reverse recovery characteristics of the diode strongly affect efficiency, especially when the load voltage is high.

P_L is the sum of DCR loss (P_{DCR}) and AC core loss (P_{AC}). DCR is the DC resistance of inductor which is mentioned in the inductor data sheet.

$$P_L = P_{DCR} + P_{AC}[W] \quad (38)$$

Each power loss is approximately calculated as follows:

$$P_{DCR} = I_{SUPPLY}^{2} \times R_{DCR}[W] \quad (39)$$

$$P_{AC} = K \times \Delta I^{\beta} F_{SW}^{\alpha}[W] \quad (40)$$

$$\Delta I = \frac{V_{SUPPLY} \times D \times \frac{1}{F_{SYNC}}}{L_M} \quad (41)$$

ΔI is the peak-to-peak inductor current ripple. K, α, and β are core dependent factors which can be provided by the inductor manufacturer.

P_{RS} is calculated as follows:

$$P_{RS} = D \times I_{SUPPLY}^{2} \times R_S[W] \quad (42)$$

Efficiency of the power converter can be estimated as follows:

$$\text{Efficiency} = \frac{V_{LOAD} \times I_{LOAD}}{P_{TOTAL} + V_{LOAD} \times I_{LOAD}} \times 100[\%] \quad (43)$$

4 Component Selection Summary

Please see the *LM5155EVM-BST User's Guide* for more testing results.

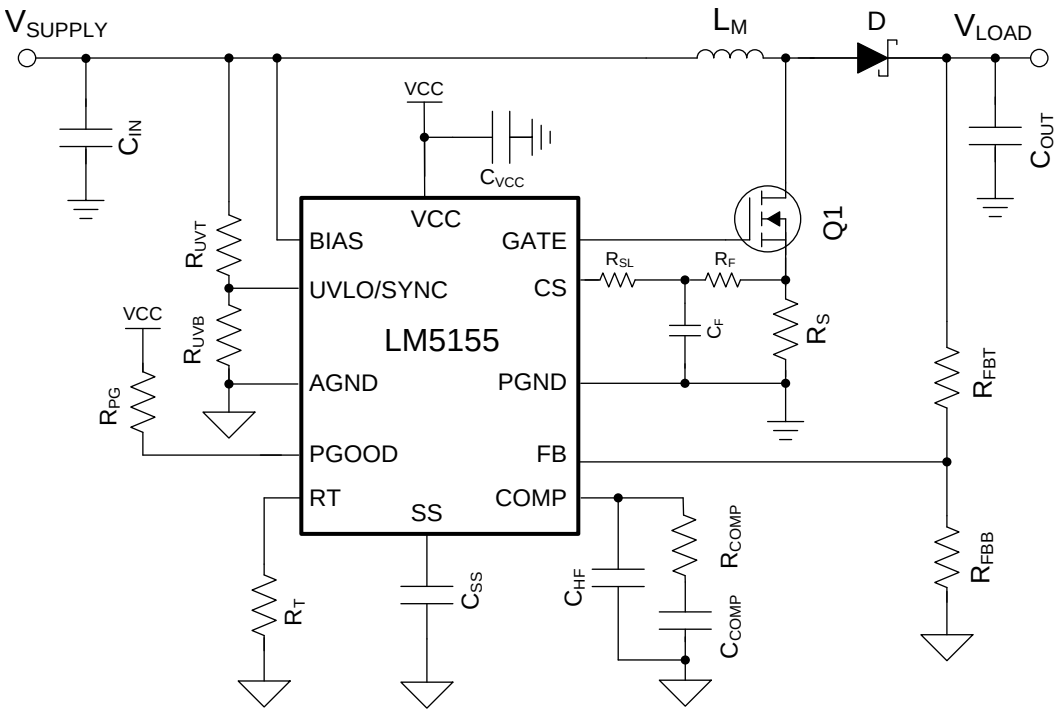

Figure 3. Application Circuit

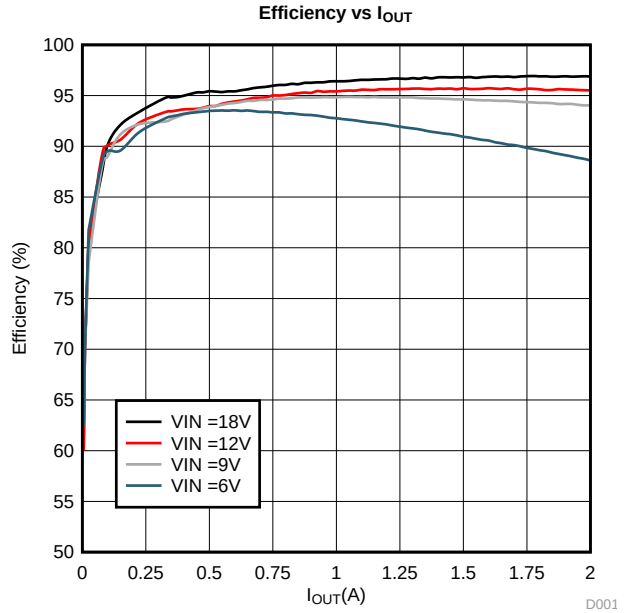

Figure 4. Efficiency vs I_{OUT}

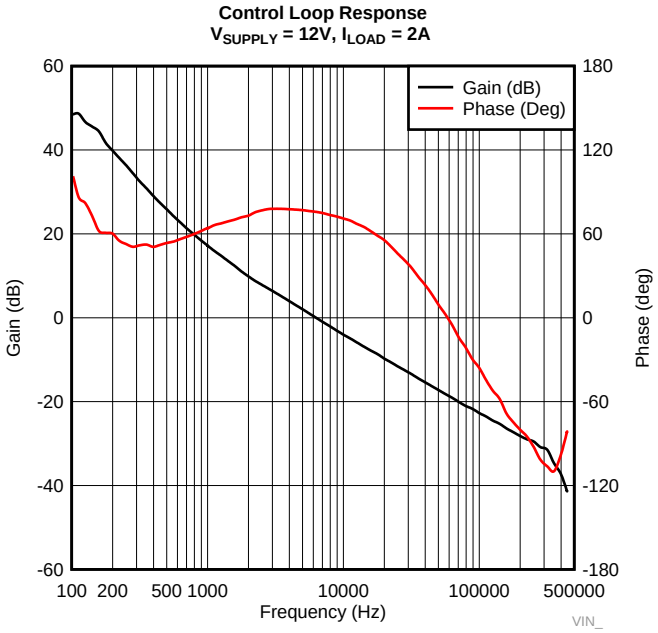

Figure 5. Control Loop Response V_{SUPPLY} = 12V I_{LOAD} = 2A

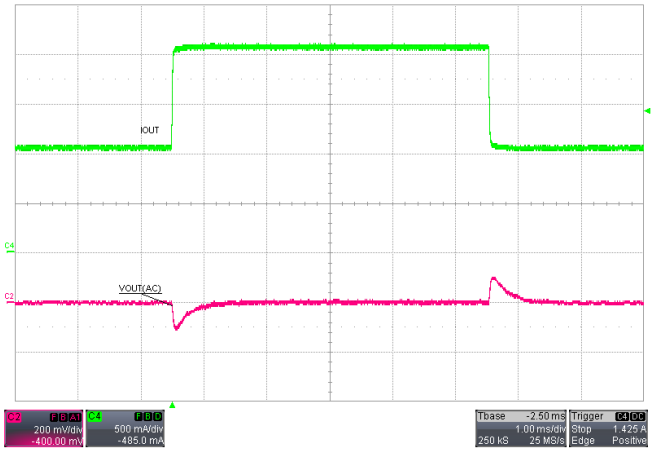

Figure 6. Figure 6. Load Step: I_{LOAD} 1A to 2A, V_{SUPPLY} =12V

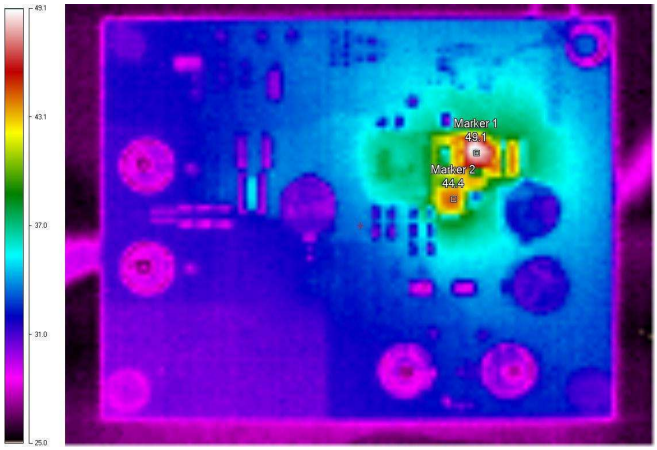

Figure 7. Thermal Image: V_{SUPPLY} = 6V, I_{LOAD} =2A

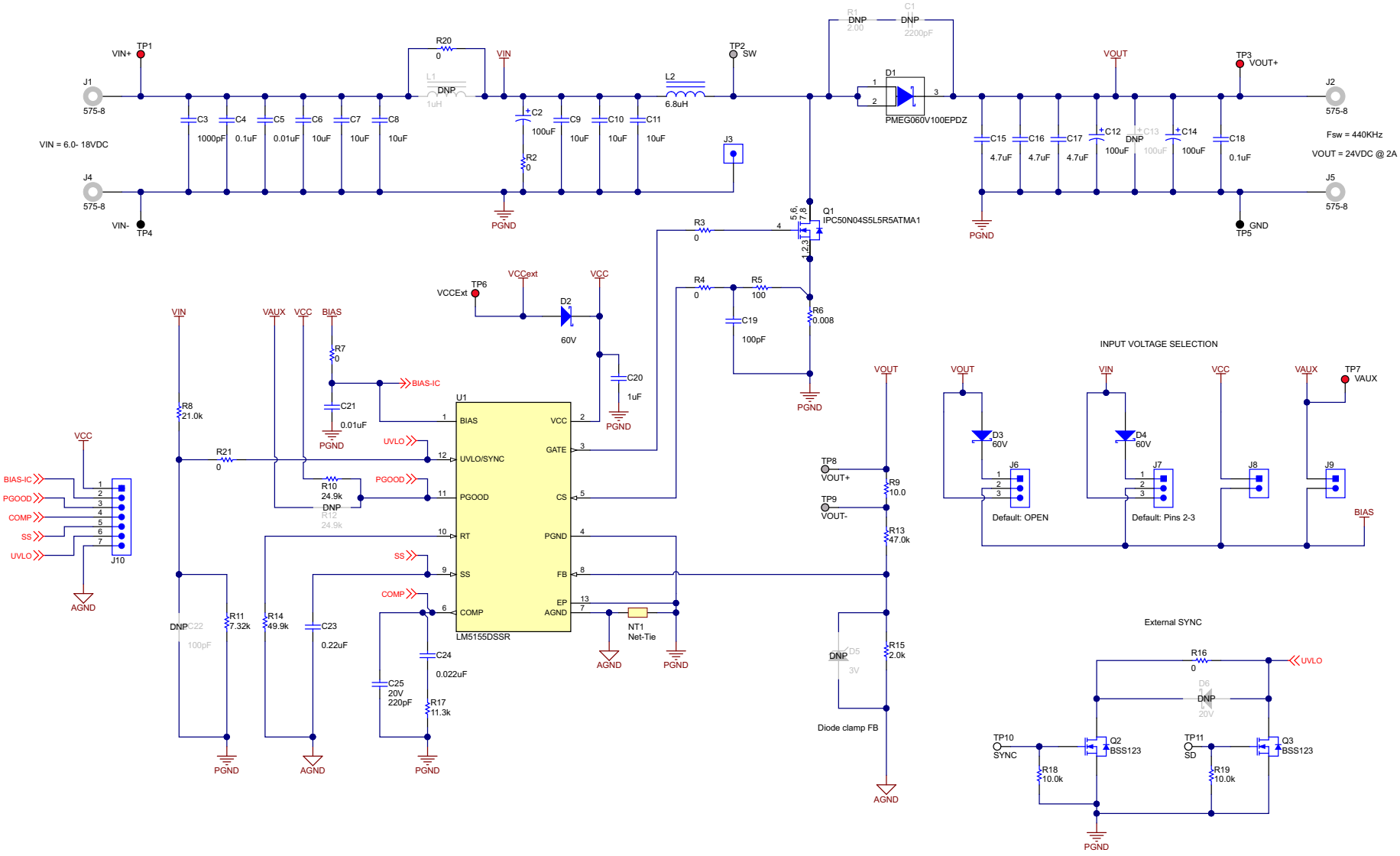

Figure 8. LM5155EVM-BST Schematic

Table 2. List of Materials

REFERENCE DESIGNATOR	QTY.	SPECIFICATION	MANUFACTURER	PART NUMBER
R_T	1	RES, 49.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060349K9FKEA
R_{FBT}	1	RES, 22.0 k, 1%, 0.1 W, 0603	Yageo America	RC0603FR-0722KL
R_{FBB}	1	RES, 2.43 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06032K43FKEA
L_M	1	Shielded, Composite, 1.2 uH, 26.3 A, 0.0025 ohm, AEC-Q200 Grade 1, SMD	Coilcraft	XAL1060-122MEB
R_S	1	RES, 0.003, 1%, 3 W, AEC-Q200 Grade 0, 2512 WIDE	Susumu Co Ltd	KRL6432E-M-R003-F-T1
R_{SL}	1	RES, 0, 5%, 0.1 W, 0603	Yageo America	RC0603JR-070RL
C_{OUT1}	3	'CAP, CERM, 4.7 uF, 50 V, +/- 10%, X7R, 1210	TDK	C3225X7R1H475K250AB
C_{OUT2} (Bulk)	1	CAP, Polymer Hybrid, 100 uF, 50 V, +/- 20%, 28 ohm, 10x10 SMD	Panasonic	EEHZC1H101P
C_{IN1}	6	CAP, CERM, 10 uF, 50 V, +/- 10%, X7R, 1210	MuRata	GRM32ER71H106KA12L
C_{IN2} (Bulk)	1	CAP, Polymer Hybrid, 100 uF, 50 V, +/- 20%, 28 ohm, 10x10 SMD	Panasonic	EEHZC1H101P
Q1	1	MOSFET, N-CH, 60 V, 100 A, AEC-Q101, SOT669	Nexperia	BUK9Y6R0-60E,115
D1	1	Schottky, 60 V, 10 A, AEC-Q101, CFP15	Nexperia	PMEG060V100EPDZ
R_{COMP}	1	RES, 2.21 k, 1%, 0.1 W, 0603	Yageo America	RC0603FR-072K21L
C_{COMP}	1	CAP, CERM, 0.047 uF, 25 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	MuRata	GCM188R71E473KA37D
C_{HF}	1	CAP, CERM, 2200 pF, 25 V, +/- 10%, X7R, 0603	MuRata	GRM188R71E222KA01D
R_{UVLOT}	1	RES, 24.9 k, 1%, 0.1 W, 0603	Yageo America	RC0603FR-0724K9L
R_{UVLOB}	1	RES, 76.8 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060376K8FKEA
R_{UVLOS}	0	N/A	N/A	N/A
C_{SS}	1	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0603	TDK	C1608X7R1H104K080AA
D_G	0	N/A	N/A	N/A
R_G	1	RES, 0, 5%, 0.1 W, 0603	Yageo America	RC0603JR-070RL
C_F	1	CAP, CERM, 100 pF, 50 V,+/- 1%, C0G/NP0, 0603	Kemet	C0603C101F5GACTU
R_F	1	RES, 100, 1%, 0.1 W, 0603	Yageo America	RC0603FR-07100RL
R_{SNB}	0	N/A	N/A	N/A
C_{SNB}	0	N/A	N/A	N/A
R_{BIAS}	1	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Panasonic	ERJ-3GEY0R00V
C_{BIAS}	1	CAP, CERM, 0.01 uF, 50 V, +/- 10%, X7R, 0603	Samsung Electro-Mechanics	CL10B103KB8NCNC
C_{VCC}	1	CAP, CERM, 1 uF, 16 V, +/- 20%, X7R, AEC-Q200 Grade 1, 0603	MuRata	GCM188R71C105MA64D
R_{PG}	1	RES, 24.9 k, 1%, 0.1 W, 0603	Yageo America	RC0603FR-0724K9L

5 Small Signal Frequency Analysis

This section provides detailed equations used to model the control loop when the LM5155 is configured as a boost regulator. These equations are only valid when the regulator is operating in continuous conduction mode. The simplified formulas allow for quick evaluation of the control loop, but loose accuracy at high frequencies. The comprehensive formulas are more complex but provide better accuracy at high frequencies.

5.1 Boost Regulator Modulator Modeling

These equations model the plant of a peak current mode boost regulator in continuous conduction mode.

Table 3. Control Loop Equations

	Simplified Formula	Comprehensive Formula
Modulator Equations		
Modulator Transfer Function	$\frac{\hat{v}_{LOAD}(s)}{\hat{v}_{COMP}(s)} = A_M \frac{\left(1+\frac{s}{\omega_{Z\_ESR}}\right)\left(1-\frac{s}{\omega_{Z\_RHP}}\right)}{\left(1+\frac{s}{\omega_{P\_LF}}\right)}$ (44)	$\frac{\hat{v}_{LOAD}(s)}{\hat{v}_{COMP}(s)} = A_M \frac{\left(1+\frac{s}{\omega_{Z\_ESR}}\right)\left(1-\frac{s}{\omega_{Z\_RHP}}\right)}{\left(1+\frac{s}{\omega_{P\_LF}}\right)\left(1+\frac{s}{Q\cdot\omega_n}+\frac{s^2}{\omega_n^2}\right)}$ (45)
Modulator DC Gain	$A_M = G_{COMP}\frac{R_{LOAD}}{A_{CS}\cdot R_S}\times\frac{D'}{2}$ (46)	
RHP Zero	$\omega_{Z\_RHP} = \frac{R_{LOAD}\left(D'\right)^2}{L_M}$ (47)	
ESR Zero	$\omega_{Z\_ESR} = \frac{1}{C_{OUT}\cdot R_{ESR}}$ (48)	
Low Frequency Pole	$\omega_{P\_LF} = \frac{2}{C_{OUT}\cdot R_{LOAD}}$ (49)	
Sub-Harmonic Double Pole	Not Considered	$\omega_n = \pi\cdot f_{sw}$ (50)
Quality Factor	Not Considered	$Q = \frac{1}{\pi\left[D'\cdot\left(1+\frac{s_e}{s_n}\right)-\frac{1}{2}\right]}$ (51)
Slope Compensation	Not Considered	$s_e = \left(V_{SLOPE}+I_{SLOPE}\cdot R_{SL}\right)\cdot f_{sw}$ (52)
Sensed Rising Inductor Slope	Not Considered	$s_n = \frac{V_{SUPPLY}\cdot R_S\cdot A_{CS}}{L_M}$ (53)

5.2 Compensation Modeling

These equations model a type II compensation network implemented using a transconductance error amplifier.

Table 4. Compensation Modeling Equations

	Simplified Formula	Comprehensive Formula
Feedback Equations		
Feedback Transfer Function	$\frac{\hat{v}_{COMP}(s)}{\hat{v}_{LOAD}(s)} = -A_{FB}\frac{\left(1+\frac{s}{\omega_{Z\_EA}}\right)}{s\cdot\left(1+\frac{s}{\omega_{P\_EA}}\right)}$ (54)	

Table 4. Compensation Modeling Equations (continued)

	Simplified Formula	Comprehensive Formula
Feedback Equations		
Feedback DC Gain	$A_{FB} = \frac{R_{FBB} \cdot g_m}{(R_{FBB} + R_{FBT}) \cdot C_{COMP}}$ (55)	$A_{FB} = \frac{R_{FBB} \cdot g_m}{(R_{FBB} + R_{FBT}) \cdot (C_{COMP} + C_{HF})}$ (56)
Low Frequency Zero	$\omega_{Z\_EA} = \frac{1}{R_{COMP} \cdot C_{COMP}}$ (57)	$\omega_{Z\_EA} = \frac{1}{R_{COMP} \cdot C_{COMP}}$ (58)
High Frequency Pole	$\omega_{P\_EA} = \frac{1}{R_{COMP} \cdot C_{HF}}$ (59)	$\omega_{P\_EA} = \frac{C_{COMP} + C_{HF}}{R_{COMP} \cdot C_{COMP} \cdot C_{HF}}$ (60)
Mid-band Gain	$G_{MID} = \frac{R_{COMP} \cdot R_{RFBB} \cdot g_m}{(R_{FBB} + R_{FBT})}$ (61)	$G_{MID} = \frac{C_{COMP} \cdot R_{COMP} \cdot R_{RFBB} \cdot g_m}{(C_{HF} + C_{COMP}) \cdot (R_{FBB} + R_{FBT})}$ (62)

5.3 Open Loop Modeling

These equations model the open loop transfer function of the control loop.

Table 5. Open Loop Modeling Equations

	Simplified Formula	Comprehensive Formula
Open Loop Equations		
Open Loop Transfer Function	$T(s) = A_M \cdot A_{FB} \cdot \frac{\left(1 + \frac{s}{\omega_{Z\_ESR}}\right)\left(1 - \frac{s}{\omega_{Z\_RHP}}\right)}{\left(1 + \frac{s}{\omega_{P\_LF}}\right)} \cdot \frac{\left(1 + \frac{s}{\omega_{Z\_EA}}\right)}{s \cdot \left(1 + \frac{s}{\omega_{P\_EA}}\right)}$ (63)	$T(s) = A_M \cdot A_{FB} \cdot \frac{\left(1 + \frac{s}{\omega_{Z\_ESR}}\right)\left(1 - \frac{s}{\omega_{Z\_RHP}}\right)}{\left(1 + \frac{s}{\omega_{P\_LF}}\right)\left(1 + \frac{s}{Q \cdot \omega_n} + \frac{s^2}{\omega_n^2}\right)} \cdot \frac{\left(1 + \frac{s}{\omega_{Z\_EA}}\right)}{s \cdot \left(1 + \frac{s}{\omega_{P\_EA}}\right)}$ (64)
Crossover Frequency	$f_{CROSS} = \frac{G_{COMP} \cdot V_{SUPPLY} \cdot g_m \cdot R_{COMP}}{2\pi \cdot A_{CS} \cdot R_{CS} \cdot C_{OUT} \cdot V_{LOAD}^2}$ (65)	Use Bode Plot

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