Application Note

How to Design an Isolated Flyback Converter Using LM5157x/LM5158x

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ABSTRACT

The LM5157x/LM5158x device is a wide-input range, non-synchronous converter with an integrated power MOSFET. The commonly supported configurations include Boost, Flyback and SEPIC topologies. This report focuses on designing the LM5157x/LM5158x as a primary side regulated (PSR) flyback converter. The design procedure is generic on selecting suitable components of the PSR flyback converter for the given application specification. The LM5175EVM-FLY evaluation module is used as the example to illustrate the design procedure, and the circuit performance results are also presented in the LM5157EVM-FLY User's Guide. For typical applications the LM5157/58 Flyback Controller Quick Start Calculator can also be used to efficiently complete the calculations described in this report.

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Trademarks

1 Introduction

The typical design procedures and calculations to implement an isolated nonsynchronous flyback controller operating in continuous conduction mode are presented in this report. The design example produce multiple output voltage rails for typical applications of the 3-phase inverter gate driver bias supplies. The converter can provide a regulated output of 10 V at 250 mA from an input of 8 V to 16 V, and three isolated and cross-regulated 20-V rails at 75 mA, 75 mA, and 150 mA, respectively.

2 Example Application

Table 2-1 shows the specification for the example application.

Table 2-1. Application Specification

Parameter	
V_{SUPPLY}	8 V to 16 V
V_{LOAD1}	10 V
I_{LOAD1}	250 mA
V_{LOAD2}	20 V
I_{LOAD2}	75 mA
V_{LOAD3}	20 V
I_{LOAD3}	75 mA
V_{LOAD4}	20 V
I_{LOAD4}	150m A
P_{OUT_total}	8.5 W
f_{SW}	250 kHz

3 Calculations and Component Selection

This section covers the equations for the selections of the external components against the application specification given in Table 2-1. Depending on the operating voltage range and power level, designing with the LM51571, LM5158 and LM51581, which maybe more suitable, can use the same equations with given application specifications.

Figure 4-1 shows the PSR flyback converter topology implemented with the LM5157 to produce a regulated voltage rail and three isolated voltage rails as specified in Table 2-1.

3.1 Switching Frequency

Selecting the switching frequency is the first step in the design process. Higher switching frequencies yields a smaller total solution size. However, the small size comes at the cost of increased switching losses, decreasing the efficiency of the converter. Higher efficiency is achieved by selecting a relatively lower switching frequency but requires physically larger components. Harmonics of the switching frequency should be considered in designs that have strict EMC requirements. Equation 1 is used to set the frequency of the internal oscillator of the LM5157x/LM5158x. The example application is selected to have a switching frequency of 250 kHz.

$$R_T = \frac{2.21 \times 10^{10}}{f_{SW}} - 955 = \frac{2.21 \times 10^{10}}{250kHz} - 955 = 87.45k\Omega \quad (1)$$

A standard value of 86.6 kΩ is chosen for R_T.

Note that the internal oscillator of the LM5157x/LM5158x can be synchronized to an external clock as described in the data sheet. The LM5157x/LM5158x has a maximum duty cycle limit that is frequency dependent. See the LM5157x/LM5158x data sheet for details on the maximum duty cycle limit.

3.2 Transformer Selection

In a flyback regulator, selecting the proper transformer for any application is a critical step. The first decision is to select the correct switching type of operation for the application, discontinuous conduction mode (DCM) or

continuous conduction mode (CCM). CCM is selected for this design to minimize the primary side RMS currents, maximize full load efficiency while minimizing load voltage ripple.

3.2.1 Maximum Duty Cycle and Turns Ratio Selection

In CCM operation the duty cycle of the low side switch is calculated using Equation 2.

$$D = \frac{\frac{N_P}{N_S} \times |V_{LOAD}|}{V_{SUPPLY} + \frac{N_P}{N_S} \times |V_{LOAD}|} \quad (2)$$

where

- N_P is the number of turns on the primary side winding and assumed to be 1
- N_S is the number of turns on the secondary side winding.

The maximum duty cycle occurs when the supply voltage is at the minimum value. By selecting the maximum duty cycle, the number of turns on the secondary winding can be determined. Selecting the duty cycle to be less than 50% brings two main benefits. First, it reduces the need for slope compensation which is required for stable operation when the duty cycle is greater than 50% in CCM operation. As for some wide input voltage designs limiting the duty cycle below 50% might not be possible, the LM5157x/LM5158x provides programmable slope compensation for such designs. Second, the right-half plane zero (RHPZ) of the converter is pushed to a higher frequency when designing with a smaller duty cycle, this helps to improve the load transient response and simplifying the control loop compensation calculations. For this design the maximum duty cycle (D_{MAX}) is selected to be 50%. The number of turns on the secondary winding is calculated using Equation 3.

$$N_{S\_calc} = \frac{(|V_{LOAD}|) \times (1 - D_{MAX}) \times N_P}{V_{SUPPLY\_min} \times D_{MAX}} = \frac{(|10V|) \times (1 - 0.5) \times 1}{8V \times 0.5} = 1.25 \quad (3)$$

Selecting N_{S1} to be 1.2 turns the turns ratio to achieved in the fewest number of full turns. The other secondary windings N_{Sx} are selected to be:

Winding	Turns
N_{S1}	1.2
N_{S2}	2.4
N_{S3}	2.4
N_{S4}	2.4

In this example the minimum number of turns is 5 on the primary winding and 6 turns on the first secondary winding. With N_{S1} selected, Equation 4 is used to calculate the maximum duty cycle.

$$D_{MAX} = \frac{\frac{N_P}{N_S} \times |V_{LOAD}|}{V_{SUPPLY\_min} + \frac{N_P}{N_S} \times |V_{LOAD}|} = \frac{\frac{1}{1.2} \times 10V}{8V + \frac{1}{1.2} \times 10V} = 0.51 \quad (4)$$

D_{MAX} is calculated to be approximately 50.1%, which is a little bit above the target maximum duty cycle of 50%. The number of turns on the auxiliary winding is calculated using Equation 5.

$$N_{S2\_calc} = N_{S1} \times \frac{|V_{LOAD2}|}{|V_{LOAD1}|} = 1.2 \times \frac{20V}{10V} = 2.4 \quad (5)$$

where

- V_{Load1} is the Load1 winding voltage

3.2.2 Primary Winding Inductance Selection

Three main parameters are considered when selecting the inductance value of primary winding: primary winding current ripple ratio (IL_{RR}), falling slope of the transformer current and the RHPZ frequency (ω_{Z_RHP}). Finding a balance between these three parameters helps to simplify the rest of the design process.

- The primary winding ripple current ripple ratio is selected to balance the copper loss and core loss of the transformer. As the relative ripple current increases; the core losses increase and the copper losses decrease.
- The falling slope of the transformer current should be small enough to prevent sub-harmonic oscillation in applications with a duty cycle greater than 50%. A relatively larger inductance value of the primary winding results in a smaller falling slope. The LM5157x/LM5158x provides fixed internal slope compensation as well as programmable slope compensation for these applications.
- The right half plane zero should be placed at high frequency, allowing for a higher crossover frequency of the control loop. As the relative inductance value of the primary winding decreases the right half plane zero frequency increases.

A maximum ripple ratio between 30% and 70% results in a good balance of the total power loss of the transformer, matching the down slope of the transformer current to the internal slope compensation and the increasing the right half plane zero frequency. The maximum ripple ratio of the inductor current is set to 60%. In CCM operation, the maximum primary winding ripple current occurs when the supply voltage is at the maximum value. For this application we choose CCM at the minimum input voltage and DCM for the higher voltage range. The primary winding inductance value for CCM operation is calculated using Equation 6.

$$L_{M\_calc} = \frac{{N_P}^2 \times {V_{SUPPLY}}^2 \times {V_{LOAD}}^2}{IL_{RR} \times f_{SW} \times P_{OUT\_total} \times (N_S \times V_{SUPPLY} + N_P \times |V_{LOAD}|)^2} \tag{6}$$

$$L_{M\_calc} = \frac{1^2 \times 8V^2 \times 10V^2}{0.6 \times 250kHz \times 8.5W \times (1.2 \times 8V + 1 \times 10V)^2} = 13.1\mu H$$

where

- IL_{RR} is the ripple ratio
- V_{SUPPLY} is the minimum supply voltage
- P_{OUT_total} is the maximum power delivered by the flyback regulator

The primary winding inductance is selected to be 8µH. The primary winding ripple current and primary winding peak current are calculated using Equation 7 and Equation 8, respectively. The peak primary winding current occurs at the minimum supply voltage.

$$\Delta IL_M = \frac{V_{SUPPLY\_min} \times D}{L_M \times f_{SW}} = \frac{8V \times 0.51}{8\mu H \times 250kHz} = 2.04A \tag{7}$$

$$IL_{PEAK} = \frac{P_{OUT\_total}}{V_{SUPPLY\_min} \times D} + \frac{\Delta IL_M}{2} = \frac{8.5W}{8V \times 0.51} + \frac{2.04A}{2} = 3.10A \tag{8}$$

IL_{PEAK} is used to properly size the current sense resistor. Table 3-1 summarizes the key parameters of selected transformer.

Table 3-1. Selected Transformer Parameters

Parameter	Value
Turns Ratio (N_P:N_{S1}:N_{S2}:N_{S3}:N_{S4})	1:1.2:2.4:2.4:2.4 (5:6:12:12:12)
Primary winding inductance (L_M)	8 µH
Primary winding saturation current (I_{SAT})	5.5 A

3.3 Slope Compensation Check

According to the theory of the peak current mode control, the slope of the compensation ramp must be greater than half of the sensed inductor current falling slope to prevent subharmonic oscillation at high duty cycle. Therefore, the following inequality in Equation 9 should be satisfied.

$$0.5 \times \frac{(V_{LOAD} + V_F) - V_{SUPPLY}}{L_M} \times A_{CS} \times \text{Margin} < 500\text{mV} \times f_{sw} \quad (9)$$

where

- A_{CS} is the equivalent current sensing gain.
- 500mV is the slope compensation peak voltage.

Typically 82% of the sensed inductor current falling slope is an optimal value of the slope compensation, which reflects to a margin of 1.6. If the inequality is failed, the inductance value of L_M must be increased so that the falling slope can be smaller. If the L_M inductance value is changed the peak current must be re-calculated and the device selection must be re-examined. In this example, the inequality is verified in Equation 10, Equation 11, and Equation 12.

$$0.5 \times \frac{(V_{LOAD} + V_F) - V_{SUPPLY}}{L_M} \times A_{CS} \times \text{Margin} = 0.5 \times \frac{(10V + 0.5V) - 8V}{8\mu\text{H}} \times 0.095 \times 1.6 = 23.75 \times 10^3 \quad (10)$$

$$500\text{mV} \times f_{sw} = 500\text{mV} \times 250k\text{Hz} = 125 \times 10^3 \quad (11)$$

$$23.75 \times 10^3 < 125 \times 10^3 \quad (12)$$

3.4 Diode Selection

The diode on the secondary side must have a reverse voltage rating greater than the reflected voltage for the primary transformer winding to the secondary winding plus the secondary load voltage. The reverse voltage of the secondary diode is calculated in Equation 13.

$$V_{D\_reverse} = \left(\frac{N_S}{N_P} \cdot V_{SUPPLY\_max}\right) + V_{LOAD} = \left(\frac{0.5}{1} \cdot 36V\right) + 5V = 23V \quad (13)$$

Due to leakage inductance, there is a negative spike when the primary side switch is being turned off. A snubber needs to be added across the diode to help minimize this voltage spike. Even if a snubber is added, some voltage margin must be added to the value calculated in Equation 13. For this application, a diode with a reverse voltage rating of 40 V is selected.

The average current of the secondary side diode is estimated using Equation 14.

$$I_{D\_AVG} = I_{LOAD} = 5A \quad (14)$$

The diode must be able to conduct the value calculated in Equation 14 with some margin. For the design, the selected diode is capable of conducting 10 A of average forward current.

3.5 Output Capacitor Selection

The output capacitor is required to smooth the load voltage ripple and provides an energy source during load transients and provides energy to the load during the on-time of the MOSFET. A practical way to size the output capacitor is based on the required load transient specification. The load transient specification is related to the control loop crossover frequency. For this estimate it is expected that the control loop cross over frequency is set to 1/5th the RHPZ frequency, which is calculated using Equation 15.

$$f_{CROSS} = \frac{f_{Z\_RHP}}{5} = \frac{N_P^2}{N_S^2} \cdot \frac{\frac{V_{LOAD}^2}{P_{OUT\_total}} \cdot (D')^2}{5 \cdot 2 \cdot \pi \cdot L_M} = \frac{1^2}{0.5^2} \cdot \frac{\frac{5^2}{20.2W} \cdot (1 - 0.357)^2}{5 \cdot 2 \cdot \pi \cdot 21\mu H} = 8.68kHz \quad (15)$$

For this design example, the load transient specification indicates that the load voltage should not overshoot or undershoot more than 100 mV during a load transient from 50% load current (2 A) to 100% load current (4 A) occurs. Equation 16 is used to calculate the estimated load capacitance to achieve the specified load transient load voltage ripple requirements.

$$C_{LOAD\_min} = \frac{\Delta I_{LOAD}}{2\pi \cdot f_{CROSS} \cdot \Delta V_{LOAD}} = \frac{2A}{2\pi \cdot 8.6kHz \cdot 100mV} = 366\mu F \quad (16)$$

where

- ΔI_{LOAD} is the difference in the load current conditions (4 A - 2 A)
- ΔV_{LOAD} is the specified overshoot voltage specification and undershoot voltage specification

In this design C_{LOAD} is selected to be 540 µF.

3.6 Input Capacitor Selection

The input capacitors smooth the supply ripple voltage during operation. For this design, the input voltage ripple is designed to be less than 50 mV when the supply voltage is at the minimum value. Equation 17 is used to estimate the required input capacitor based on the supply ripple voltage specification.

$$C_{IN\_min} = \frac{\frac{P_{OUT\_total}}{V_{SUPPLY\_min}} \times \left(1 - D\right)}{\Delta V_{SUPPLY} \times f_{SW}} = \frac{\frac{8.5W}{8V} \times \left(1 - 0.51\right)}{250mV \times 250kHz} = 8.33\mu F \quad (17)$$

The input capacitor is selected to be 100 µF. Ceramic capacitors are added to help lower the ESR of the input capacitor bank.

3.7 UVLO Resistor Selection

The external under voltage lockout (UVLO) resistors set the minimum operating supply voltage of the regulator. Two levels must be specified; the voltage the LM5157/58 starts operation ($V_{SUPPLY(ON)}$) and the voltage the LM5157/58 enters stand-by mode ($V_{SUPPLY(OFF)}$). In this example, $V_{SUPPLY(ON)}$ voltage is 7.5 V and the $V_{SUPPLY(OFF)}$ is 7 V. Using Equation 18, the top UVLO resistor (R_{UVLOT}) is calculated.

$$R_{UVLOT} = \frac{0.967 \times V_{SUPPLY(ON)} - V_{SUPPLY(OFF)}}{5\mu A} = \frac{0.967 \times 7.5V - 7V}{5\mu A} = 50.5k\Omega \quad (18)$$

R_{UVLOT} is selected to be 49.9 kΩ. R_{UVLOB} is calculated using Equation 19.

$$R_{UVLOB} = \frac{1.5V \times R_{UVLOT}}{V_{SUPPLY(ON)} - 1.5V} = \frac{1.5V \times 49.9k\Omega}{7.5V - 1.5V} = 12.48k\Omega \quad (19)$$

R_{UVLOB} is selected to be 12.4 kΩ.

3.8 Control Loop Compensation

One benefit of the peak current mode control is the easier compensation design compared with that of the voltage mode control. A simple two-pole (one at origin), single zero network is adequate. A type II compensation network is implemented as shown in Figure 3-1, which provides a programmable zero and a pole. The following section introduces a general technique to set the crossover frequency and place the pole and zero of the error amplifier to achieve a stable system in the CCM for a primary side regulated Flyback. The detailed models of the control loop are presented in Section 5. An example for the compensation of an isolated Flyback can be found in How to Design an Isolated Flyback using LM5155 application note.

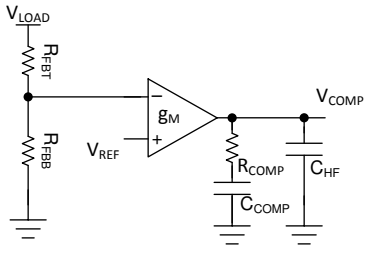

Figure 3-1. Type II Compensation Network

3.8.1 Crossover Frequency (f_{cross}) Selection

The crossover frequency of the loop can be either selected to be 1/10 the switching frequency or 1/5 the right-half plane zero frequency, which ever is lower. Equation 20 shows the calculation for 1/10 the switching frequency. Equation 21 and Equation 22 show how to calculate the 1/5 the right half plane zero frequency at full load and half load conditions.

$$f_{\text{cross}} = \frac{f_{\text{sw}}}{10} = \frac{250\text{kHz}}{10} = 25\text{kHz} \tag{20}$$

$$f_{CROSS\_1} = \frac{f_{Z\_RHP}}{5} = \frac{1}{5} \times \frac{\frac{{N_p}^2}{{N_{s1}}^2} \times \frac{{V_{LOAD1}}^2}{P_{OUT\_total}}(D')^2}{2 \times \pi \times L_M \times D} = \frac{1}{5} \times \frac{\frac{1^2}{1.2^2} \times \frac{10V^2}{8.5W}(1-0.51)^2}{2 \times \pi \times 8\mu H \times 0.51} = 15.3kHz \tag{21}$$

$$f_{CROSS\_2} = \frac{f_{Z\_RHP}}{5} = \frac{1}{5} \times \frac{\frac{{N_p}^2}{{N_{s1}}^2} \times \frac{{V_{LOAD1}}^2}{P_{OUT\_total}}(D')^2}{2 \times \pi \times L_M \times D} = \frac{1}{5} \times \frac{\frac{1^2}{1.2^2} \times \frac{10V^2}{4.25W}(1-0.51)^2}{2 \times \pi \times 8\mu H \times 0.51} = 7.65kHz \tag{22}$$

where

- D' is (1 -D) a the minimum supply voltage
- P_{OUT_total} is the summed up total output power of all outputs

To give some margin, the crossover frequency is selected to be 9 kHz, a little less than 1/5 the right half plane zero frequency at half load condition. In this design example, the performance under the full load condition is more important and needs to be optimized. Therefore, the full load condition with the input voltage from 8 V to 16 V is used for the calculations below. After the design and selection of the compensation loop, the stability of the half load condition can be checked with the equations in Section 5.

3.8.2 R_{COMP} Selection

The R_{COMP} value directly affects the crossover frequency of the control loop. The higher the crossover frequency, the faster the control loop reacts to transient conditions. Knowing the desired loop crossover frequency, 5 kHz, R_{COMP} is calculated using Equation 23.

$$R_{COMP} = \frac{2 \times \pi \times A_{Cs} \times C_{OUT\_total} \times \frac{N_{S1}}{N_p} \times V_{LOAD1} \times f_{CROSS}}{G_{COMP} \times g_m \times \left(1 - D_{VIN\_min}\right)}$$
$$R_{COMP} = \frac{2 \times \pi \times 0.095 \times 300\mu F \times \frac{1.2}{1} \times 10V \times 5kHz}{G_{COMP} \times g_m \times (1-0.51)} = 10.96k\Omega \tag{23}$$

where

- g_m is the transconductance of the error amplifier, 2 mA/V (see data sheet)
- A_{CS} is gain of the internal sensed current, 0.095 (see data sheet)
- G_{COMP} is COMP to PWM gain, 1 V/V

R_{COMP} is selected to be 10 kΩ. Decreasing the R_{COMP} resistance value lowers the crossover frequency but helps ensure the control loop remains stable over the specified supply voltage range.

3.8.3 C_{COMP} Selection

The R_{COMP} resistor and C_{COMP} capacitor set a low frequency zero of the compensation network, providing a phase boost. Placement of this zero frequency largely impacts the transient response of the control loop. A good strategy to help ensure adequate phase margin is to place the zero at geometric mean of the crossover frequency (f_{CROSS}) and the low frequency pole of the modulator. Equation 24 places the low frequency zero of error amplifier a the geometric mean of f_{CROSS} and low frequency pole of the plant (ω_{P_LF}). Equation 24 is used to calculate the value of C_{COMP}.

$$C_{COMP} = \sqrt{\frac{{C_{LOAD\_total} \times V_{LOAD1}}^2}{2 \times \pi \times {R_{COMP}}^2 \times f_{CROSS} \times P_{OUT\_total} \times \left(1 + D\right)}} \quad (24)$$

$$C_{COMP} = \sqrt{\frac{300\mu F \times {10V}^2}{2 \times \pi \times {10k\Omega}^2 \times 5kHz \times 8.5W \times \left(1 + 0.51\right)}} = 27.2nF$$

C_{COMP} is selected to be 22 nF.

3.8.4 C_{HF} Selection

The C_{HF} capacitor sets the high frequency pole of the compensation network. The high frequency pole aids in attenuating high frequency noise due to the switching frequency and assuring enough gain margin achieved. It is recommended to set the pole frequency between or between the RHP zero (ω_{Z_RHP}), which is usually smaller than the ESR zero, or between the RHP zero and half the switching frequency. In this design example, the high frequency pole is placed at the RHP zero. Equation 25 is used to calculate the value of C_{HF}.

$$C_{HF} = \frac{D_{VIN\_min} \times L_M \times \frac{{N_{S1}}^2}{{N_P}^2} \times \frac{{P_{OUT\_total}}^2}{{V_{LOAD1}}^2}}{R_{COMP} \times \left(1 - D_{VIN\_min}\right)^2} = \frac{0.51 \times 8\mu H \times \frac{{1.2}^2}{1^2} \times \frac{{8.5W}^2}{{10V}^2}}{10k\Omega \times \left(1 - 0.51\right)^2} = 208pF \quad (25)$$

For the EVM the C_{HF} is chosen to be 1 nF.

4 Component Selection Summary

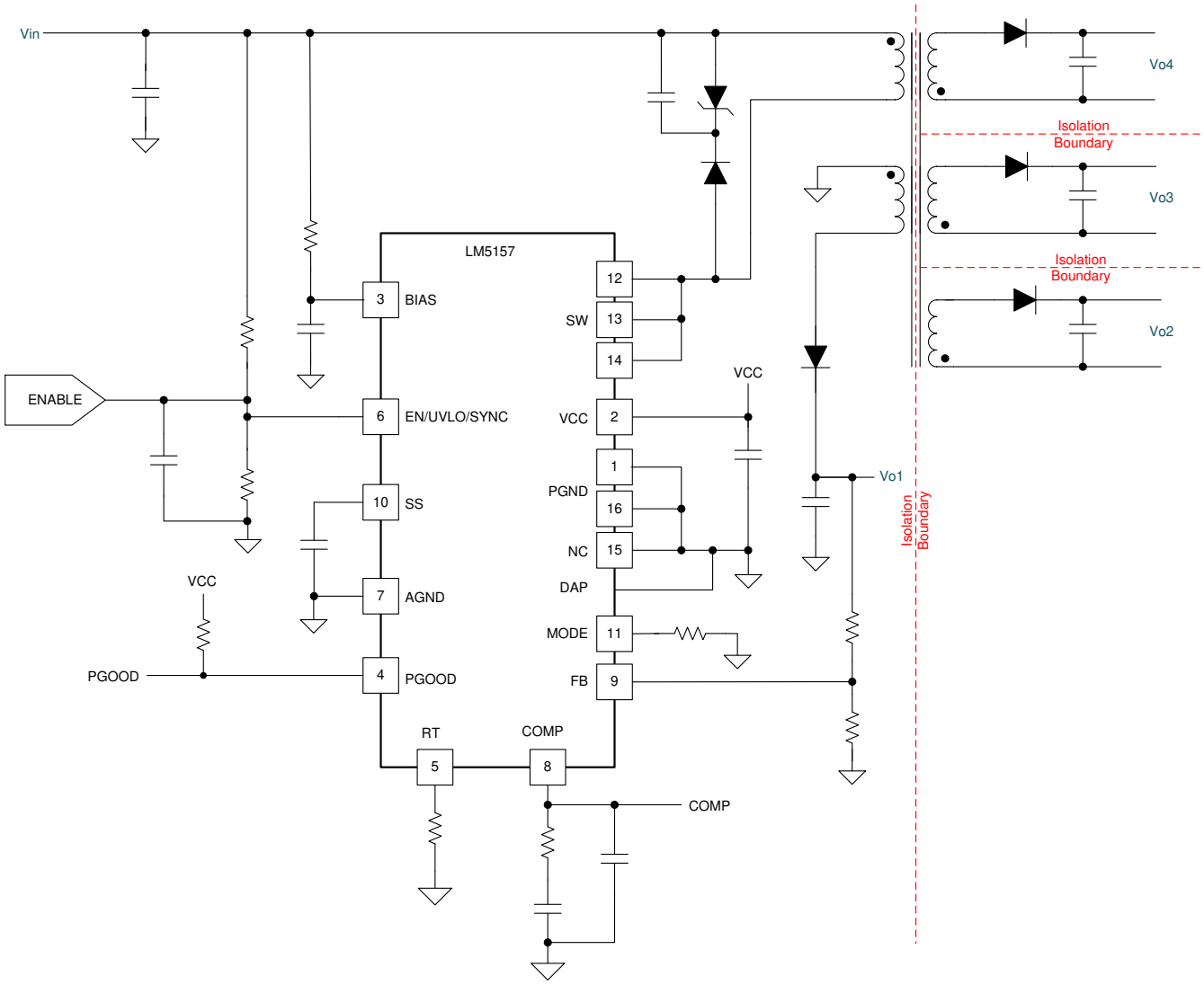

Figure 4-1. Application Circuit

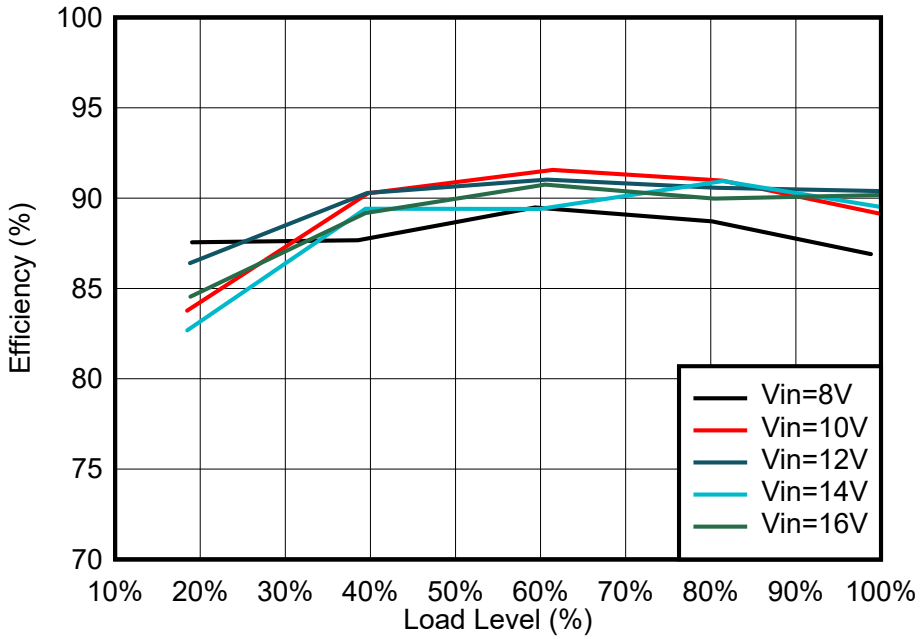

Figure 4-2. Efficiency vs. I_{LOAD}

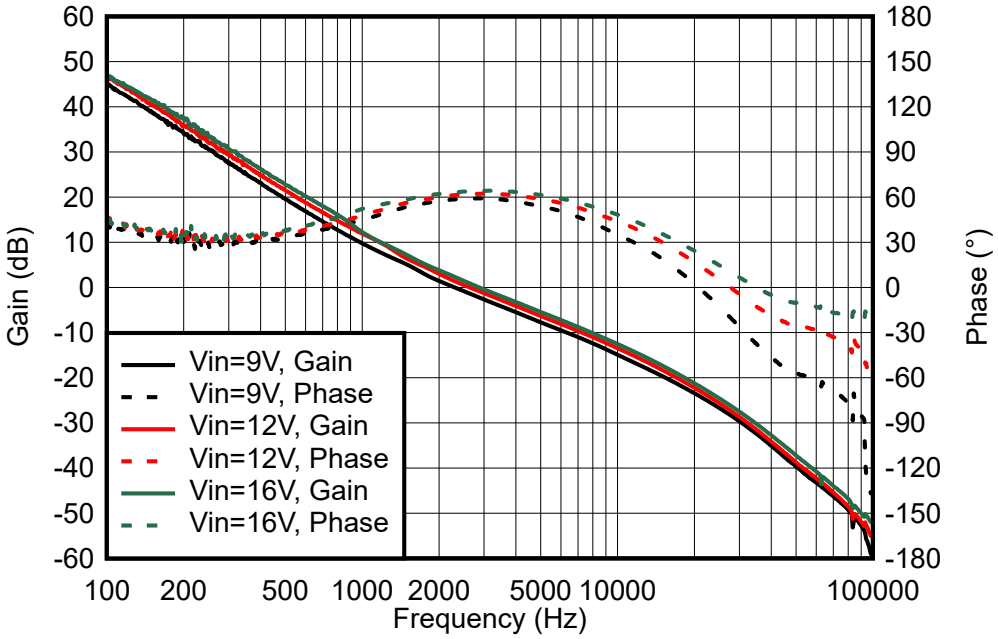

Figure 4-3. Control Loop Response (Vo1-4: 100% Load)

4.1 Application Circuit

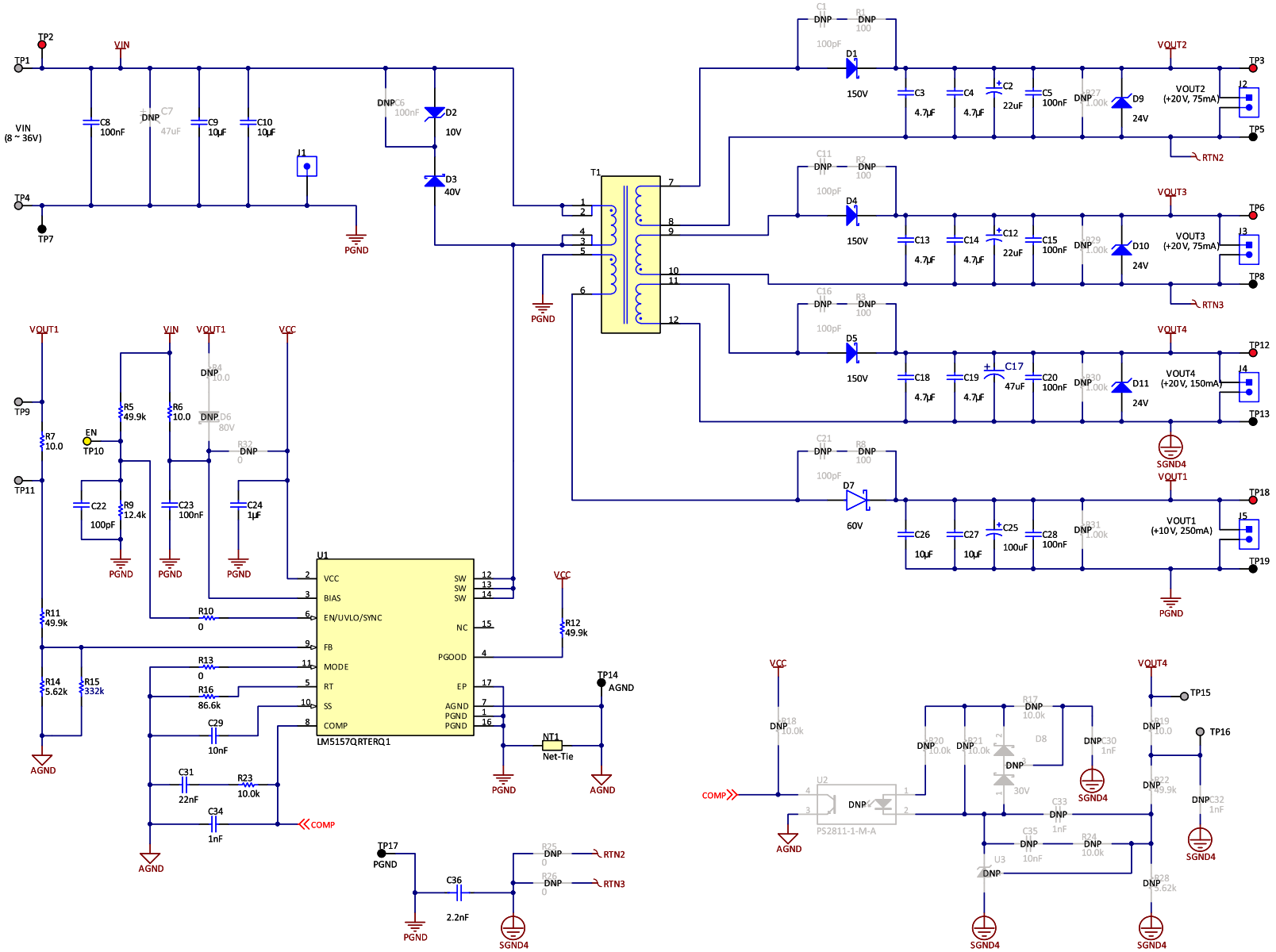

Figure 4-4. LM5157EVM-FLY Schematic

4.2 Bill of Materials

Table 4-1. LM5157EVM-FLY Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
C2, C12	2	22uF	CAP, Polymer Hybrid, 22 uF, 50 V, ± ±20%, 0.08 ohm, AEC-Q200 Grade 1, D6.3xL5.8mm SMD	D6.3xL5.8mm	EEH-ZC1H220P	Panasonic
C3, C4, C13, C14, C18, C19	6	4.7uF	CAP, CERM, 4.7 µF, 50 V,±10%, X7R, AEC-Q200 Grade 1, 1210	1210	C1210C475K5RACAUTO	Kemet
C5, C8, C15, C20, C23, C28	6	0.1uF	CAP, CERM, 0.1 µF, 50 V,±10%, X7R, AEC-Q200 Grade 1, 0603	0603	C0603C104K5RACAUTO	Kemet
C7, C17	2	47µF	47µF 50V Aluminum - Polymer Capacitors Radial, Can - SMD 30mOhm 4000 Hrs @ 125°C	SMD2	EEH-ZC1H470P	Panasonic
C9, C10	2	10uF	CAP, CERM, 10 µF, 50 V,±10%, X7R, AEC-Q200 Grade 1, 1206	1206	CGA5L1X7R1H106K160AE	TDK
C22	1	100pF	CAP, CERM, 100 pF, 50 V, ±5%, C0G/NP0, AEC-Q200 Grade 0, 0603	0603	CGA3E2NP01H101J080AA	TDK
C24	1	1uF	CAP, CERM, 1 uF, 25 V, ±10%, X7R, 0603	0603	06033C105KAT2A	AVX
C25	1	100uF	CAP, Aluminum Polymer, 100 uF, 16 V, ±20%, 0.035 ohm, 10x10.3 SMD	10x10.3	16SVP100M	Panasonic
C26, C27	2	10uF	CAP, CERM, 10 µF, 16 V,±10%, X7R, AEC-Q200 Grade 1, 1206	1206	C1206C106K4RACAUTO	Kemet
C29	1	0.01uF	CAP, CERM, 0.01 uF, 16 V, ±10%, X7R, 0603	0603	C0603C103K4RACTU	Kemet
C31	1	0.022uF	CAP, CERM, 0.022 uF, 25 V, ±10%, X7R, 0603	0603	C0603C223K3RACTU	Kemet
C34	1	1000pF	CAP, CERM, 1000 pF, 50 V, ±5%, X7R, 0603	0603	C0603C102J5RACTU	Kemet
C36	1	2.2nF	2200pF ±10% 2000V (2kV) Ceramic Capacitor X7R (2R1) 1206 (3216 Metric)	1206	1206Y2K00222KET	Knowles Syfer
D1, D4, D5	3	150V	Diode, Schottky, 150 V, 1 A, PowerDI123	PowerDI123	DFLS1150-7	Diodes Inc.
D2	1	10V	Diode, Zener, 10 V, 1.5 W, SMA	SMA	1SMA5925BT3G	ON Semiconductor
D3	1	40V	Diode, Schottky, 40 V, 1 A, AEC-Q101, SMA	SMA	B140Q-13-F	Diodes Inc.
D7	1		DIODE SCHOTTKY 60V 1A POWERDI123	PowerDI123	DFLS160-7	Diodes
D9, D10, D11	3	24V	Diode, Zener, 24 V, 500 mW, SOD-123	SOD-123	DDZ24C-7	Diodes Inc.
R5, R11, R12	3	49.9k	RES, 49.9 k, 1%, 0.1 W, 0603	0603	RC0603FR-0749K9L	Yageo
R6, R7	2	10.0	RES, 10.0, 1%, 0.1 W, 0603	0603	RC0603FR-0710RL	Yageo
R9	1	12.4k	RES, 12.4 k, 1%, 0.1 W, 0603	0603	RC0603FR-0712K4L	Yageo
R10, R13	2	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3GEY0R00V	Panasonic
R14	1	5.62k	RES, 5.62 k, 1%, 0.1 W, 0603	0603	RC0603FR-075K62L	Yageo
R15	1	332k	RES, 332 k, 0.1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	RC0603FR-07332KL	Yageo
R16	1	86.6k	RES, 86.6 k, 1%, 0.1 W, 0603	0603	RC0603FR-0786K6L	Yageo
R23	1	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo
T1	1		FLYBACK TRANSFORMER	SMT_TRANSFORMER_17MM20_21MM97	ZB1324-AL	Coilcraft

Table 4-1. LM5157EVM-FLY Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
U1	1		2.2MHz Wide VIN Boost/Sepic/Flyback Converter with Dual Random Spread Spectrum, RTE0016K (WQFN-16)	RTE0016K	LM5157QRTERQ1	Texas Instruments
C1, C11, C16, C21	0	100pF	CAP, CERM, 100 pF, 100 V, ±1%, C0G/NP0, 0603	0603	C1608C0G2A101F080AA	TDK
C6	0	0.1uF	CAP, CERM, 0.1 µF, 50 V,±10%, X7R, AEC-Q200 Grade 1, 0603	0603	C0603C104K5RACAUTO	Kemet
C30, C32, C33	0	1000pF	CAP, CERM, 1000 pF, 50 V, ±5%, X7R, 0603	0603	C0603C102J5RACTU	Kemet
C35	0	0.01uF	CAP, CERM, 0.01 uF, 16 V, ±10%, X7R, 0603	0603	C0603C103K4RACTU	Kemet
D6	0	80V	Diode, Schottky, 80 V, 0.5 A, SOD-123	SOD-123	MBR0580-TP	Micro Commercial Components
D8	0	30V	Diode, Schottky, 30 V, 0.2 A, SOT-323	SOT-323	BAT54SWT1G	Fairchild Semiconductor
R1, R2, R3, R8	0	100	RES, 100, 1%, 0.1 W, 0603	0603	RC0603FR-07100RL	Yageo
R4, R19	0	10.0	RES, 10.0, 1%, 0.1 W, 0603	0603	RC0603FR-0710RL	Yageo
R17, R18, R20, R21, R24	0	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo
R22	0	49.9k	RES, 49.9 k, 1%, 0.1 W, 0603	0603	RC0603FR-0749K9L	Yageo
R25, R26	0	0	RES, 0, 5%, 0.25 W, AEC-Q200 Grade 0, 1206	1206	ERJ-8GEY0R00V	Panasonic
R27, R29, R30, R31	0	1.00k	RES, 1.00 k, 1%, 0.25 W, AEC-Q200 Grade 0, 1206	1206	ERJ-8ENF1001V	Panasonic
R28	0	5.62k	RES, 5.62 k, 1%, 0.1 W, 0603	0603	RC0603FR-075K62L	Yageo
R32	0	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3GEY0R00V	Panasonic
U2	0		Optocoupler, 2.5 kV, 100-200% CTR, SMT	PS2811-1	PS2811-1-M-A	California Eastern Laboratories
U3	0		Low-Voltage (1.24V) Adjustable Precision Shunt Regulators, 3-pin SOT-23, Pb-Free	DBZ0003A		Texas Instruments

5 Small Signal Frequency Analysis

This section provides detailed equations used to model the control loop when the LM5157/58 is configured as an isolated flyback regulator. These equations are only valid when the regulator is operating in continuous conduction mode. The simplified formulas allow for quick evaluation of the control loop, but loose accuracy at high frequencies. The comprehensive formulas are more complex but provide better accuracy at high frequencies.

5.1 Flyback Regulator Modulator Modeling

These equations model the plant of a peak current mode flyback regulator in continuous conduction mode.

Table 5-1. Control Loop Equations

	Simplified Formula	Comprehensive Formula
Modulator Equations		
Modulator Transfer Function	$\frac{\widehat{V}_{LOAD}(s)}{\widehat{V}_{COMP}(s)} = A_M \frac{\left(1+\frac{s}{\omega_{Z\_ESR}}\right)\left(1-\frac{s}{\omega_{Z\_RHP}}\right)}{\left(1+\frac{s}{\omega_{P\_LF}}\right)}$ (26)	$\frac{\widehat{V}_{LOAD}(s)}{\widehat{V}_{COMP}(s)} = A_M \frac{\left(1+\frac{s}{\omega_{Z\_ESR}}\right)\left(1-\frac{s}{\omega_{Z\_RHP}}\right)}{\left(1+\frac{s}{\omega_{P\_LF}}\right)\left(1+\frac{s}{Q\times\omega_n}+\frac{s^2}{{\omega_n}^2}\right)}$ (27)
Modulator DC Gain	$A_M = G_{COMP} \times \frac{N_P}{N_S} \frac{{V_{LOAD}}^2}{P_{OUT}} \frac{(1-D)}{(1+D)\times A_{CS}\times R_S}$ (28)	
RHP Zero	$\omega_{Z\_RHP} = \frac{\frac{{N_P}^2}{{N_S}^2}\times\frac{{V_{LOAD}}^2}{P_{OUT}}\times(1-D)^2}{L_M\times D}$ (29)	
ESR Zero	$\omega_{Z\_ESR} = \frac{1}{C_{LOAD}\times R_{ESR}}$ (30)	
Low Frequency Pole	$\omega_{P\_LF} = \frac{1+D}{C_{LOAD}\times\frac{{V_{LOAD}}^2}{P_{OUT}}}$ (31)	
Sub-Harmonic Double Pole	Not Considered	$\omega_n = \pi \times f_{SW}$ (32)
Quality Factor	Not Considered	$Q = \frac{1}{\pi\left[D'\times\left(1+\frac{s_e}{s_n}\right)-\frac{1}{2}\right]}$ (33)
Slope Compensation	Not Considered	$s_e = (V_{SLOPE} + I_{SLOPE}\times R_{SL})\times f_{SW}$ (34)
Sensed Rising Inductor Slope	Not Considered	$s_n = \frac{V_{SUPPLY}\times(1-D)\times R_S\times A_{CS}}{L_M}$ (35)

1. G_{COMP} is COMP to PWM gain, 0.142V/V

5.2 Compensation Modeling

These equations model a type II compensation network implemented using a transconductance error amplifier.

Table 5-2. Compensation Modeling Equations

	Simplified Formula	Comprehensive Formula
Feedback Equations		
Feedback Transfer Function	$\frac{\widehat{V}_{COMP}(s)}{\widehat{V}_{LOAD}(s)} = -A_{FB}\frac{\left(1+\frac{s}{\omega_{Z\_EA}}\right)}{s\times\left(1+\frac{s}{\omega_{P\_EA}}\right)}$ (36)	
Feedback DC Gain	$A_{FB} = \frac{R_{FBB}\times g_m}{(R_{FBB}+R_{FBT})\times C_{COMP}}$ (37)	$A_{FB} = \frac{R_{FBB}\times g_m}{(R_{FBB}+R_{FBT})\times (C_{COMP}+C_{HF})}$ (38)
Low Frequency Zero	$\omega_{Z\_EA} = \frac{1}{R_{COMP}\times C_{COMP}}$ (39)	$\omega_{Z\_EA} = \frac{1}{R_{COMP}\times C_{COMP}}$ (40)
High Frequency Pole	$\omega_{P\_EA} = \frac{1}{R_{COMP}\times C_{HF}}$ (41)	$\omega_{P\_EA} = \frac{C_{COMP}+C_{HF}}{R_{COMP}\times C_{COMP}\times C_{HF}}$ (42)
Mid-band Gain	$G_{MID} = \frac{R_{COMP}\times R_{RFBB}\times g_m}{(R_{FBB}+R_{FBT})}$ (43)	$G_{MID} = \frac{C_{COMP}\times R_{COMP}\times R_{RFBB}\times g_m}{(C_{COMP}+C_{HF})\times (R_{FBB}+R_{FBT})}$ (44)

1. g_m is the transconductance of the error amplifier, 2mA/V

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