Application Report
SNVA856A–February 2019–Revised May 2020

# Working With Inverting Buck-Boost Converters

*Frank De Stasi*

**ABSTRACT**

Generating a negative output voltage rail from a positive input voltage rail can be done by reconfiguring an ordinary buck regulator. The result is an inverting buck-boost (IBB) topology implementation. This application report gives details regarding this conversion with examples.

**Contents**



**List of Figures**

## Trademarks

All trademarks are the property of their respective owners.

## 1 Introduction

Many systems require a negative power supply rail, when all that is available is a positive supply with respect to ground. Examples of such systems include both medical ultrasound scanners and test and measurement equipment. A unique DC/DC converter called an inverting buck-boost (IBB) can be used to provide this negative rail from a positive supply, all with a common ground connection. Almost any ordinary buck regulator can be converted into an IBB with a few simple changes in line and load connections. This application report details the conversion from a buck to an IBB, the operation of the converter and things that you need to consider to make your power supply application a success.

## 2 Inverting Buck-Boost Converter

The diagrams in Figure 1 show a comparison between an ordinary buck DC/DC converter and the IBB. The buck converter takes a positive input voltage and converts it to a positive output voltage of smaller magnitude. The IBB takes a positive input voltage and coverts it to a negative output voltage, with a common ground connection between input and output. It is easy to see the similarity between the two converters. The top schematic in Figure 2 shows the connections for taking the buck regulator and converting it into an IBB. Looking at the connections shown in red, we see that the buck output is now the system ground and the buck "ground" becomes the negative output. An additional input capacitor is added between the input supply and system ground. The lower schematic shows the connections when using a synchronous buck regulator IC. A non-synchronous converter can also be used. Notice that the "ground" reference for the IC is now the negative output voltage. This has consequences for the maximum input voltage and the control inputs when using this configuration. Also, notice that the feed-back connection to the regulator is not changed from that of an ordinary buck. Although the examples show a synchronous buck with an internal feedback divider, a non-synchronous IC, and/or external feedback dividers can also be used.

The connection changes are detailed in the following list:

1. Reassign buck positive output as system ground.
2. Reassign buck regulator ground nodes as the negative output voltage node.
3. Positive input stays the same.

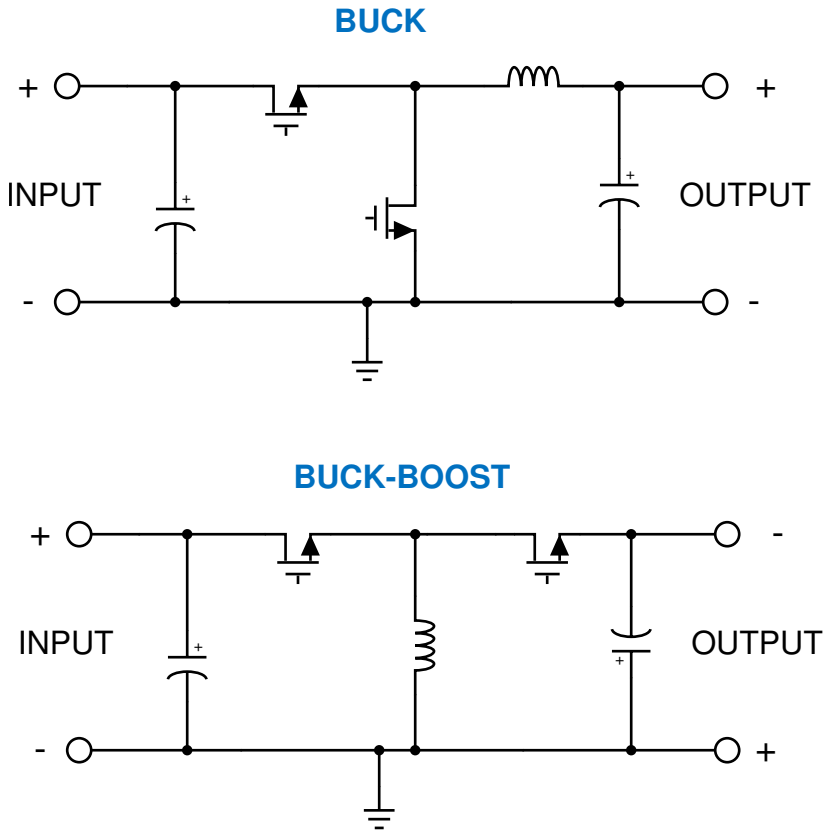


**Figure 1. Comparison of Buck and Inverting Buck-Boost Topology**

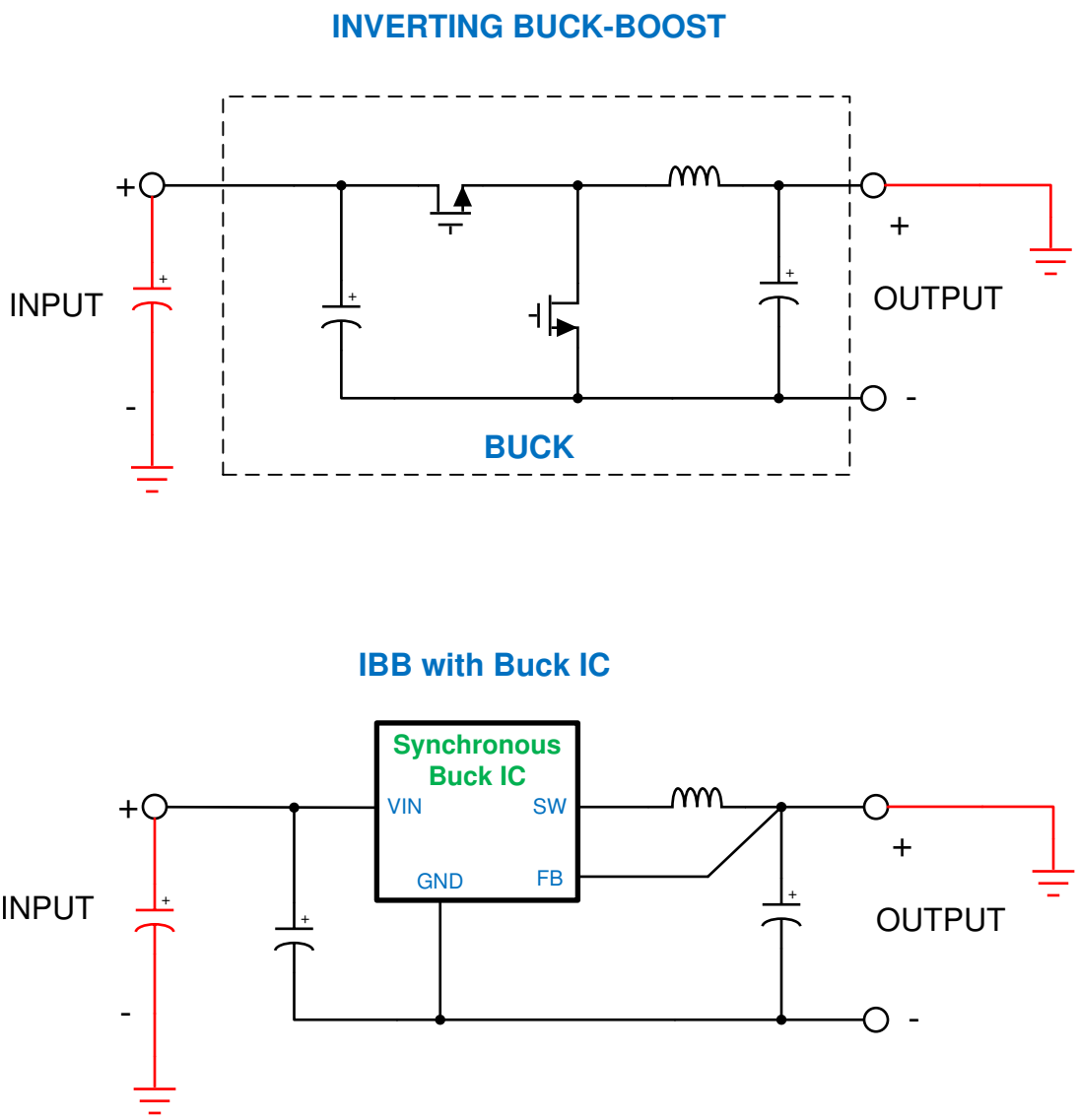


**Figure 2. Converting a Buck to an Inverting Buck-Boost**

## 3 Basic Operation

The basic operation of the converter is shown in Figure 3. During the portion of the switching cycle in which the HS FET is on, the inductor voltage is equal to $V_{IN}$. For the remainder of the switching cycle, the LS FET turns on and the inductor voltage is $-V_{OUT}$. At this point the inductor energy is supplied to the load and the output capacitor. The controller regulates the output voltage by adjusting the duty cycle of the HS and LS FET switches. Performing a standard analysis on the circuit in Figure 3, we arrive at the conversion law found in Equation 1.

$$\frac{|V_{OUT}|}{V_{IN}} = \frac{D}{1-D} \cdot \eta \quad (1)$$

where

- $\eta$ = Efficiency

A plot of this equation is shown in Figure 4 for a typical duty cycle range of 0.1 to 0.9. The first thing to notice is that the conversion ratio can be less than or greater than one. This means that the IBB can either increase or decrease the input voltage, depending on the duty cycle D; hence the name "buck-boost". For example you can regulate to an output voltage of –5 V from an input voltage of from 5 V and 24 V or convert an input range of 12 V to 24 V to an output of –15 V. The controller smoothly moves from "buck" mode to "boost" mode as the input voltage changes, while regulating the output voltage. Rearranging Equation 1, we arrive at the duty cycle as a function of our input and output voltages; as found in Equation 2.

$$D = \frac{|V_{OUT}|}{|V_{OUT}| + \eta \cdot V_{IN}} \tag{2}$$

In the IBB topology, both the input and output currents are "chopped". In other words these currents are discontinuous and have very fast transition times. This means that the IBB may generate more voltage spikes in the output voltage than a buck. These issues can be addressed with properly sized output capacitors or post regulation filters.

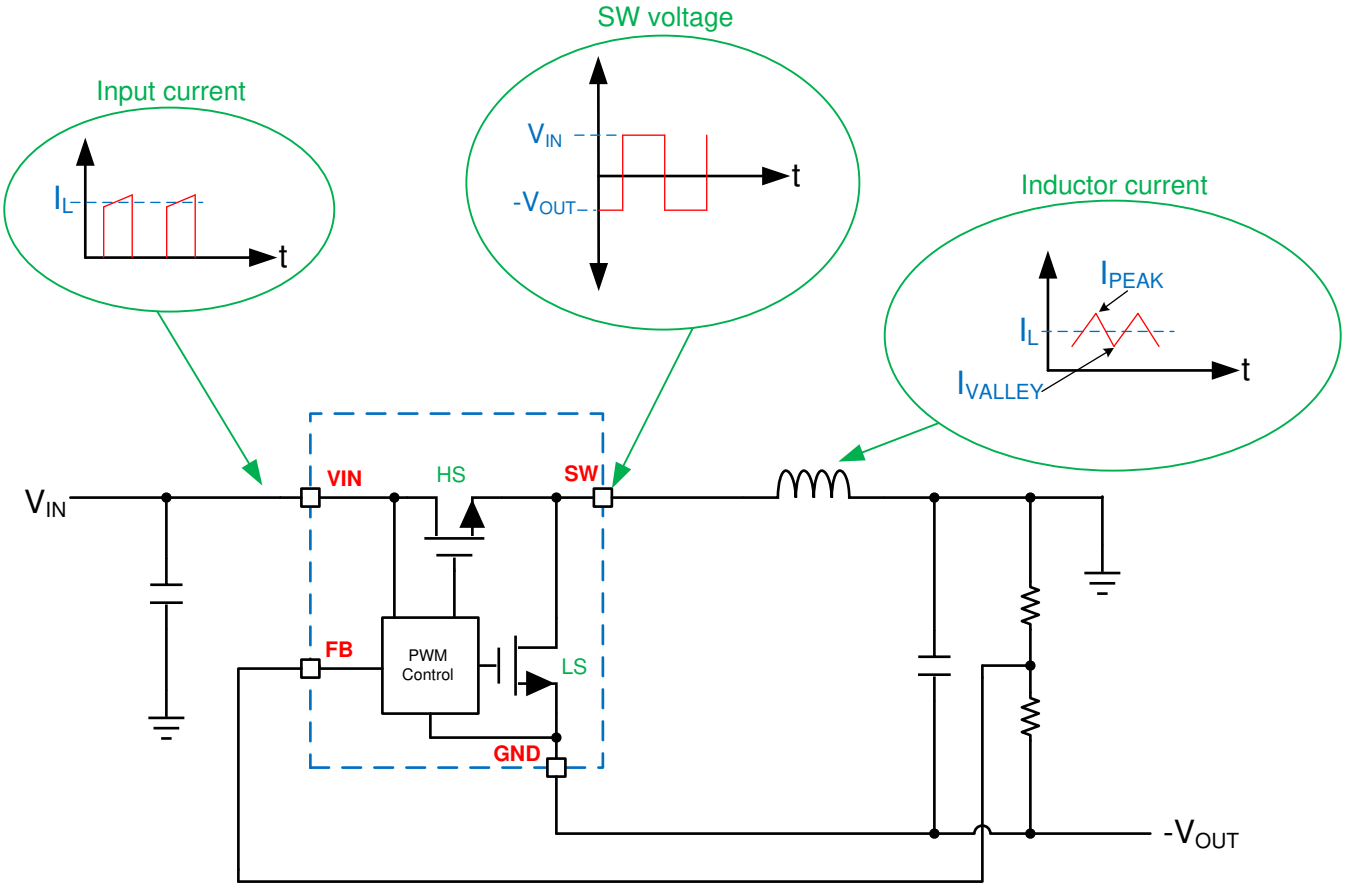


**Figure 3. Inverting Buck-Boost Waveforms**

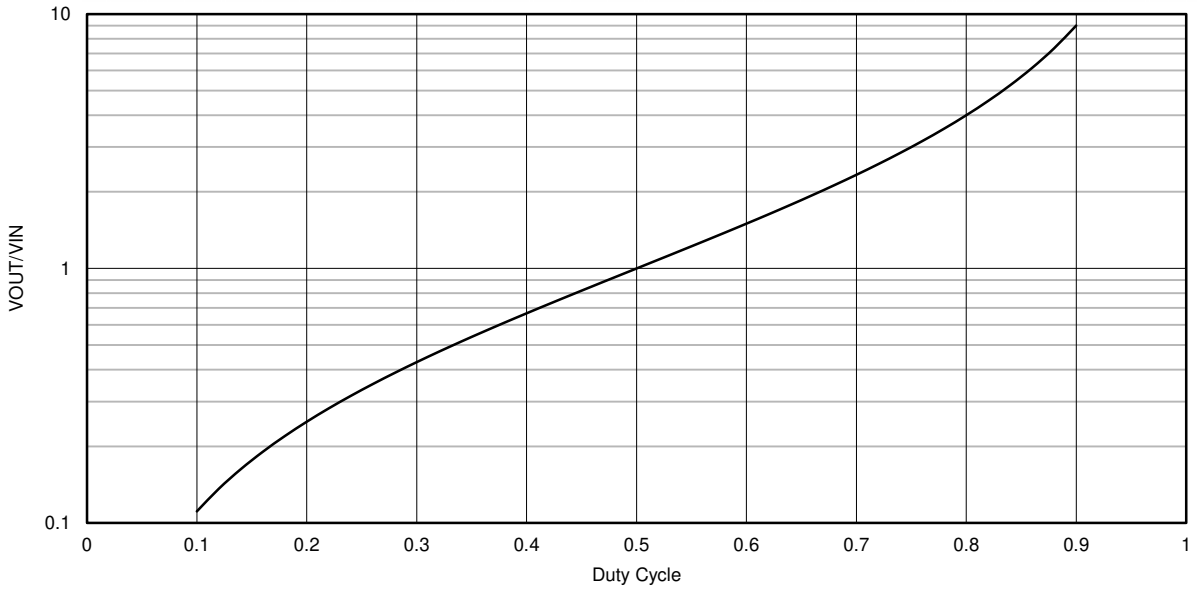


**Figure 4. Conversion Ratio vs Duty Cycle**

# 4 Operating Considerations of a Buck Based Inverting Buck-Boost

## 4.1 Voltage Stress

Selecting a buck regulator to convert to an IBB requires special attention to the voltage and current requirements of the application. A quick glance at Figure 5 shows that the voltage across the VIN and GND pins of the regulator IC is equal to the input voltage plus the negative output voltage. This voltage is greater than for a buck regulator, which only sees the input voltage across the VIN and GND terminals. As an example, if you needed to convert from an input of +24 V to an output of –15 V, you would need a regulator with a voltage rating of at least 39 V. This would exclude many of the available "36-V" devices, requiring the use of a device rated at 40 V or more. The data sheet specification that applies here is the "*Input Voltage Absolute Maximum*" ratings. The same applies to the voltage rating of the "catch" diode in a non-synchronous solution.

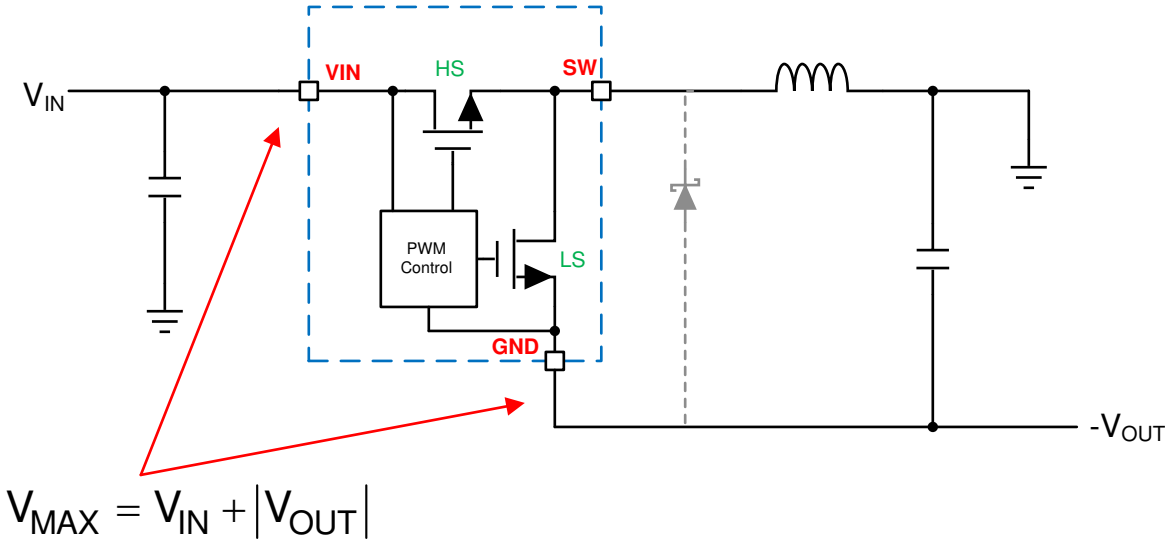


**Figure 5. Voltage Stress on an IBB**

### 4.2 Current Stress

The inductor currents and peak switch currents in the IBB are larger than in the equivalent buck converter from which it is made. First, the average input supply current can be calculated as for any converter, using Equation 3.

$$I_{IN} = I_{OUT} \cdot \frac{|V_{OUT}|}{V_{IN} \cdot \eta} \tag{3}$$

Notice that when the magnitude of the output voltage is less than the input voltage (buck mode), the input current is less than the output current. This is the same as for an ordinary buck. However, when the output voltage is greater than the input voltage (boost mode), the input current is greater than the output current. This is the same as for an ordinary boost converter. Another thing to note is that the efficiency of the IBB is somewhat less than an equivalent buck or boost; this is discussed further on. The average inductor current is the sum of the input and output currents, and is given by Equation 4. The peak and valley of the inductor current are given in Equation 5. The first term in Equation 5 is the average inductor current, while the second terms represent the inductor ripple current. Since the peak and valley of the inductor current pass through the MOSFET power switches, they determine how much output current a given IBB can supply, when built from a buck. Most buck regulators are rated for a certain maximum load current. This is convenient since the load current and average inductor current are the same for a buck. However, as seen from Equation 4 the average inductor current for an IBB is always greater than the load current. Therefore, choose a buck regulator with a greater maximum load current when using it as an IBB.

$$I_L = I_{OUT} \cdot \left[1 + \frac{|V_{OUT}|}{V_{IN} \cdot \eta}\right] \tag{4}$$

$$I_{PEAK} = I_{OUT} \cdot \left[1 + \frac{|V_{OUT}|}{V_{IN} \cdot \eta}\right] + \frac{V_{IN}}{2 \cdot F_s \cdot L} \cdot D$$

$$I_{VALLEY} = I_{OUT} \cdot \left[1 + \frac{|V_{OUT}|}{V_{IN} \cdot \eta}\right] - \frac{V_{IN}}{2 \cdot F_s \cdot L} \cdot D \tag{5}$$

The peak and/or valley current limit of the converter dictate the maximum inductor current and therefore the maximum load current that can be supplied. Equation 5 can be modified to a slightly more user friendly form, and used to help choose a buck regulator that has enough current capability to be used in a given IBB application. If we choose a typical value for the inductor current ripple ($\Delta I_L$) as 30% of the output current, then we can use Equation 6 to determine the peak and valley of the inductor current for a given application. As an example, suppose we need to convert +12 V to –5 V at a load current of 2 A. Using $\Delta I_L$ = 0.6 A and an efficiency of 0.85, in Equation 6, we find an $I_{PEAK}$ of 3.28 A and an $I_{VALLEY}$ of 2.68 A. A regulator such as the LMR33630 has a peak current limit of 3.85 A (minimum) and a valley current limit of 2.9 A (minimum). Since our peak and valley currents are less than the peak and valley current limits of the device, this regulator is suitable for the application. A device such as the LMR14030 uses peak current limit only, with a minimum specification of 4.5 A. This regulator would also be a good candidate. Notice that these are all "3-A" regulators, even though we only need 2 A of load current in our example. A "2-A" regulator such as the LMR33620 having peak and valley current limits of 2.9 A (minimum) and 1.95 A (minimum) would not work. Note that the worst case for calculating the current occurs at the minimum input voltage and/or when the IBB is boosting.

$$I_{PEAK} = I_{OUT} \cdot \left[1 + \frac{|V_{OUT}|}{V_{IN} \cdot \eta}\right] + \frac{\Delta I_L}{2}$$

$$I_{VALLEY} = I_{OUT} \cdot \left[1 + \frac{|V_{OUT}|}{V_{IN} \cdot \eta}\right] - \frac{\Delta I_L}{2} \tag{6}$$

## 4.3 Power Loss and Efficiency

Because of the larger voltage and current stresses in an IBB, when compared to the buck, the power loss of the IBB will be greater. This means that the efficiency of the IBB will be less than that of a buck under similar conditions. As an example the LMR33630 achieves nearly 95% efficiency when converting +12 V to +5 V at a load current of 2 A. This gives a loss of about 0.53 W. This loss could be 3 to 4 times larger when the buck is used as an IBB converting to –5 V. This would reduce the efficiency to about 85%. This reduction in efficiency needs to be taken into account when calculating the device currents as above. Unfortunately, it is not easy to estimate the efficiency before the IBB is designed and tested. The best plan is to take a conservative approach to calculating the maximum operating currents when choosing a candidate buck.

The increased power dissipation also has consequences for die temperature. Every regulator has a maximum rated die temperature that must not be exceeded. Since the IBB has more dissipation than the equivalent buck, the extra heat will need to be removed or the die temperature may get too high. This means that the total $\theta_{JA}$ of the application will have to be lowered. With modern device packaging, most of the heat will flow out of the bottom of the device and into the PCB. Therefore, the best way to reduce the $\theta_{JA}$ is to increase the PCB copper area and choose a device with a die attached paddle (DAP) to help dissipate the heat. The application report *AN-2020 Thermal design by insight, not hindsight* provides guidance for achieving good thermal performance from your PCB layout.

## 4.4 Small Signal Behavior

Although the IBB is built using an ordinary buck regulator, the small signal closed-loop characteristics are quite different from that of a buck. The most outstanding difference is that the IBB loop contains a "right-half-plane" (RHP) zero in the small signal frequency response. This zero adds a lagging phase to the loop, rather than leading phase, as an ordinary zero would contribute. As a result the phase margin of the closed loop response is reduced, leading to potential instability and poor load transient response. Equation 7 gives the frequency of the RHP zero.

$$F_{RHP} = \frac{V_{IN}^2}{\left(V_{IN} + \left|V_{OUT}\right|\right)} \cdot \frac{1}{2\pi \cdot L \cdot I_{OUT}} \tag{7}$$

Generally, the RHP frequency must be about 4 times the loop gain crossover frequency. From Equation 7 we see that decreasing the size of the inductance will increase the frequency of the RHP zero and help to keep it away from the loop gain crossover point. However, the minimum inductance may be limited by other considerations. Another way to help with this issue is to reduce the loop gain crossover frequency by using a larger output capacitance than would normally be used with a buck. This may also help with the load transient response and reduce the output voltage ripple. If external feed-back resistors are used (as in Figure 3), then a feed-forward capacitor across the top feed-back resistor can be used. Sometimes this capacitor can give enough phase lead to improve both the phase margin and load transient response. When selecting a buck regulator to use as an IBB, a converter utilizing current mode control is the best choice. Current mode control provides a small signal loop response with fewer poles (and less phase lag) than a voltage mode controller. This tends to reduce the impact of the extra phase lag from the RHP zero. Some regulators feature external loop compensation components. These devices allow the designer much more flexibility in setting the loop gain crossover frequency and tailoring the loop response.

### 4.4.1 Measuring IBB Bode Plots

Since the ground of the buck regulator is floating on the negative output, taking a Bode plot for the IBB needs some consideration. The setup shown in Figure 6 has proven helpful when taking this measurement in our lab. Note that the grounds of the input probes to the frequency response analyzer need to be floating with respect to the input power supply and load ground (system ground), while the injection transformer used with the analyzer, isolates the source. The probe grounds (common) are connected to the negative output as shown in Figure 6 . These connections must form a star point as close as possible to the bottom terminal of $R_{FBB}$. The value of $R_{INJ}$ is usually between 10 Ω and 50 Ω.

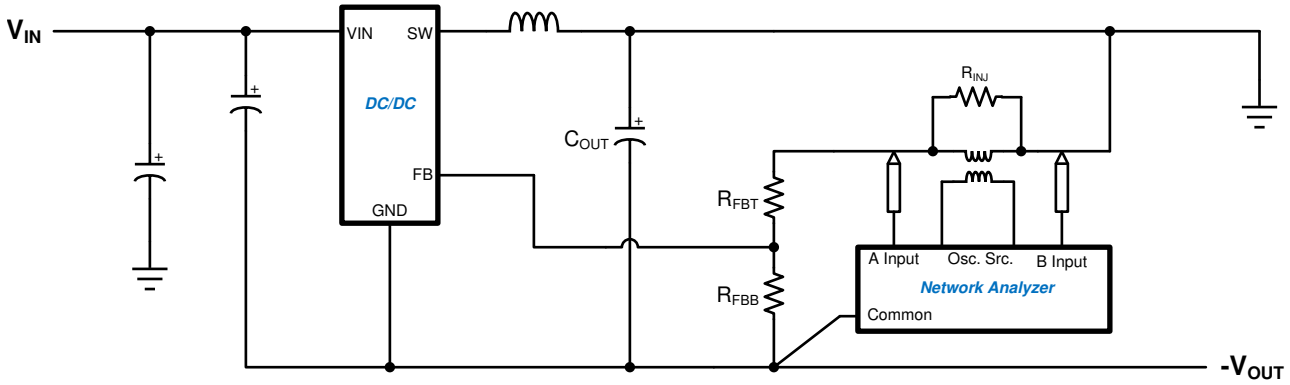


**Figure 6. Set-up for Measuring Bode Plots for an IBB**

### 4.4.2 Testing Load Transients on an IBB

One of the best ways to test the stability and robustness of any design is to perform load transient testing. The circuit shown in Figure 7 can be used with the IBB. The PFET is used as a source follower, allowing the load pulse parameters to be set by the pulse generator. This arrangement allows the pulse generator ground to be the same as the system ground. With this method both the load current amplitude and the slew rate of the current pulse are under the control of the pulse generator. The pulse generator amplitude is adjusted to give the desired load current pulse magnitude. Measure the output voltage transient near the terminals of the output capacitor. Size the PFET and R based on the required load current. A value of R = 0.1 Ω is convenient for load currents in the range of 1 A to 3 A. The power dissipation in the PFET must be checked, especially at higher output voltages and loads.

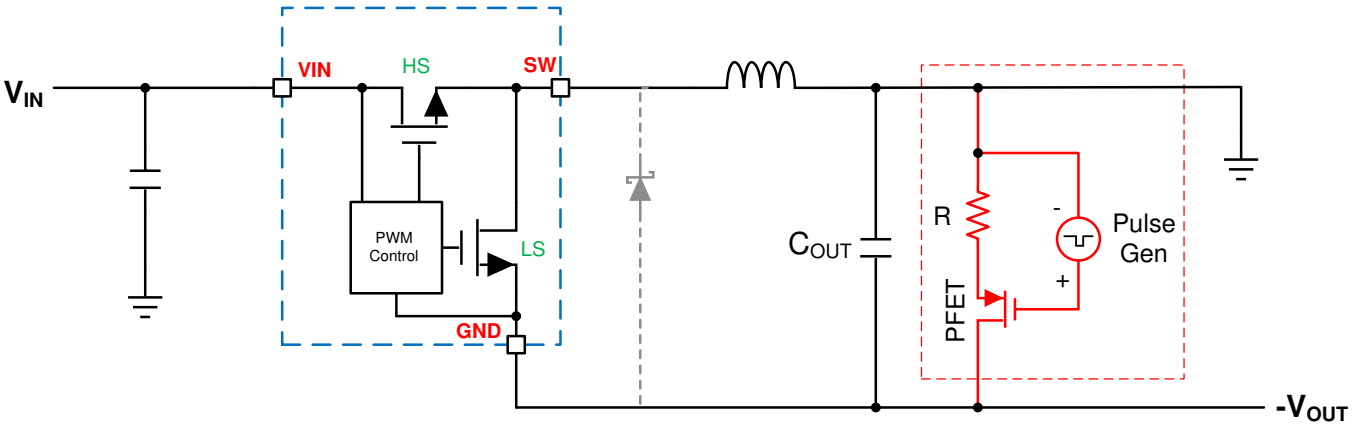


**Figure 7. Set-up for Measuring Load Transient Response for an IBB**

### 4.4.3 Simulation

Simulating an IBB can be tricky. Typically, you can't take a simulation model for a buck and use it directly for an IBB. This is because the internal circuits in the model are referenced to a global "ground", or zero volt reference node. As we have seen, for the IBB topology, the IC ground becomes the output voltage in the application. There are two ways to get around this issue. In many cases, you will find a dedicated IBB model on the product folder for the device you are interested in. Usually the file name will contain wording such as "inverting", or "IBB". These are the same models as for the buck regulator, but with the ground of the internal circuits separated from the zero volt reference. These models can be used directly to simulate an IBB. Where a dedicated IBB model is not available, the trick shown in Figure 8 can be used. With this method, the input supply is boot-strapped across the input and output of the buck converter. In this case you must be careful when monitoring voltages to ensure that you have the correct reference point for the measurement.

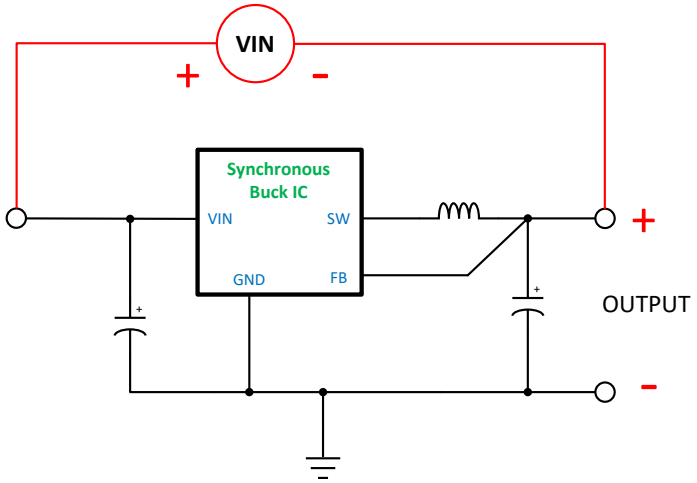


**Figure 8. Simulation of IBB**

## 5 Component Selection for the IBB

The required external components for an IBB are the same as that for a buck, with the exception of an extra input capacitor as shown in Figure 9.

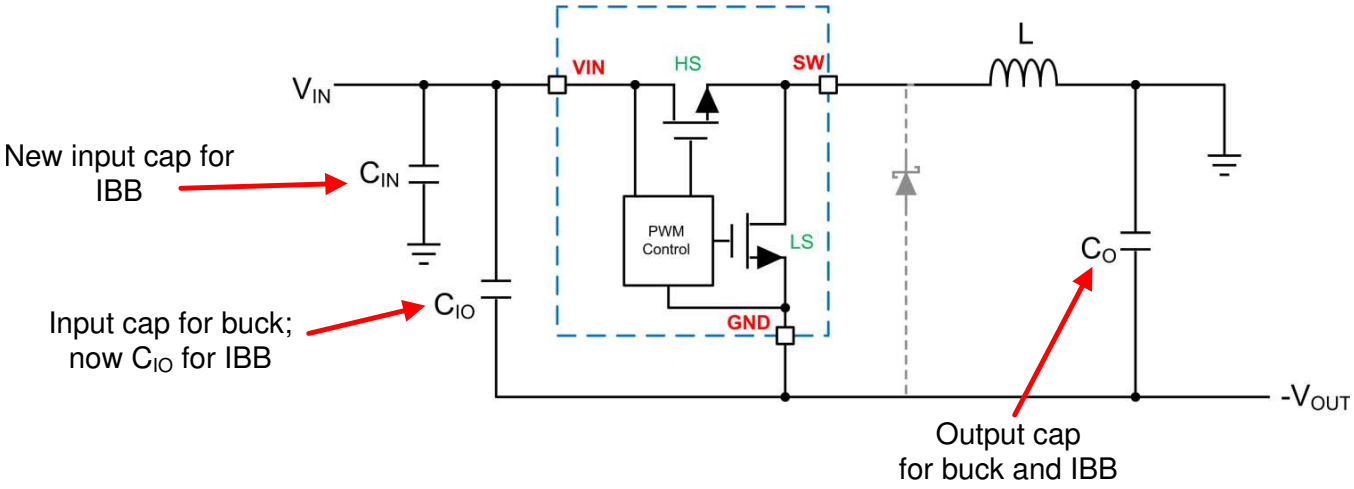


**Figure 9. IBB External Components**

### 5.1 Inductor Selection

The inductor for the IBB is selected based on the desired ripple current, much like any other DC/DC converter. Typically a value of between 20% and 40% of the load current is used for $\Delta I_L$. Equation 8 and Equation 4 can then be used to determine the value of L along with the maximum inductor current. This information is used to select a standard inductor that is suitable for the application.

$$L = \frac{V_{IN}}{F_s \cdot \Delta I_L} \cdot \frac{|V_{OUT}|}{V_{IN} \cdot \eta + |V_{OUT}|} \quad (8)$$

where

- $F_s$ = Switching frequency (Hz)

### 5.2 Capacitor Selection

As we see from Figure 9 the input capacitor(s) of the buck become the $C_{IO}$ of the IBB. Typically this will be one or two ceramic capacitors in parallel with a small case size high frequency by-pass capacitor. To size these capacitors, use the recommendations in the buck data sheet; they can also be increased if desired. $C_{IO}$ can help with load transients by providing a path from input to output for the load current transient. Remember that the $C_{IO}$ bank will see a voltage of $V_{IN} + |V_{OUT}|$ , and must have a voltage rating in excess of this voltage to help mitigate the voltage derating effect of the ceramic capacitors. As a first pass, the output capacitor can be sized based on the buck data sheet recommendations. Although the first pass should be stable, the output capacitors will probably need to be increased to get the best performance. Finally, the "new" input capacitor from $V_{IN}$ to system ground helps to provide a low impedance path at the input for the IBB. This can be a ceramic or a large value aluminum electrolytic.

The RMS current in $C_{IO}$ is calculated as for an ordinary buck, while the RMS current in $C_O$ is calculated as that for a boost converter. The currents and duty cycle found in the above equations are used for these calculations.

### 5.3 External Feed-back Divider

If an external feedback divider is used, the values can be calculated the same way as for a buck. Be sure to follow the procedure in the buck data sheet when designing the feedback divider network.

## 6 General Considerations

In general the recommendations in the buck data sheet can be followed during the detailed design of the IBB, while taking account of the differences in operation outlined above. This should give a good starting point and a solution that can be performance tested. Typically the output capacitors may need to be adjusted from this point in order to meet load transient performance. The example PCB layout shown in the buck data sheet should also be used as a starting point for the IBB. As with any DC/DC design the IBB must be thoroughly tested before committing to production. This includes basic functionality and efficiency over the operating input voltage, output voltage, temperature and load. Bode plots and load transient testing should also be conducted, in order to ensure that the design has adequate stability margins.

Most regulators have Spice models available that can be used to simulate an ordinary buck application. However, these models cannot be used with an IBB, unless they are specifically designed for the inverting configuration. This is true since most Spice models have internal global ground connections. This prevents the use of the "GND" node as the negative output node. Always check the model before using it in an IBB application.

## 7 Auxiliary Functions

From the connections of the IBB we see that the "ground" of the buck regulator is referenced, or floated, on the negative output voltage. Since all of the control signals of the buck are referenced to its ground terminal, this means that these functions will need to be level-shifted to system ground if they are to be utilized by the system. These functions and the extra circuitry required to use them in an IBB are discussed next.

### 7.1 Enable Input Level Shift

If it is required that the system control the enable function of the IBB, then a simple level shifter is required. Two possible circuits are shown in Figure 10.

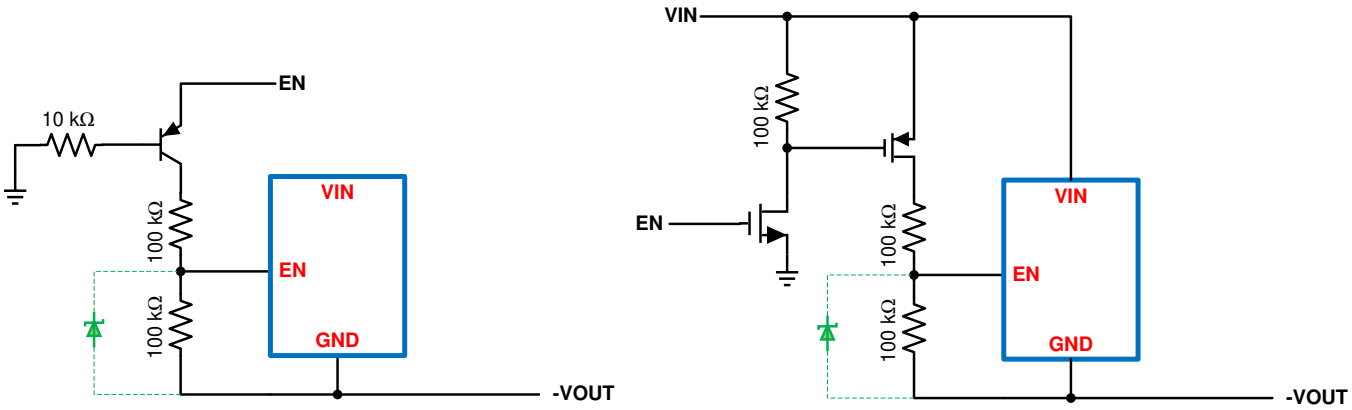


**Figure 10. Enable Level Shifters**

The circuit on the left has a large hysteresis in the threshold and requires a small amount of current from the controlling logic. However, it requires only one transistor. The circuit on the right has no hysteresis and requires no current from the logic, but requires two transistors. In any case, be sure that the EN input of the buck can withstand the full input voltage rating of the regulator (from datasheet *Absolute Maximum Ratings* section). If not, then a Zener diode, rated below the maximum enable voltage limit, must be used as shown. Even if the system is not required to control the enable of the regulator, this input must still be terminated correctly to keep the regulator turned on. In this case, consult the buck datasheet for the correct connections to the enable input.

In some systems the user may wish to use the enable control as an input undervoltage lockout (UVLO) feature. The best way to do this would be to use one of the enable level shifters shown, with an external op-amp/reference to provide the UVLO function. The TLV6713 , or similar product, could be used with one of the circuits shown in Figure 10 to provide an input UVLO feature for an IBB.

## 7.2 Synchronizing Input Level Shift

Some regulators have a synchronizing input for locking the switching frequency to the system clock. One of the level shifters shown in Figure 11 can be used to provide this function.

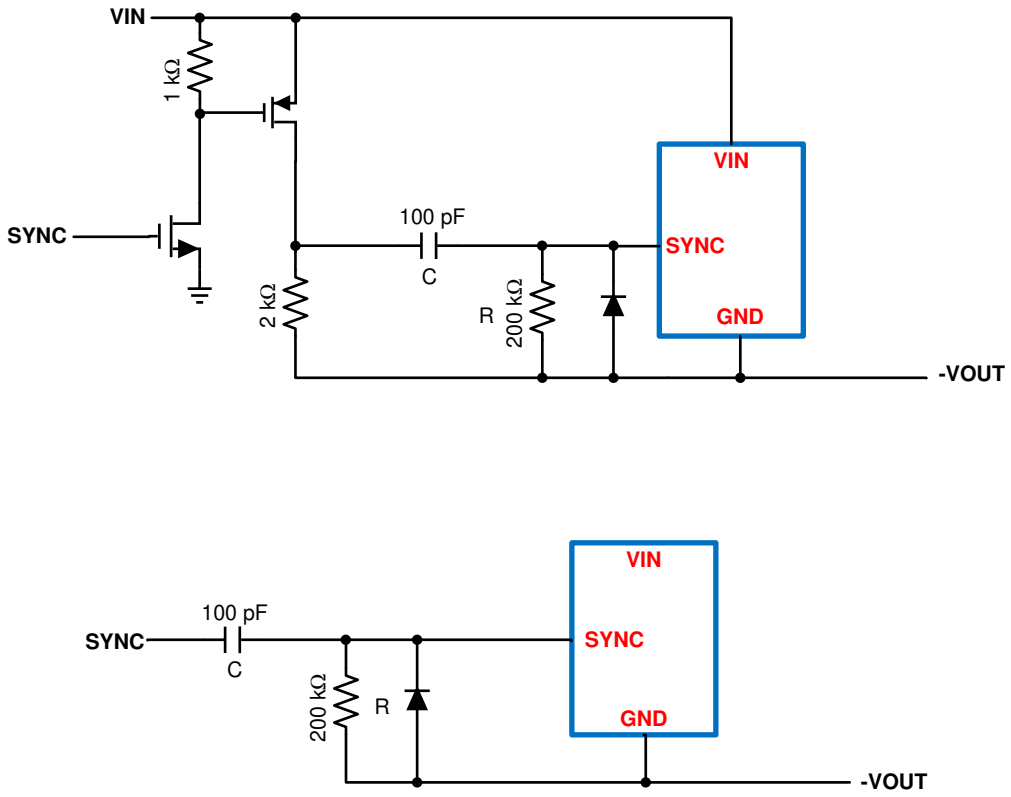


**Figure 11. Synchronization Level Shifters**

The lower schematic shows a simple solution, but requires a low impedance drive signal. The solution in the upper schematic although more complex allows the use of ordinary logic drive. Also, this solution requires that the **SYNC** input can withstand $V_{IN}$ + $|V_{OUT}|$. In all cases the RC time constant should be much longer than the switching period.

## 7.3 Power-Good Flag Level Shift

Many applications require a "power-good" or "reset" flag from the DC/DC converter to alert the µC that the output voltage is within specification. The circuits shown in Figure 12 can be used to level shift the status flag to the system ground.

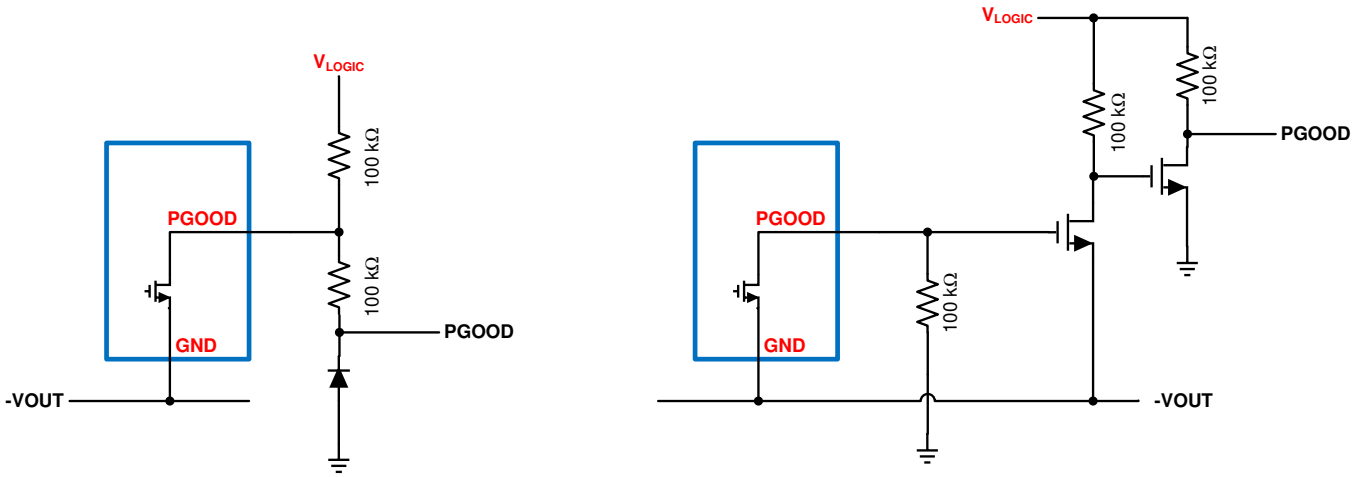


**Figure 12. Power-Good Flag Level Shifters**

The circuit on the left is simple, however the **PGOOD** signal swings below ground by a diode drop. The circuit on the right is slightly more complicated, giving a **PGOOD** signal that swings to zero volts. In either case the **PGOOD** signal swings high to the user defined $V_{LOGIC}$ level. Be sure to check the *Absolute Maximum Rating* on the power good pin from the buck data sheet. For the circuit on the left, the power good pin must withstand $V_{LOGIC}$ + $|V_{OUT}|$. For the other design the power good must withstand $|V_{OUT}|$.

## 7.4 Output Clamp

Many times the negative supply is used in conjunction with a positive rail to supply a common load such as an op amp. If one of the supplies starts up before the other, it may try to pull the other supply to its level, preventing proper start-up of the slower regulator. Also, with the presence of $C_{IO}$, the negative output may be momentarily pulled slightly positive when the input supply is turned on. Both of these issues can be solved by placing a diode clamp across the negative output as shown in Figure 13.

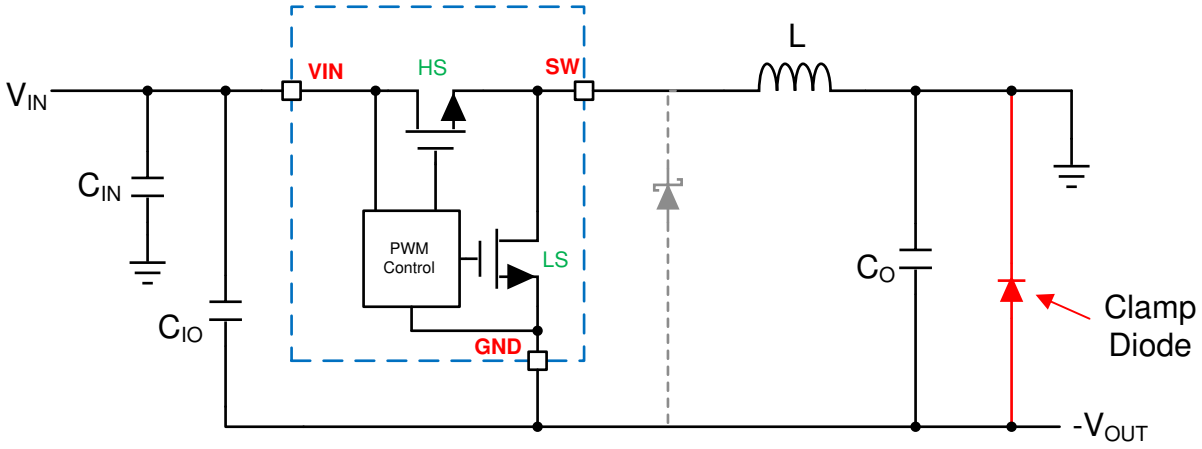


**Figure 13. Output Clamp Diode**

## 7.5 Output Noise Filtering

As mentioned previously, a post filter may be needed on the output of the IBB to reduce the ripple voltage to acceptable levels. Typically this takes the form of a simple low-pass LC filter. Take the feedback for the regulator before the filter in order to avoid introducing extra phase lag into the regulator loop gain. Design the filter with low resistance to reduce the DC voltage drop to the load, while remaining well damped. In some cases a resistor across the inductor of the filter can help achieve this compromise.

# 8 Design Examples

Two design examples will now be given to help clarify the process. The auxiliary functions mentioned above can be added if needed.

## 8.1 Converting +12 V to –5 V at 3 A

The design objectives are shown in Table 1 .

**Table 1. +12V to -5V, 3-A Design Specifications**

| $V_{IN}$ | $V_{OUT}$ | $I_{OUT}$ | SWITCHING FREQUENCY |
|---|---|---|---|
| +12 V | -5 V | 2.5 A | 400 kHz |

First, calculate the maximum voltage that the buck regulator will experience. This is simply the input voltage plus the output voltage; or +17 V. Next calculate the value of power inductance. For this example, use a $\Delta I_L$ of 30% of $I_{OUT}$ or 0.75 A. We will also assume an efficiency of 0.85 throughout this example. Using Equation 8 we determine a value of 13 µH. We will choose a standard value of 10 µH. Rearranging Equation 8 we can calculate the actual value of $\Delta I_L$ for the 10-µH inductor and use that for further calculations. With Equation 6 we find that $I_{PEAK}$ = 4.2 A and $I_{VALLEY}$ = 3.2 A. The average inductor current being 3.7 A. Looking at the LMR33640 we find that the minimum peak current limit is 4.8 A, and the minimum valley current limit is 3.9 A. These are within our limits, so we will use this device for the example. We would then choose a 10-µH inductor with at least a 5-A current rating. Note that in this example, you might be able to squeeze out 3 A of load current if the designer is OK with getting very close to the minimum guaranteed spec for the current limits. In this example, 3 A of load would give a typical peak current of about 4.9 A, and 3.9A for the valley current. Usually these values would be "too close for comfort", since the current will change with input voltage and the tolerance of the inductor. However, it may allow the designer to provide some head room for any momentary surge currents that may exist in the particular application.

For $C_{IO}$ we use the data sheet recommendations. We find that a 10-µF ceramic is required. In addition place a small case size 0.22-µF bypass cap close to the VIN and GND pins of the device. Also, as mentioned in the data sheet, $C_{IN}$ can be a small aluminum electrolytic of 47 µF to 100 µF. The data sheet recommends 4 × 22-µF ceramics for the output capacitor bank for a 5-V, 4-A, 400-kHz design. This is a good starting point for our IBB. Allow space on the PCB for extra output capacitors if they are required to improve the load transient response and/or the loop stability. The values of $C_{BOOT}$ and $C_{VCC}$ remain the same as with the positive buck; 0.1 µF and 1 µF, respectively.

The LMR33640 requires a feedback voltage divider. Use the data sheet values for a 5-V output. In this case we use $R_{FBT}$ = 100 kΩ and $R_{FBB}$ = 24.9 kΩ. Also, leave a place on the PCB for a $C_{FF}$ capacitor so that the loop stability can be optimized. Choose the LMR33640A to get 400 kHz. If the enable or PGOOD functions are needed, one of the level shifters shown previously can be used.

Once the design is completed, measure the efficiency to ensure that the converter can supply the required load current over the entire range of input voltage and ambient temperature. The complete schematic for the +12 V to –5 V design using the LMR33640 is shown in Figure 14.

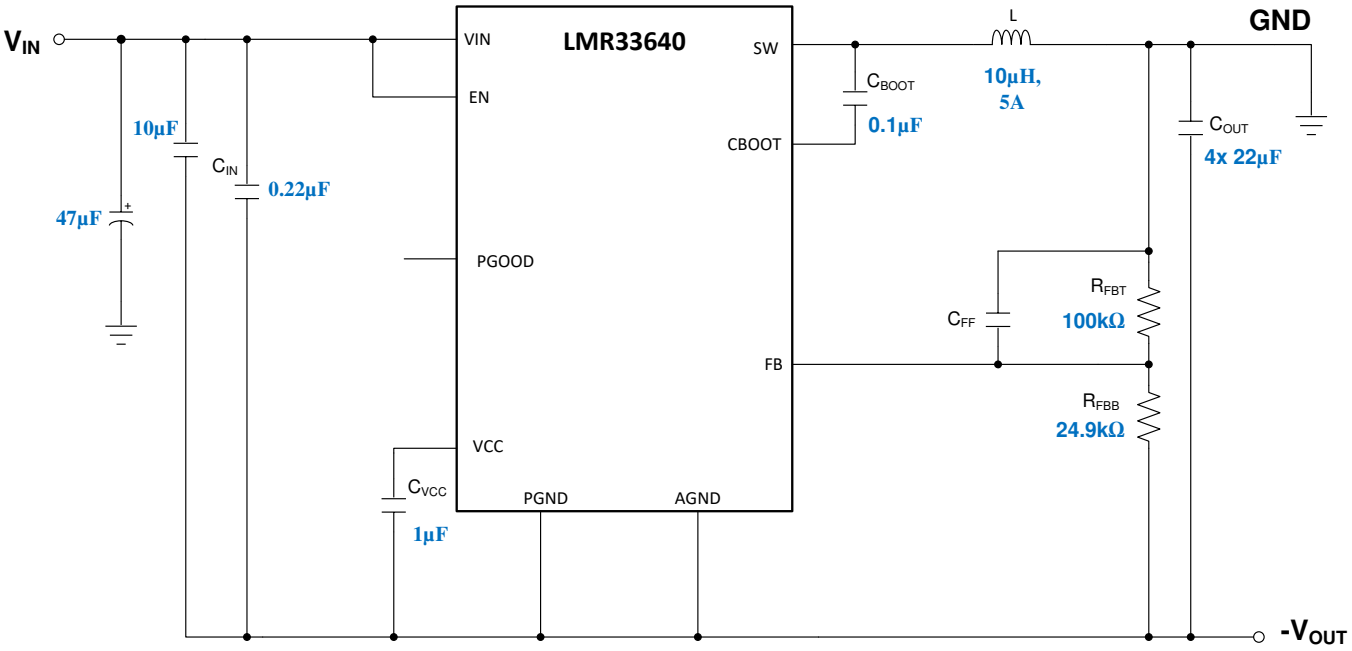


**Figure 14. +12 V to –5 V, 3-A Design with the LMR33640**

## 8.2 Converting +5 V to –5 V at 1 A

The design objectives are shown in Table 2 .

**Table 2. +5 V to –5 V, 1 A Design Specifications**

| $V_{IN}$ | $V_{OUT}$ | $I_{OUT}$ | SWITCHING FREQUENCY |
|---|---|---|---|
| +5 V | -5 V | 1 A | 400 kHz |

The maximum voltage seen by the regulator is 10 V. The inductor is calculated based on 30% of 1 A, or 0.3 A. We find an inductance of 22 µH; a standard value. With an efficiency of 0.85, the peak and valley currents are 2.33 A and 2.02 A, respectively. The average inductor current is about 2.18 A. The LMR14020 has a minimum peak current limit of 2.5 A. We will use the LMR14020 for the this example. So our inductor will be 22 µH rated for at least 3 A.

For $C_{IO}$ we use the data sheets recommendation of one 10-µF capacitor and one 0.1-µF capacitor rated for at least 16 V. For $C_{IN}$ a small aluminum electrolytic of 47µF to 100µF can be used. For a +5 V, 2 A design the data sheet recommends one 47 µF or two 22 µF ceramic capacitors. This is a good starting point for our IBB. Allow space on the PCB for extra output capacitors is they are required to improve the load transient response and/or the loop stability. The value of $C_{BOOT}$ is 0.1 µF.

The LMR14020 requires a feed-back voltage divider. From the data sheet we arrive at: $R_{FBT}$ = 100 kΩ and $R_{FBB}$ = 17.8 kΩ. Also, leave a place on the PCB for a $C_{FF}$ capacitor so that the loop stability can be optimized. To set the switching frequency to 400 kHz, we use an RT = 61.9 kΩ. The SS input can be used to increase the soft-start time if desired; otherwise leave it open. If using a soft-start capacitor on this pin, it should be returned directly to the device GND pin. If enable control is not needed, connect the EN input to VIN. Otherwise one of the level shifters shown previously can be used to control the EN input.

Once the design is completed, measure the efficiency to ensure that the converter can supply the required load current over the entire range of input voltage and ambient temperature. The complete schematic for the +5 V to –5 V design using the LMR14020 is shown in Figure 15.

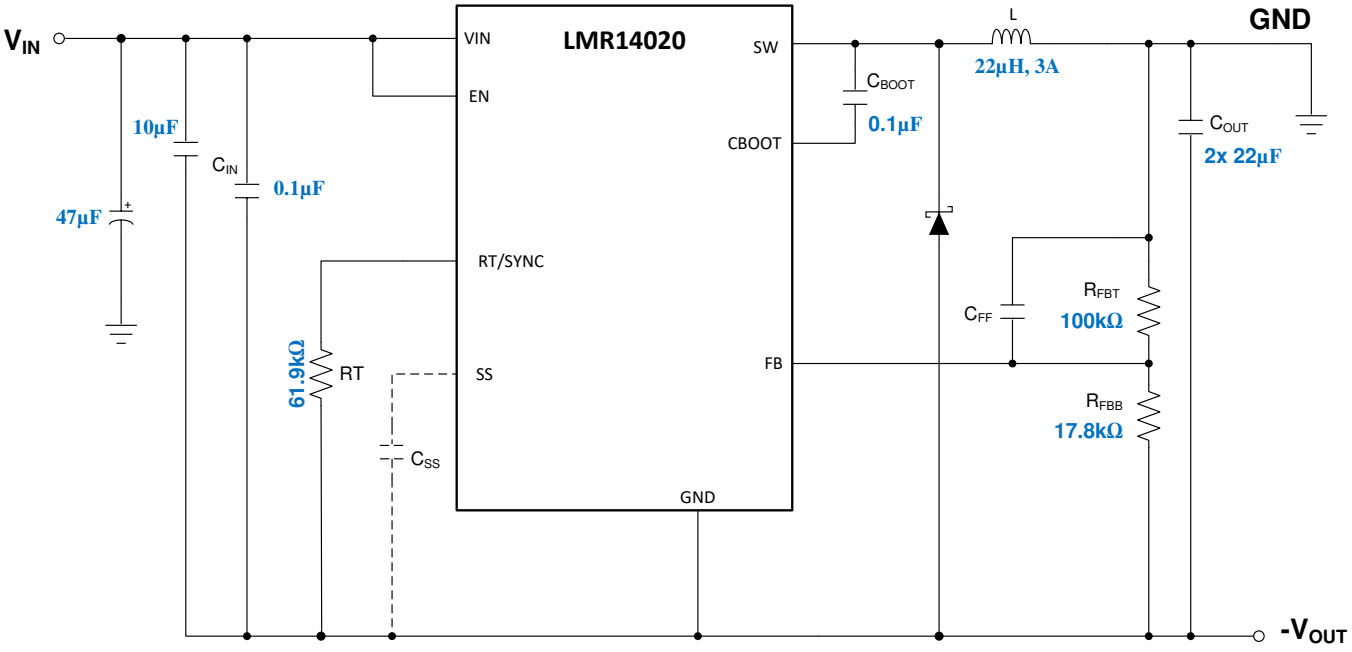


**Figure 15. +5 V to –5 V, 1-A Design with the LMR14020**

## 9 Summary

To convert a buck DC/DC converter to an IBB follow these steps:

- Calculate the maximum voltage seen by the regulator from: $V_{IN} + |V_{OUT}|$
- Based on an assumed efficiency and a $\Delta I_L$ = 30% of $I_{OUT}$, use Equation 4 and Equation 6 to calculate the maximum inductor currents.
- Choose a suitable buck DC/DC regulator to use as the IBB.
- Refer to the data sheet to size the device capacitors and feedback dividers, etc.
- Decide if any auxiliary or level shifting circuits, etc. are required
- Make the power connections shown in Figure 2 as follows:
  1. Reassign buck positive output as system ground.
  2. Reassign buck regulator ground nodes as the negative output voltage node.
  3. Positive input stays the same.
- Build the design. Be sure to follow the PCB layout guidelines in the buck data sheet. Pay particular attention to the routing of the input and output capacitors and the FB connections.
- Test the design. Check thoroughly over the entire input voltage and load current range at the expected limits of ambient temperature. Check load transients and stability margins using Bode plot tests. Finally, check the IC temperature rise to be sure that it is within the specified limits for the device.
- Texas Instruments provides many resources for designing an IBB from a buck converter. In some cases the TI Webench Design Tool can be used www.ti.com/WEBENCH . In many cases application reports are available for specific Texas Instruments devices detailing the conversion to an IBB. Please visit TI.com for more information.

The following links give details of using specific buck regulators as an inverting buck-boost converter.

1. Texas Instruments, *Create an Inverting Power Supply From a Step-Down Regulator Application Report*
2. Texas Instruments, *Using the TPS62120 in an Inverting Buck-Boost Topology Application Report*
3. Texas Instruments, *Using a buck converter in an inverting buck-boost topology Application Report*
4. Texas Instruments, *AN-1157 Positive to Negative Buck-Boost Converter Using LM267X SIMPLE SWITCHER® Regulators Application Report*
5. Texas Instruments, *AN-2027 Inverting Application for the LMZ14203 SIMPLE SWITCHER® Power Module Application Report*
6. Texas Instruments, *Inverting Applications Made SIMPLE with LM4600x and LM4360x Application Report*

## Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (February 2019) to A Revision | Page |
|---|---|
| • Added new section on simulation | 9 |
| • Changed this section of enable UVLO | 12 |
| • Changed this example to LMR33640 | 15 |

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265