Application Report
SNLA296–July 2018

LM71/LM71-Q1 Errata

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ABSTRACT

Problem: ***When the time interval between two consecutive temperature reads is less than the maximum specified conversion time of 270 ms there is a possibility to read an erronenous temperature value. The source of the problem is due to the fact that the external chip select (CS) signal is not synchronized by the LM71 internal clock. This leaves a possibility of the LM71 state machine incorrectly sample the CS signal, resulting in an erronenous temperature value being updated.***

Workaround: Following a power on reset, the user must allow at least 270 ms before making the first read transaction to ensure a first valid temperature read. After the first read, make sure that the time interval between any two consecutive temperature reads is greater than the maximum conversion time of 270 ms.

Statistics on LM71 bad readout rate:

CS Interval	Test Duration	Events	Events Per Hour
17.5 µs	5.5 hours	119	21.64
25 µs	17 hours	17	1
32.6 µs	22.5 hours	4	0.18
500 µs	4 days	8	0.083
10 ms	3 days	1	0.014
100 ms	7 days	0	0
270 ms	5 days	0	0

Contents

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1 LM71 Theory of Operation

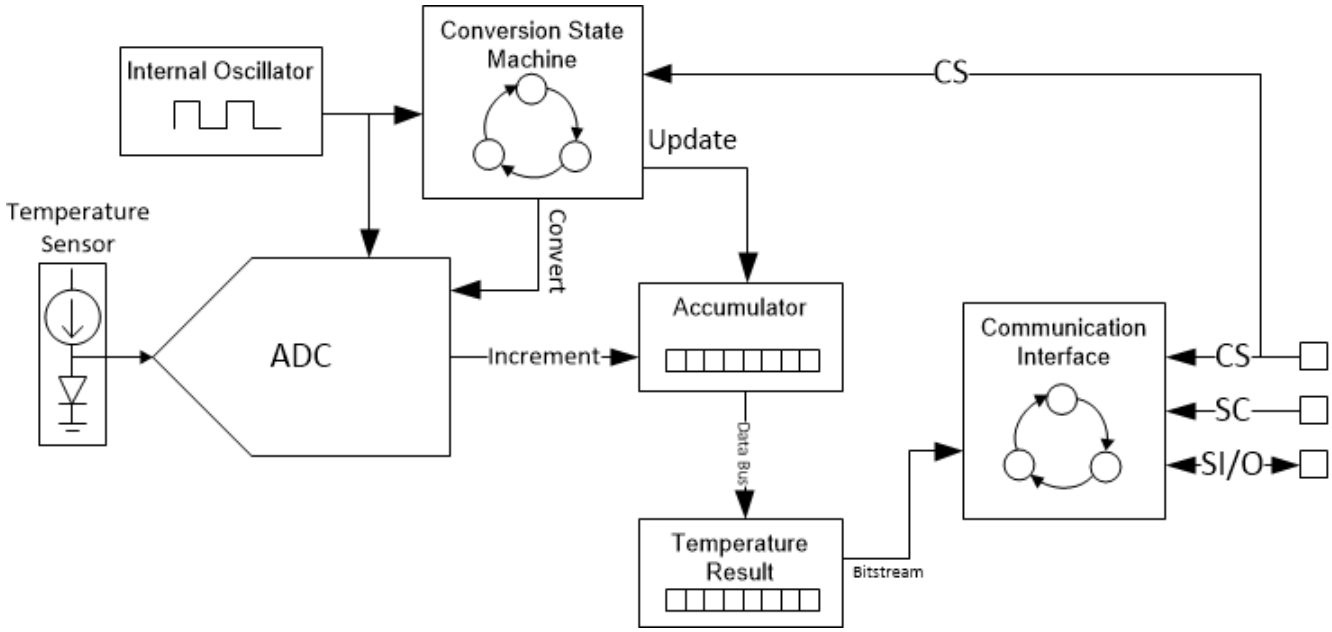

Figure 1. LM71 High-Level Block Diagram

Figure 1 is a top level block diagram of the internal architecture of the LM71 that shows the blocks used during temperature conversion and during SPI transactions on the communication interface. The device uses a diode-based temperature sensor. The voltage created across the diode with a fixed current is a function of temperature. An internal ADC is used to monitor this voltage and determine what the temperature is. Internal ADC conversions are controlled by a conversion state machine. At the end of a conversion, the temperature result register is updated with the conversion result. The value in the temperature result register is what is read by the customer during an SPI read transaction with the device.

2 LM71 Conversion Finite State Machine

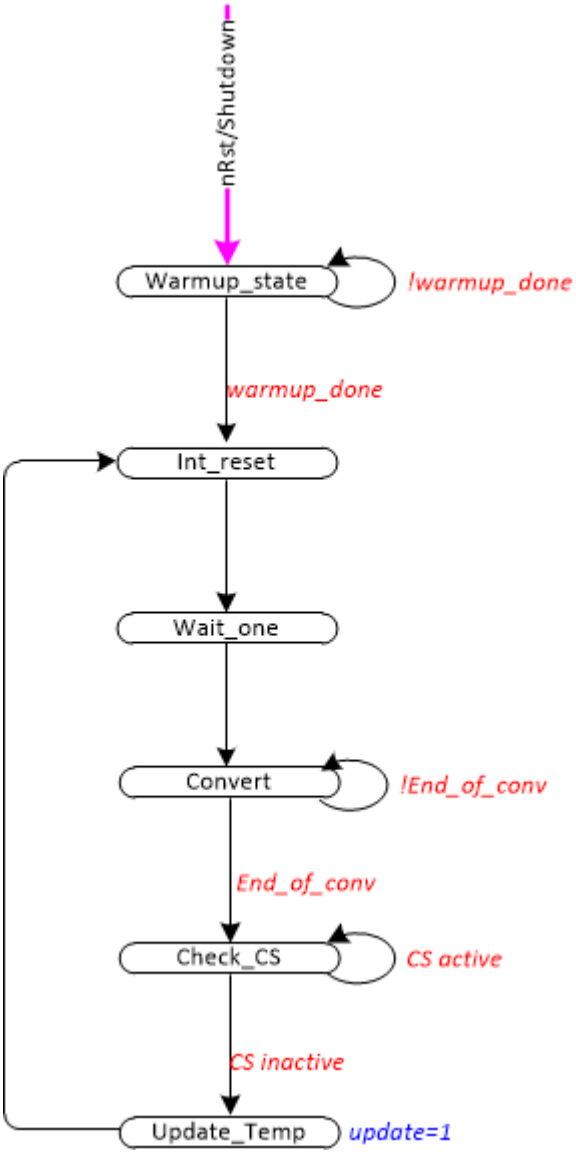

Figure 2. Conversion Finite State Machine

Figure 2 shows the conversion state machine diagram. When the device powers up or comes out of shutdown, the device moves into a “warmup_state” to wait for the internal analog circuits to turn on. The device then proceeds into a portion of the state machine that loops continuously and triggers the ADC to perform temperature conversions. An internal register shown as “Accumulator” in Figure 1 is initialized with a negative number before the conversion begins during the “Int_Reset” state. That is followed by a 1 clock cycle wait state. The device then moves into the “Convert” state during which it asserts the convert line that tells the ADC to perform a conversion. Over the duration of the conversion, the ADC will increment the value in the accumulator. When the conversion ends, the device moves into the “Check_CS” state.

3 Anomalous Operation Description

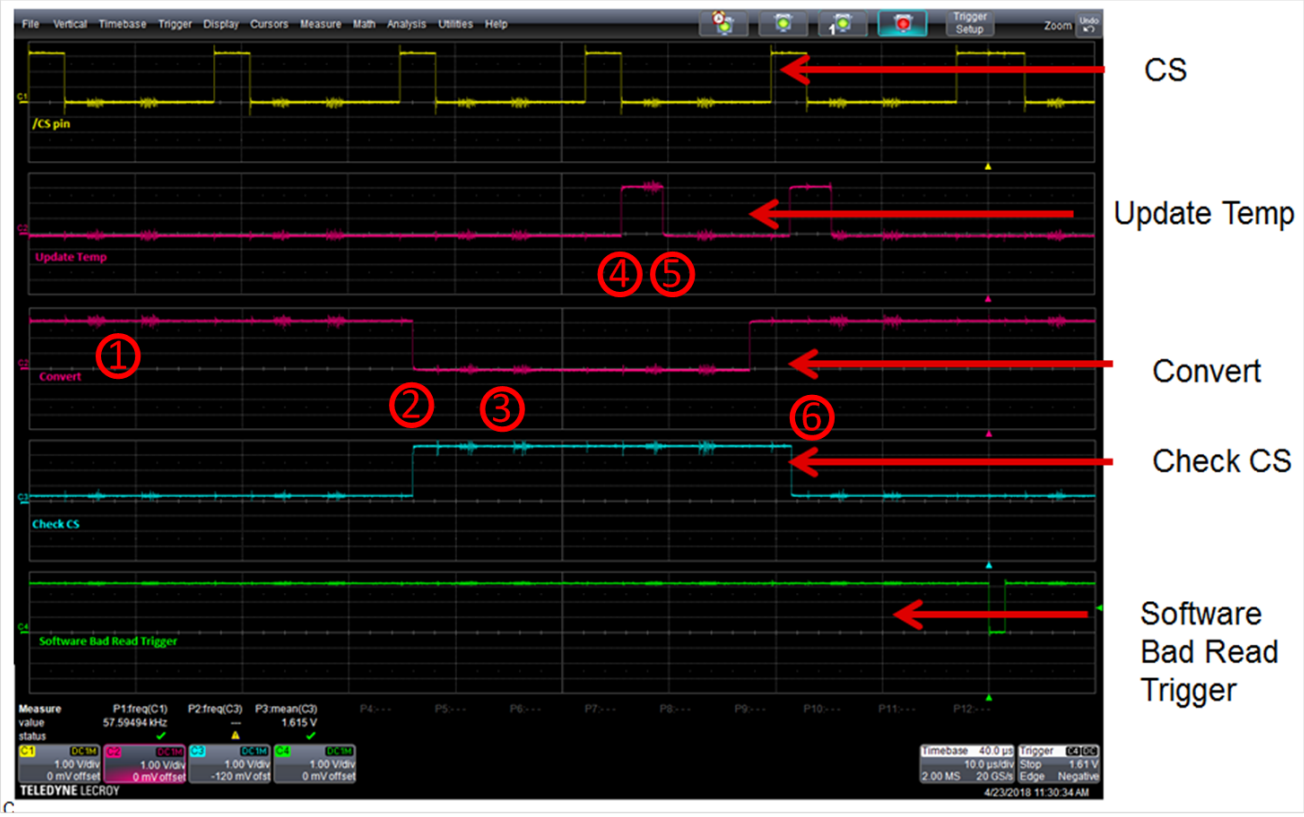

Figure 3. Oscilloscope Capture of Erroneous Result Update

Figure 3 is an oscilloscope screen capture that shows what happens on the internal nodes when the device enters this invalid state. Notice that the device is read at a very fast rate (once every 17 µs). The yellow line is the CS line during the reads. The first pink line is an indicator that the device is in the "Update_Temp" state. The second pink line is an indicator that the device is in the "Convert" state. The blue line is an indicator that the device is in the "Check_CS" state. The green line is a software trigger that is created by a microcontroller in the debug setup. The software trigger is used to tell the oscilloscope to perform the screen capture. The low pulse on the green line is generated whenever the comparison of two consecutive reads exceeds a pre-determined threshold (set to 20C in this scope capture).

As described before, the device moves into the "Check_CS" state at the end of a conversion where it monitors the polarity of the signal on the CS pin. While the device is in the "Check_CS" state and CS is low, the device waits until CS goes high. However, CS is generated external to the device, which makes it asynchronous to the internal conversion state machine. As a consequence, there is a very low probability that CS transitions can put the device into an invalid state for a short duration where the conversion state machine operates in two states at the same time. This is shown in the screenshot capture in Figure 3.

From the left of the capture, you can see that the device is performing a conversion as the "Convert" line is high at **timestamp 1**. At **timestamp 2**, when the conversion ends and the "Convert" line goes low, the "Check_CS" line goes high to indicate that the device entered the "Check_CS" state as expected. The device stays in this state as it monitors the CS line and detects the low CS line at **timestamp 3**. The problem starts at **timestamp 4**. The part of the state machine that is looking for the CS line to go high samples the CS line as high and enables the "Update_Temp" state. This is indicated by the Update_Temp line going high.

During normal operation, the part of the state machine that disables the “Check_CS” state would also sample the CS line going high and then disable the Check_CS state at this time. However, the screen capture shows this did not happen, indicating that this part of the FSM missed the CS high sample, sampled the CS as low, and decided to keep the device in the “Check_CS” state. This means that the device is in both the “Update_Temp” state and the “Check_CS” state at the same time, which is an invalid condition.

In the next clock cycle at **timestamp 5**, the device gets out of the Update_temp state after transferring the conversion result in the “Accumulator” to the “Temperature Result” register. The part of the logic that is looking to disable the “Check_CS” state, however, keeps the state enabled because the CS line is low. At **timestamp 6**, this logic samples the CS line as high and then disables the “Check_CS” state. At the same time, the logic also puts the state machine in the “Update_Temp” state for a second time as indicated by the “Update_Temp” line pulsing high a second time. In the meantime, the part of the state machine that moved ahead from the previous update pulse already reset the accumulator and started the next conversion. That part of the state machine is in the “Convert” state as indicated by the convert line being high. The second update pulse then transfers an intermediate value from the accumulator into the result register. The trailing part of the state machine reaches the “Convert State” so the device can return back to and remain in a normal state machine flow.

Now, a simple workaround to this issue is to ensure that the time interval between any two consecutive temperature reads is greater than the maximum specified LM71 conversion time of 270 ms. Following a power on reset, the user must allow at least 270 ms before making the first read transaction to ensure a first valid temperature read.

NOTE: A consecutive temperature read interval of 270 ms is more than adequate for many applications as temperature does not change that fast.

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