LMC6484QML CMOS Quad Rail-to-Rail Input and Output Operational Amplifier

Check for Samples: LMC6484QML

FEATURES

- **(Typical Unless Otherwise Noted)**
- **Rail-to-Rail Input Common-Mode Voltage Range (Ensured Over Temperature)**
- **Rail-to-Rail Output Swing (within 20 mV of Supply Rail, 100 KΩ Load)**
- **Ensured 5V and 15V Performance**
- **Operates at 3V.**
- **Excellent CMRR and PSRR: 82 dB**
- **Ultra Low Input Current: 20 fA**
- **High Voltage Gain (R_L = 500 KΩ): 130 dB**
- **Specified for 2 KΩ and 600Ω Loads**

APPLICATIONS

- **Data Acquisition Systems**
- **Transducer Amplifiers**
- **Hand-Held Analytic Instruments**
- **Medical Instrumentation**
- **Active Filter, Peak Detector, Sample and Hold, pH Meter, Current Source**
- **Improved Replacement for TLC274, TLC279**

DESCRIPTION

The LMC6484 provides a common-mode range that extends to both supply rails. This rail-to-rail performance combined with excellent accuracy, due to a high CMRR, makes it unique among rail-to-rail input amplifiers.

It is ideal for systems, such as data acquisition, that require a large input signal range. The LMC6484 is also an excellent upgrade for circuits using limited common-mode range amplifiers such as the TLC274 and TLC279.

Maximum dynamic signal range is assured in low voltage and single supply systems by the LMC6484's rail-to-rail output swing. The LMC6484's rail-to-rail output swing is ensured for loads down to 600Ω.

Ensured low voltage characteristics and low power dissipation make the LMC6484 especially well-suited for battery-operated systems.

See the LMC6482 data sheet for a Dual CMOS operational amplifier with these same features.

Connection Diagram

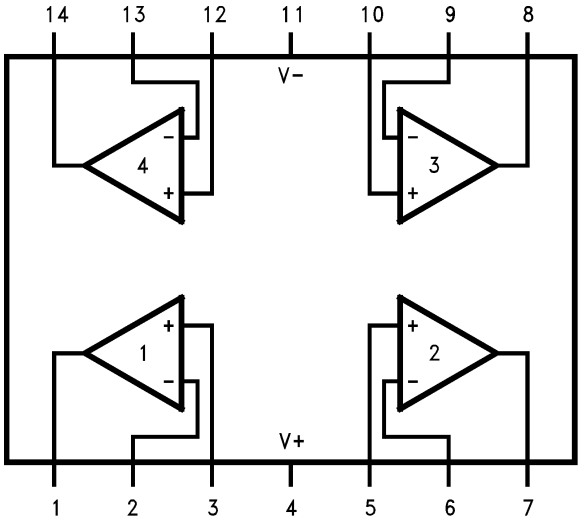


Figure 1. See 14-Pin CLGA NAC0014A Package or See 14-Pin CDIP J0014A Package

3V Single Supply Buffer Circuit

Figure 2. Rail-to-Rail Input

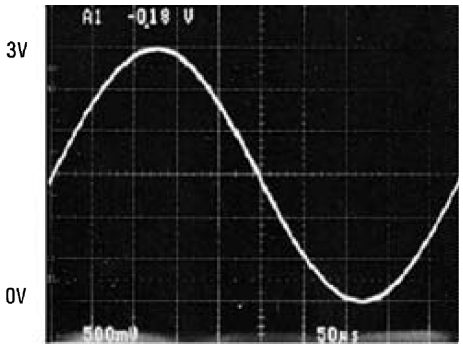
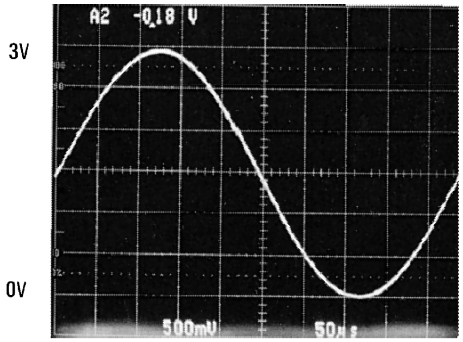
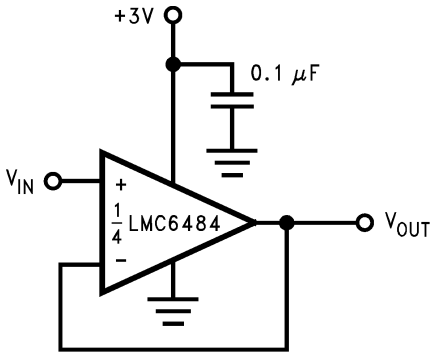


Figure 3. Rail-to-Rail Output





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Supply Voltage ($V^+ - V^-$)	16V
Differential Input Voltage	± Supply Voltage
Voltage at Input/Output Pin	(V^+) + 0.3V, (V^-) − 0.3V
Current at Input Pin (2)	±5 mA
Current at Output Pin (3), (4)	±30 mA
Current at Power Supply Pin	40 mA
Maximum Junction Temperature (T_{Jmax}) (5), (3)	150°C
Power Dissipation (5)	315mW
Storage Temperature Range	−65°C ≤ T_A ≤ +150°C
Thermal Resistance (6)	
θ_{JA}	
14LD CDIP (Still Air)	86.0°C/W
14LD CDIP (500LF/Min Air Flow)	49.0°C/W
14LD CLGA (Still Air)	116.0°C/W
14LD CLGA (500LF/Min Air Flow)	72.0°C/W
θ_{JC}	
14LD CDIP	16.0°C/W
14LD CLGA	11.0°C/W
Package Weight	
14LD CDIP	TBD
14LD CLGA	460mg
Lead Temp. (Soldering, 10 sec.)	260°C
ESD Tolerance (7)	2.0KV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.
(3) Applies to both single supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.
(4) Do not short circuit output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.
(5) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.
(6) All numbers apply for packages soldered directly into a PC board.
(7) Human body model, 1.5 KΩ in series with 100 pF.

Recommended Operating Range (1)

Supply Voltage	3.0V ≤ V^+ ≤ 15.5V
Operating Temperature Range	−55°C ≤ T_A ≤ +125°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Table 1. Quality Conformance Inspection Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp °C
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125

Table 1. Quality Conformance Inspection Mil-Std-883, Method 5005 - Group A (continued)

Subgroup	Description	Temp °C
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

LMC6484 Electrical Characteristics DC Parameters

The following conditions apply, unless otherwise specified. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage				0.75	mV	1
					1.35	mV	2, 3
I_{IB}	Input Bias Current				25	pA	1
					100	pA	2, 3
I_{IO}	Input Offset Current				25	pA	1
					100	pA	2, 3
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 15.0V$ $V^+ = 15V$		65		dB	1
				62		dB	2, 3
		$0V \le V_{CM} \le 5.0V$		65		dB	1
				62		dB	2, 3
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$		65		dB	1
				62		dB	2, 3
-PSRR	Negative Power Supply Rejection Ratio	$-15V \le V^- \le -5V$ $V_O = -2.5V$, $V^+ = 0V$		65		dB	1
				62		dB	2, 3
V_{CM}	Input Common Mode Voltage Range	$5V \le V_{CM} \le 15V$ For CMRR ≥ 50dB		V^++0.25	-0.25	V	1
				V^+	0.0	V	2, 3
I_{SC}	Output Short Circuit Current	Sourcing $V_O = 0V$		16		mA	1
				12		mA	2, 3
		Sinking $V_O = 5V$		11		mA	1
				9.0		mA	2, 3
		$V^+ = 15V$ Sourcing, $V_O = 0V$		28		mA	1
				22		mA	2, 3
		$V^+ = 15V$ Sinking, $V_O = 12V$	(1)	30		mA	1
				24		mA	2, 3
I_{CC}	Supply Current	All four Amps			2.8	mA	1
					3.6	mA	2, 3
		All four amps $V^+ = +15V$			3.0	mA	1
					4.0	mA	2, 3

(1) Do not short circuit output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.

LMC6484 Electrical Characteristics DC Parameters (continued)

The following conditions apply, unless otherwise specified. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_O	Output Swing	$V^+ = 5V$ $R_L = 2K\Omega$ to $V^+/2$		4.8	0.18	V	4
				4.7	0.24	V	5, 6
		$V^+ = 5V$ $R_L = 600\Omega$ to $V^+/2$		4.5	0.50	V	4
				4.24	0.65	V	5, 6
		$V^+ = 15V$ $R_L = 2K\Omega$ to $V^+/2$		14.4	0.32	V	4
				14.2	0.45	V	5, 6
		$V^+ = 15V$ $R_L = 600\Omega$ to $V^+/2$		13.4	1.00	V	4
				13.0	1.30	V	5, 6
A_V	Large Signal Voltage Gain	$R_L = 2K\Omega$ Sourcing	(2)	140		V/mV	4
				84		V/mV	5, 6
		$R_L = 2K\Omega$ Sinking	(2)	35		V/mV	4
				20		V/mV	5, 6
		$R_L = 600\Omega$ Sourcing	(2)	80		V/mV	4
				48		V/mV	5, 6
		$R_L = 600\Omega$ Sinking	(2)	18		V/mV	4
				13		V/mV	5, 6

(2) $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $3.5V \le V_O \le 7.5V$.

LMC6484 Electrical Characteristics AC Parameters

The following conditions apply, unless otherwise specified. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
SR	Slew Rate		(1)	0.9		V/µS	4
				0.6		V/µS	5, 6
GBW	Gain Bandwidth	$V^+ = 15V$ Set up for non-inverting		1.25		MHz	4
				1.15		MHz	5, 6

(1) $V^+ = 15V$. Connected as Voltage Follower with 10V step input, 2.5V to 12.5V for +slew, and 12.5V to 2.5V for −slew. Number specified is the slower of either the positive or negative slew rates.

Typical Performance Characteristics

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified

Supply Current vs. Supply Voltage

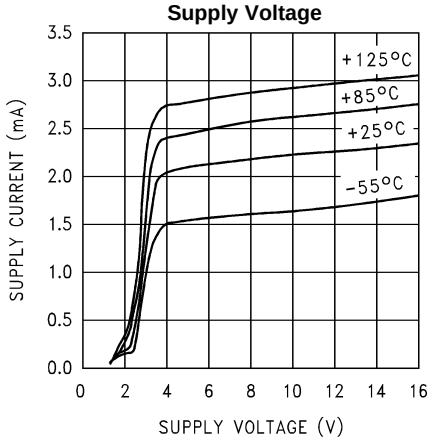


Figure 4.

Input Current vs. Temperature

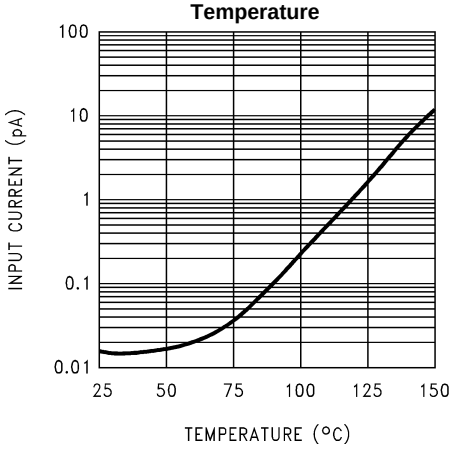


Figure 5.

Sourcing Current vs. Output Voltage

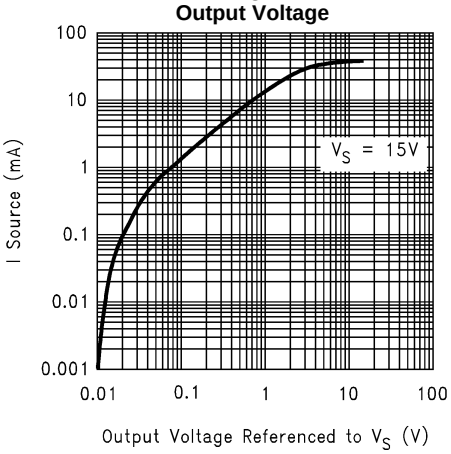


Figure 6.

Sourcing Current vs. Output Voltage

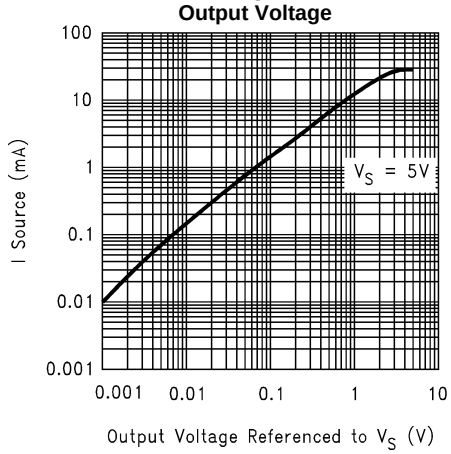


Figure 7.

Sourcing Current vs. Output Voltage

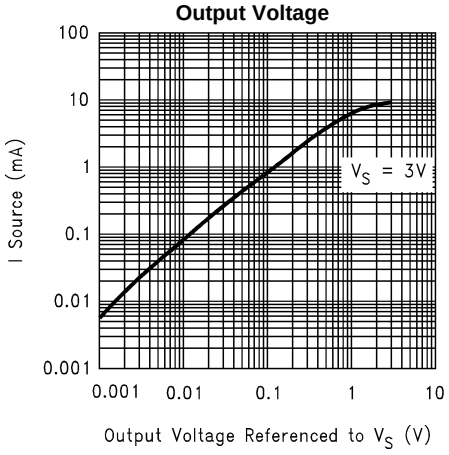


Figure 8.

Sinking Current vs. Output Voltage

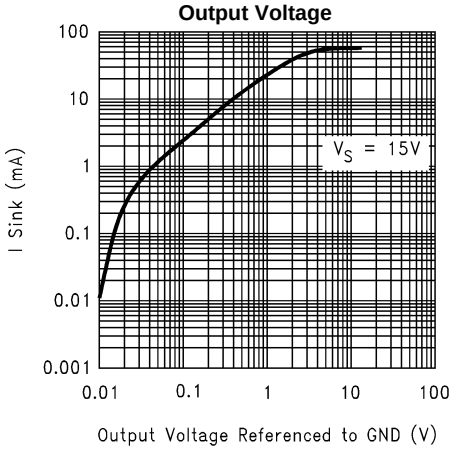


Figure 9.

Typical Performance Characteristics (continued)

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified

Sinking Current vs. Output Voltage

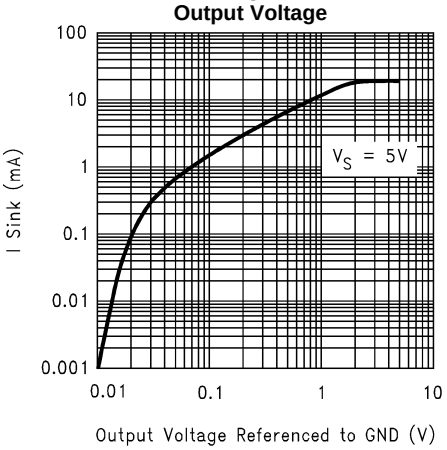


Figure 10.

Sinking Current vs. Output Voltage

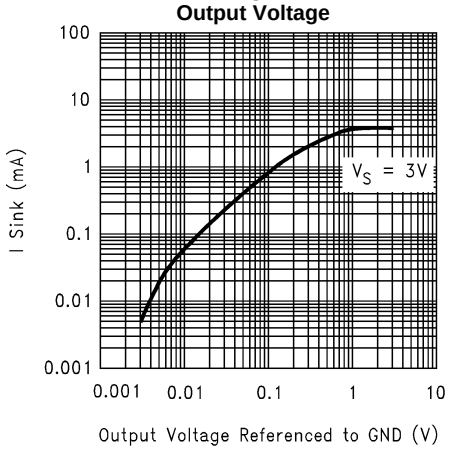


Figure 11.

Output Voltage Swing vs. Supply Voltage

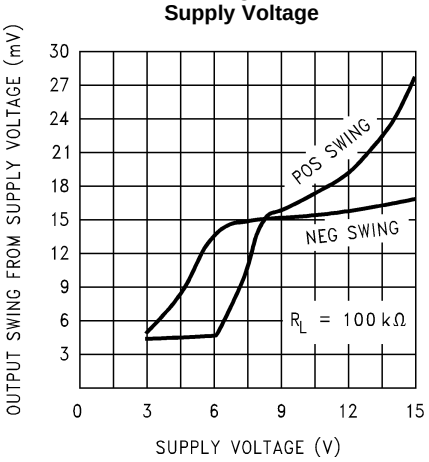


Figure 12.

Input Voltage Noise vs. Frequency

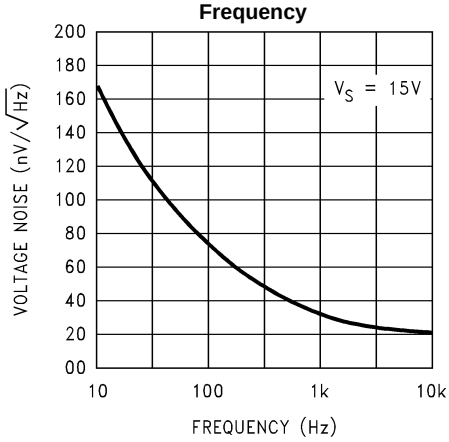


Figure 13.

Input Voltage Noise vs. Input Voltage

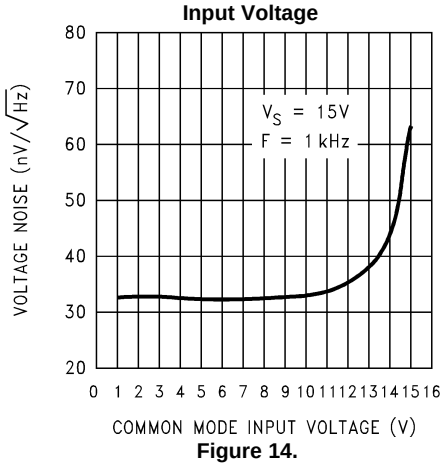


Figure 14.

Input Voltage Noise vs. Input Voltage

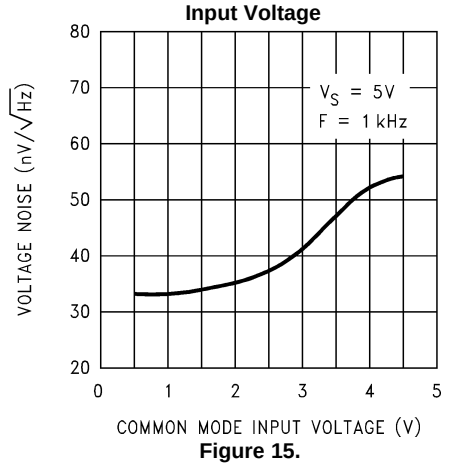


Figure 15.

Typical Performance Characteristics (continued)

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified

Input Voltage Noise vs. Input Voltage

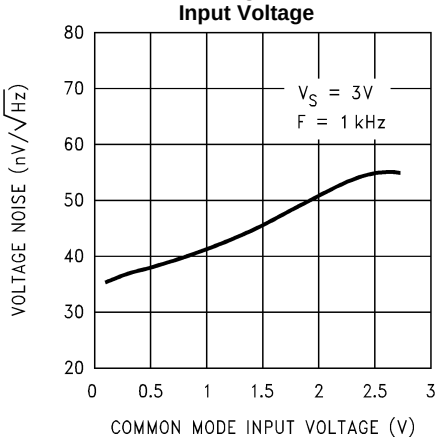


Figure 16.

Crosstalk Rejection vs. Frequency

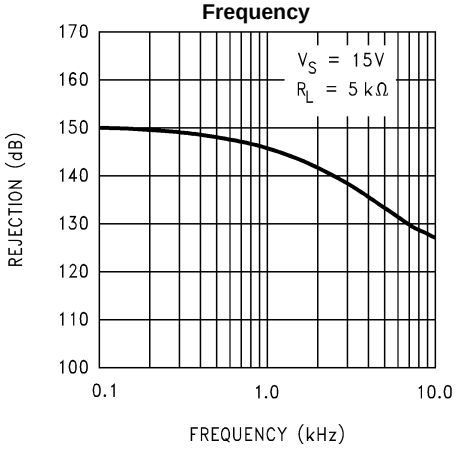


Figure 17.

Crosstalk Rejection vs. Frequency

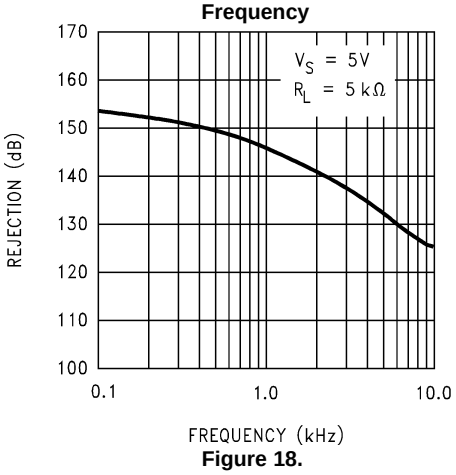


Figure 18.

Positive PSRR vs. Frequency

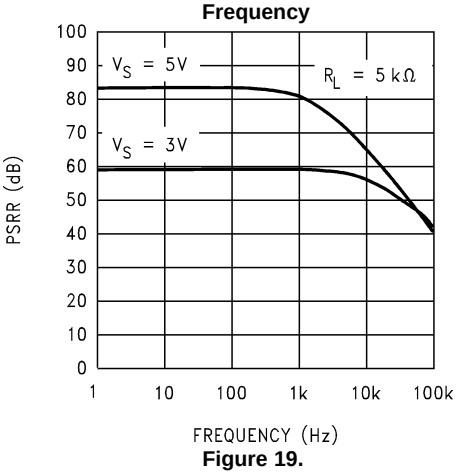


Figure 19.

Negative PSRR vs. Frequency

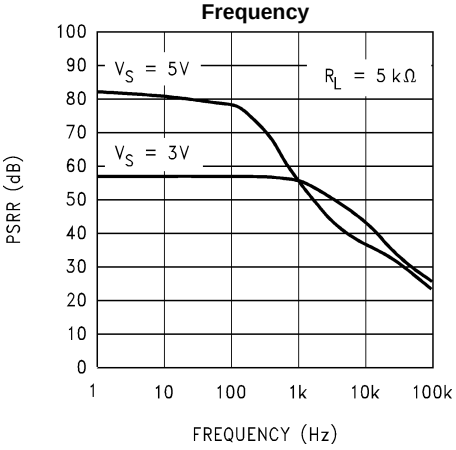


Figure 20.

CMRR vs. Frequency

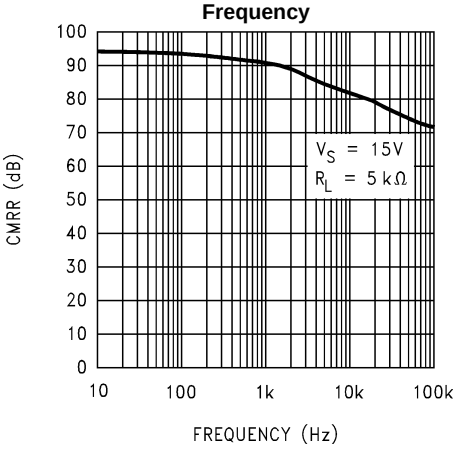


Figure 21.

Typical Performance Characteristics (continued)

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified

CMRR vs. Input Voltage

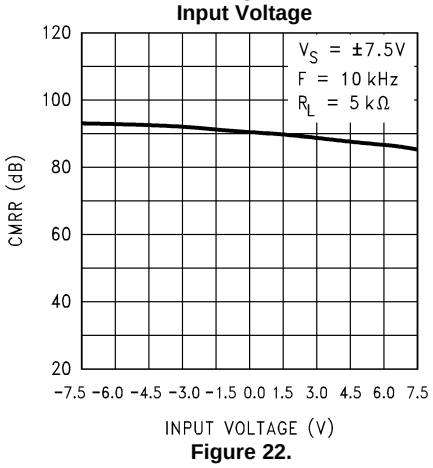


Figure 22.

CMRR vs. Input Voltage

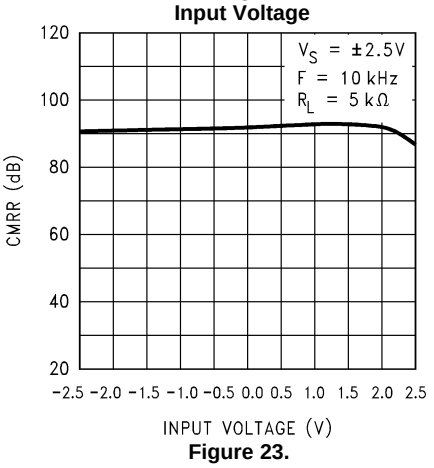


Figure 23.

CMRR vs. Input Voltage

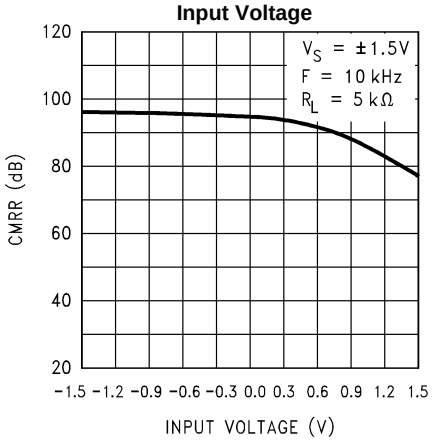


Figure 24.

ΔV_{OS} vs. CMR

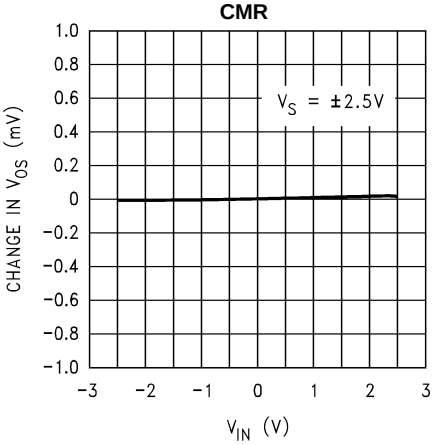


Figure 25.

Δ V_{OS} vs. CMR

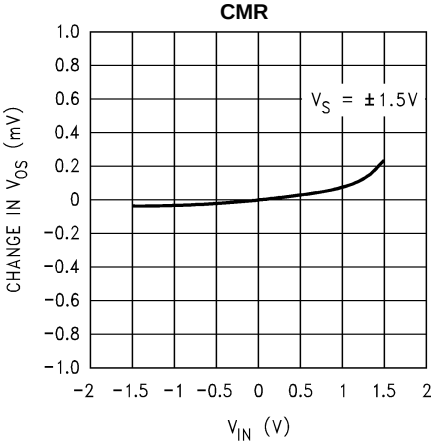


Figure 26.

Input Voltage vs. Output Voltage

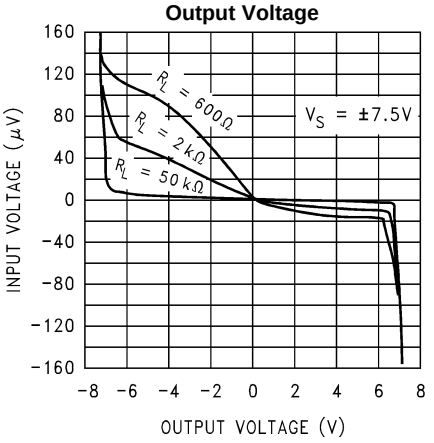


Figure 27.

Typical Performance Characteristics (continued)

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified

Input Voltage vs. Output Voltage

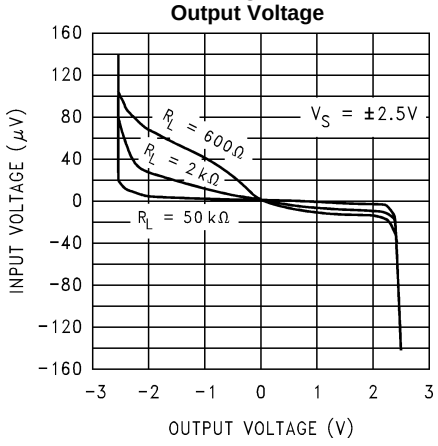


Figure 28.

Open Loop Frequency Response

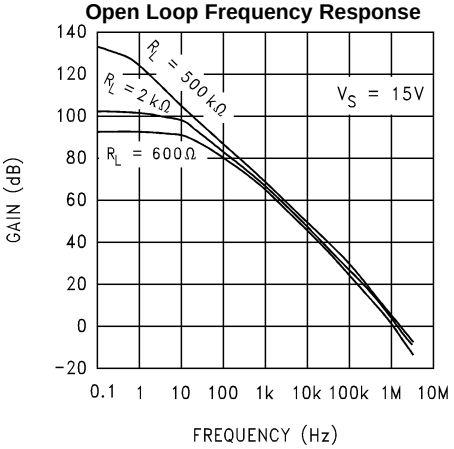


Figure 29.

Open Loop Frequency Response

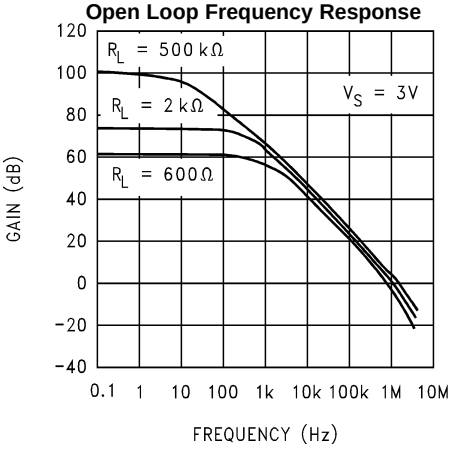


Figure 30.

Open Loop Frequency Response vs. Temperature

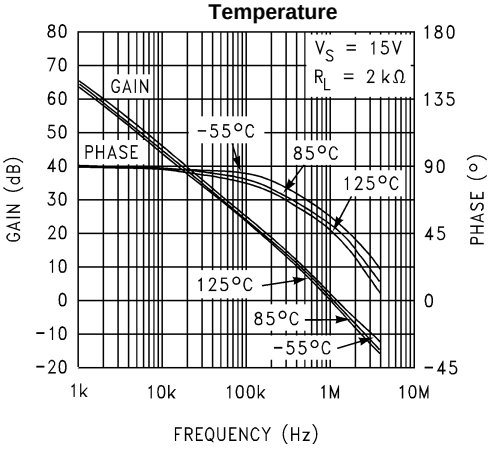


Figure 31.

Maximum Output Swing vs. Frequency

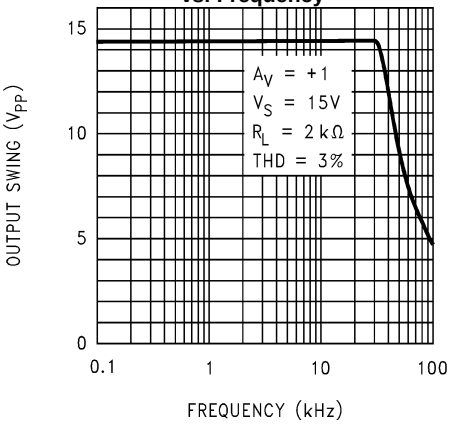


Figure 32.

Gain and Phase vs. Capacitive Load

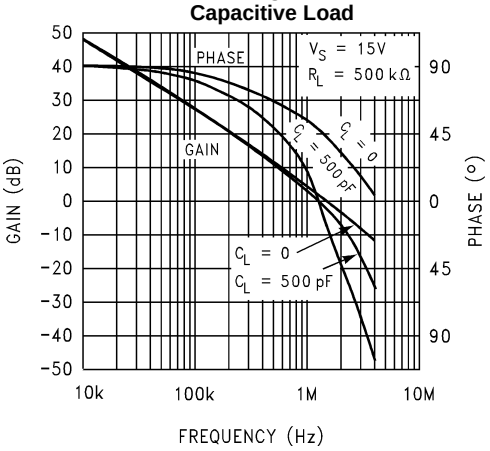


Figure 33.

Typical Performance Characteristics (continued)

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified

Gain and Phase vs. Capacitive Load

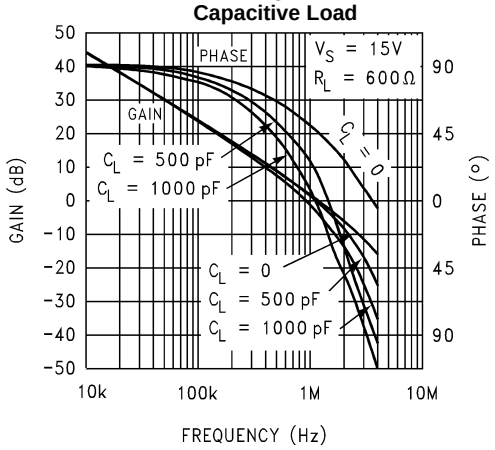


Figure 34.

Open Loop Output Impedance vs. Frequency

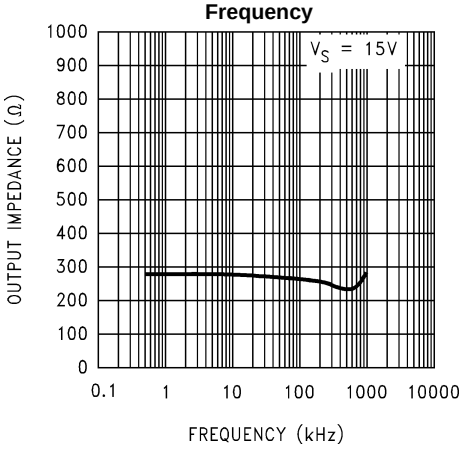


Figure 35.

Open Loop Output Impedance vs. Frequency

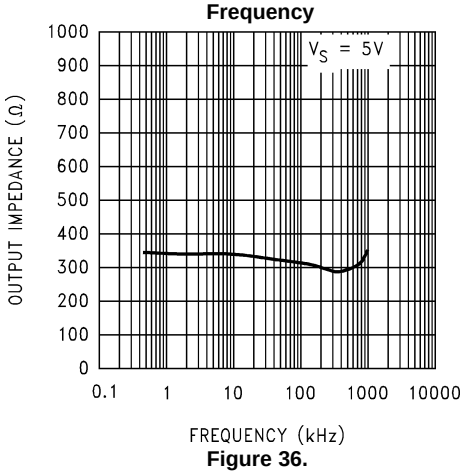


Figure 36.

Slew Rate vs. Supply Voltage

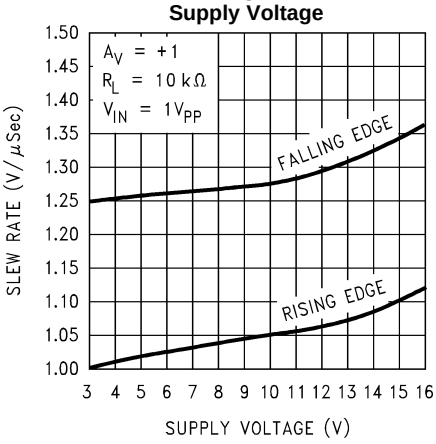


Figure 37.

Non-Inverting Large Signal Pulse Response

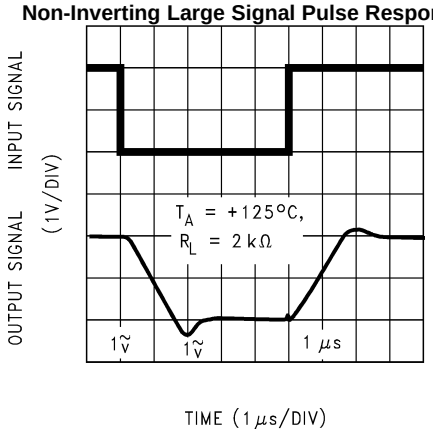


Figure 38.

Non-Inverting Large Signal Pulse Response

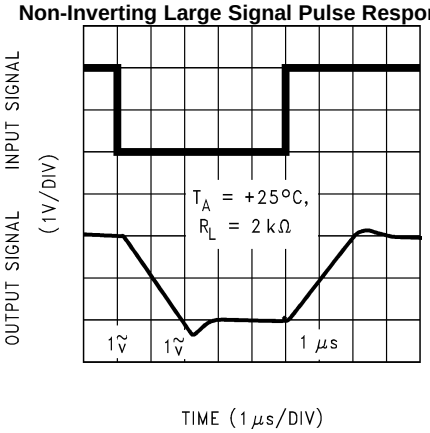


Figure 39.

Typical Performance Characteristics (continued)

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified

Non-Inverting Large Signal Pulse Response

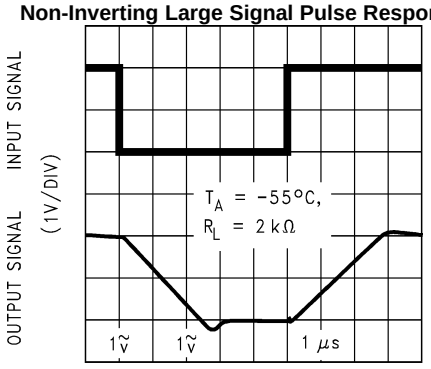


Figure 40.

Non-Inverting Small Signal Pulse Response

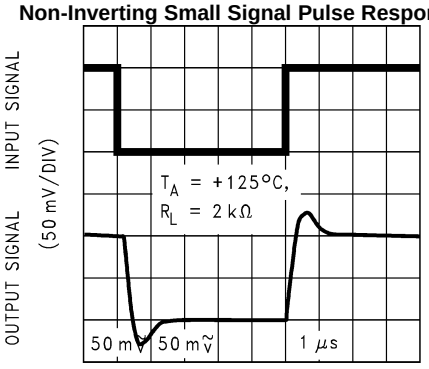


Figure 41.

Non-Inverting Small Signal Pulse Response

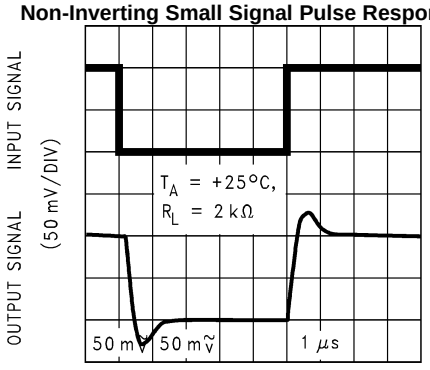


Figure 42.

Non-Inverting Small Signal Pulse Response

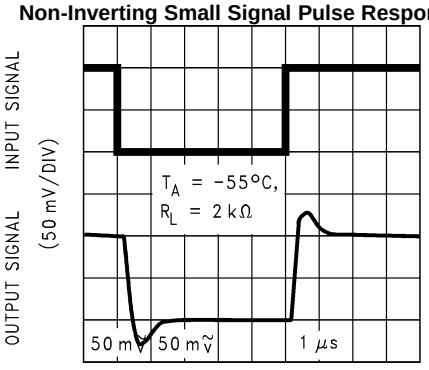


Figure 43.

Inverting Large Signal Pulse Response

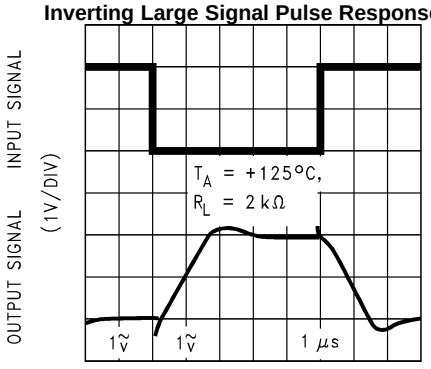


Figure 44.

Inverting Large Signal Pulse Response

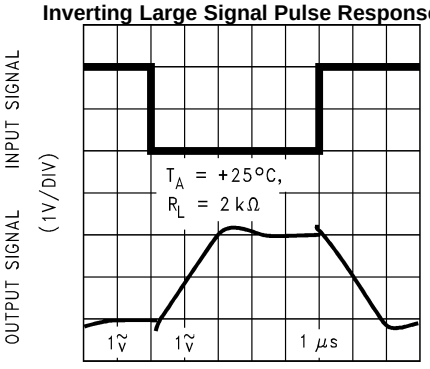
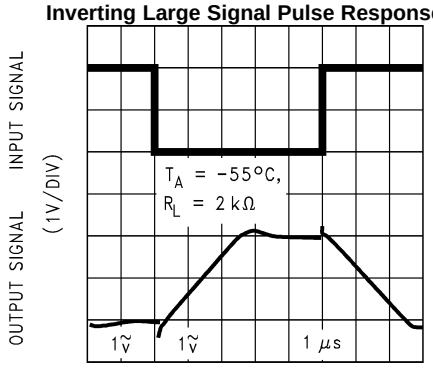


Figure 45.

Typical Performance Characteristics (continued)

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified

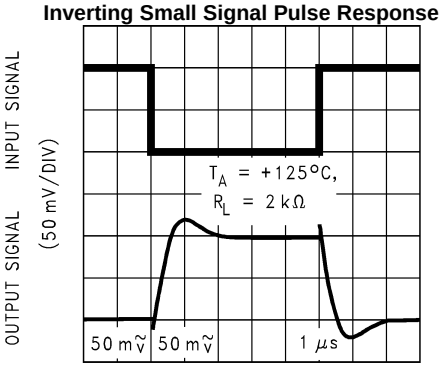
Inverting Large Signal Pulse Response



TIME (1 μs/DIV)

Figure 46.

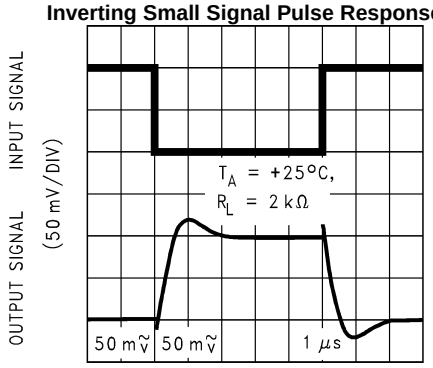
Inverting Small Signal Pulse Response



TIME (1 μs/DIV)

Figure 47.

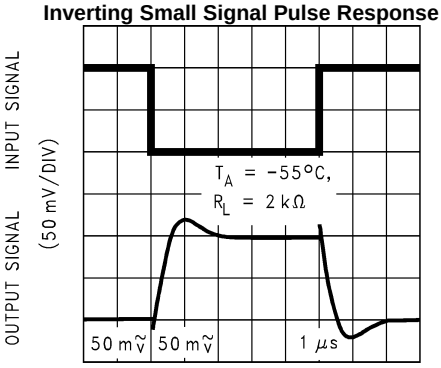
Inverting Small Signal Pulse Response



TIME (1 μs/DIV)

Figure 48.

Inverting Small Signal Pulse Response



TIME (1 μs/DIV)

Figure 49.

Stability vs. Capacitive Load

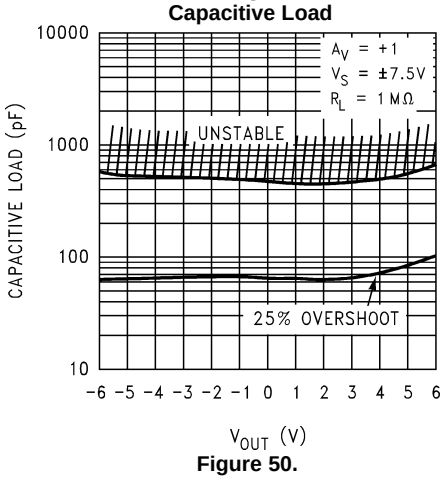


Figure 50.

Stability vs. Capacitive Load

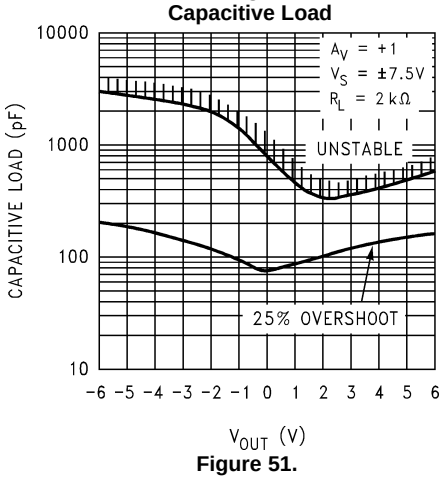


Figure 51.

Typical Performance Characteristics (continued)

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified

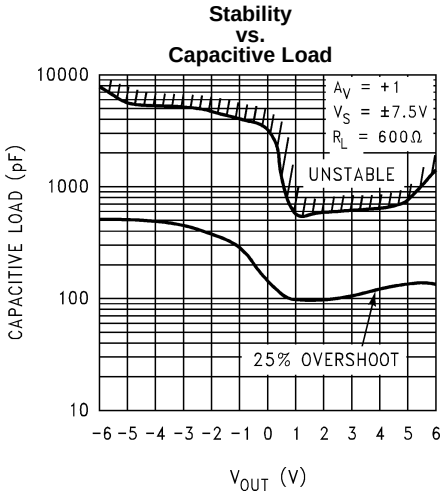


Figure 52.

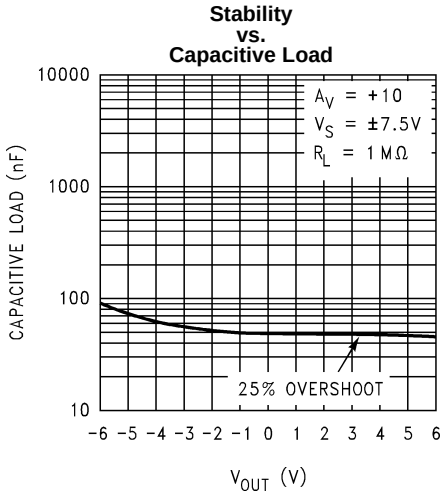


Figure 53.

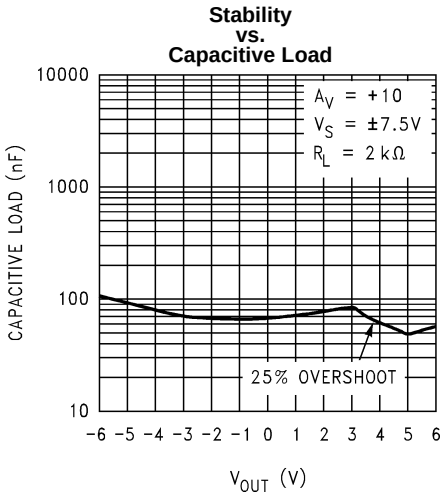


Figure 54.

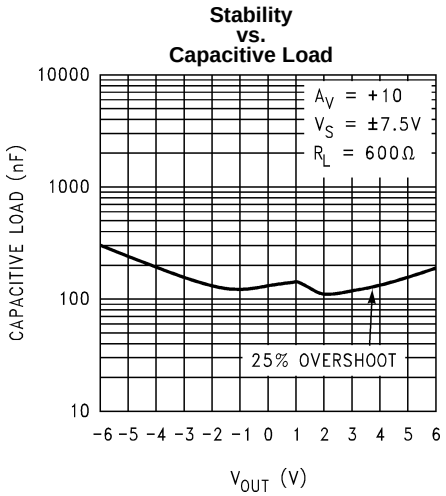


Figure 55.

APPLICATION INFORMATION

AMPLIFIER TOPOLOGY

The LMC6484 incorporates specially designed wide-compliance range current mirrors and the body effect to extend input common mode range to each supply rail. Complementary paralleled differential input stages, like the type used in other CMOS and bipolar rail-to-rail input amplifiers, were not used because of their inherent accuracy problems due to CMRR, cross-over distortion, and open-loop gain variation.

The LMC6484's input stage design is complemented by an output stage capable of rail-to-rail output swing even when driving a large load. Rail-to-rail output swing is obtained by taking the output directly from the internal integrator instead of an output buffer stage.

INPUT COMMON-MODE VOLTAGE RANGE

Unlike Bi-FET amplifier designs, the LMC6484 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. Figure 56 shows an input voltage exceeding both supplies with no resulting phase inversion on the output.

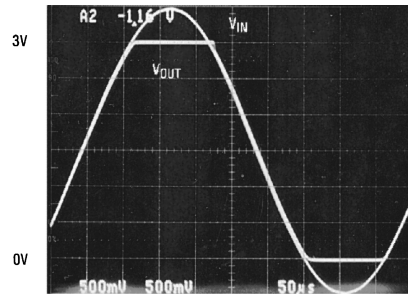


Figure 56. An Input Voltage Signal Exceeds the LMC6484 Power Supply Voltages with No Output Phase Inversion

The absolute maximum input voltage is 300 mV beyond either supply rail at room temperature. Voltages greatly exceeding this absolute maximum rating, as in Figure 57, can cause excessive current to flow in or out of the input pins possibly affecting reliability.

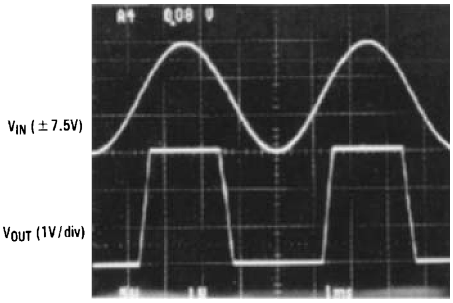


Figure 57. A ±7.5V Input Signal Greatly Exceeds the 3V Supply in *Figure 58* Causing No Phase Inversion Due to R_I

Applications that exceed this rating must externally limit the maximum input current to ±5 mA with an input resistor as shown in Figure 58.

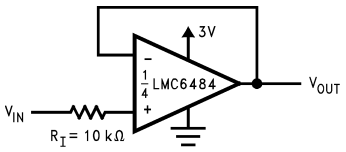


Figure 58. R_I Input Current Protection for Voltages Exceeding the Supply Voltage

RAIL-TO-RAIL OUTPUT

The approximated output resistance of the LMC6484 is 180Ω sourcing and 130Ω sinking at V_S = 3V and 110Ω sourcing and 83Ω sinking at V_S = 5V. Using the calculated output resistance, maximum output voltage swing can be estimated as a function of load.

CAPACITIVE LOAD TOLERANCE

The LMC6484 can typically directly drive a 100 pF load with V_S = 15V at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of op-amps. The combination of the op-amp's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in Figure 59. This simple technique is useful for isolating the capacitive input of multiplexers and A/D converters.

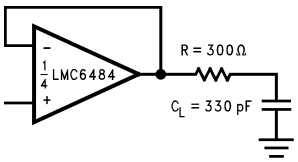


Figure 59. Resistive Isolation of a 330 pF Capacitive Load

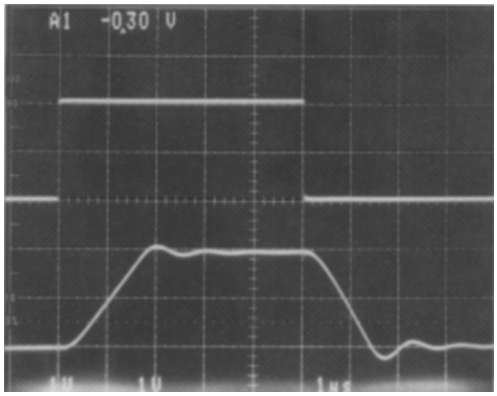


Figure 60. Pulse Response of the LMC6484 Circuit in Figure 59

Improved frequency response is achieved by indirectly driving capacitive loads as shown in Figure 61.

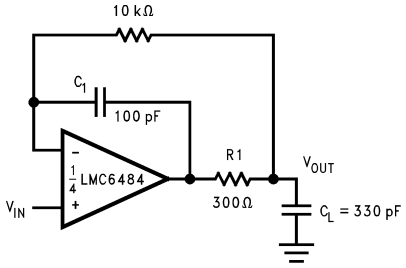


Figure 61. LMC6484 Non-Inverting Amplifier, Compensated to Handle a 330 pF Capacitive Load

R1 and C1 serve to counteract the loss of phase margin by feeding forward the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop. The values of R1 and C1 are experimentally determined for the desired pulse response. The resulting pulse response can be seen in Figure 62.

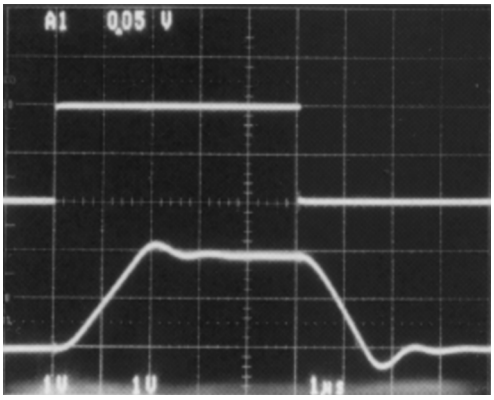


Figure 62. Pulse Response of LMC6484 Circuit in Figure 61

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance with amplifiers that have ultra-low input current, like the LMC6484. Large feedback resistors can react with small values of input capacitance due to transducers, photodiodes, and circuit board parasitics to reduce phase margins.

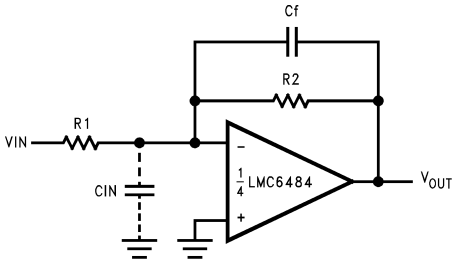


Figure 63. Canceling the Effect of Input Capacitance

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in Figure 63), C_f, is first estimated by:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \quad (1)$$

or

$$R_1 C_I \leq R_2 C_f \quad (2)$$

which typically provides significant overcompensation.

Printed circuit board stray capacitance may be larger or smaller than that of a breadboard, so the actual optimum value for C_f may be different. The values of C_f should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. when one wishes to take advantage of the ultra-low input current of the LMC6484, typically less than 20 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6484's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in Figure 64. To have a significant effect, guard rings should be placed in both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 250 times degradation from the LMC6484's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See Figure 67 for typical connections of guard rings for standard op-amp configurations.

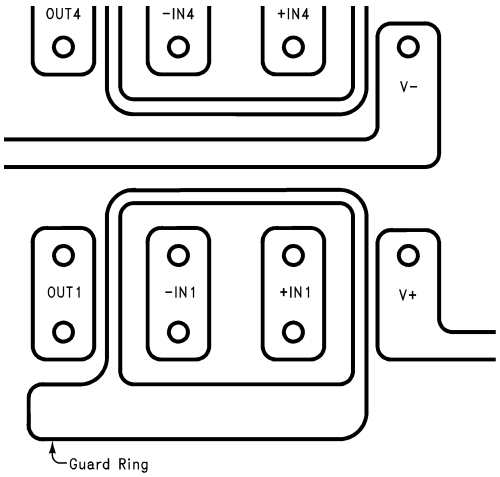


Figure 64. Example of Guard Ring in P.C. Board Layout

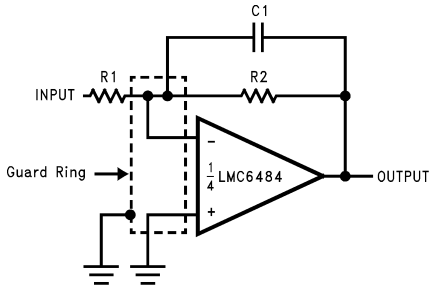


Figure 65. Inverting Amplifier

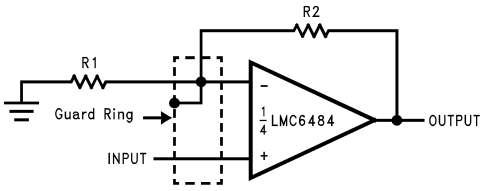
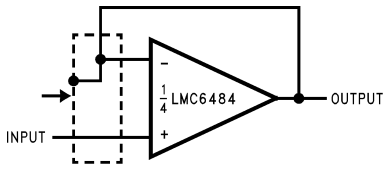


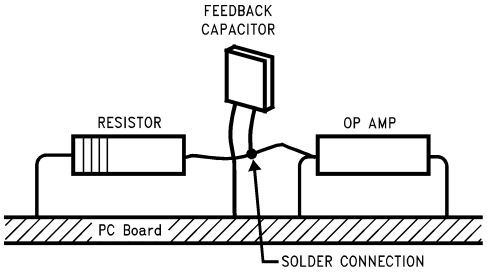
Figure 66. Non-Inverting Amplifier



Follower

Figure 67. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 68.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

Figure 68. Air Wiring

OFFSET VOLTAGE ADJUSTMENT

Offset voltage adjustment circuits are illustrated in Figure 70 Figure 71. Large value resistances and potentiometers are used to reduce power consumption while providing typically ±2.5 mV of adjustment range, referred to the input, for both configurations with V_S = ±5V.

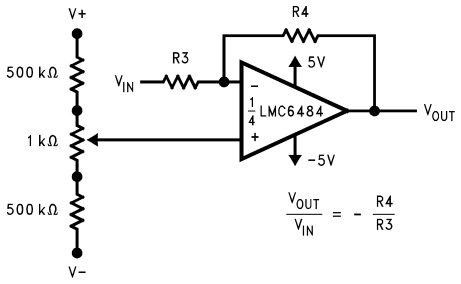


Figure 69. Inverting Configuration Offset Voltage Adjustment

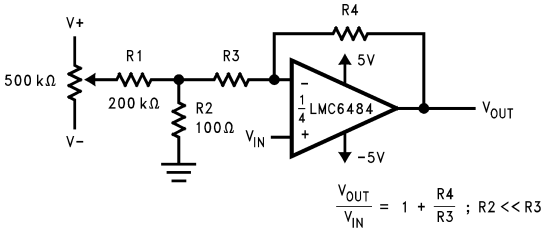


Figure 70. Non-Inverting Configuration Offset Voltage Adjustment

UPGRADING APPLICATIONS

The LMC6484 quads and LMC6482 duals have industry standard pin outs to retrofit existing applications. System performance can be greatly increased by the LMC6484's features. The key benefit of designing in the LMC6484 is increased linear signal range. Most op-amps have limited input common mode ranges. Signals that exceed this range generate a non-linear output response that persists long after the input signal returns to the common mode range.

Linear signal range is vital in applications such as filters where signal peaking can exceed input common mode ranges resulting in output phase inversion or severe distortion.

DATA ACQUISITION SYSTEMS

Low power, single supply data acquisition system solutions are provided by buffering the ADC12038 with the LMC6484 (Figure 71). Capable of using the full supply range, the LMC6484 does not require input signals to be scaled down to meet limited common mode voltage ranges. The LMC6484 CMRR of 82 dB maintains integral linearity of a 12-bit data acquisition system to ±0.325 LSB. Other rail-to-rail input amplifiers with only 50 dB of CMRR will degrade the accuracy of the data acquisition system to only 8 bits.

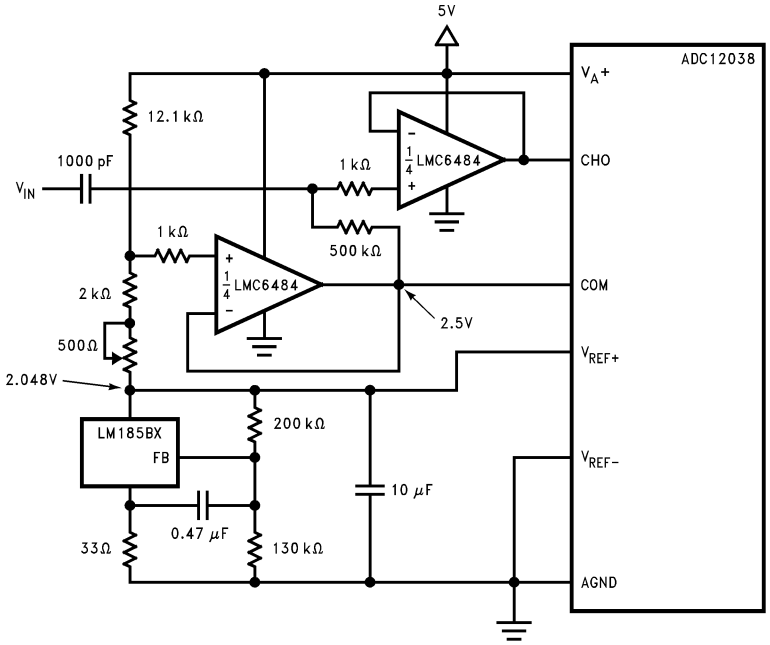


Figure 71. Operating from the same Supply Voltage, the LMC6484 buffers the ADC12038 maintaining excellent accuracy

INSTRUMENTATION CIRCUITS

The LMC6484 has the high input impedance, large common-mode range and high CMRR needed for designing instrumentation circuits. Instrumentation circuits designed with the LMC6484 can reject a larger range of common-mode signals than most in-amps. This makes instrumentation circuits designed with the LMC6484 an excellent choice for noisy or industrial environments. Other applications that benefit from these features include analytic medical instruments, magnetic field detectors, gas detectors, and silicon-based transducers.

A small valued potentiometer is used in series with Rg to set the differential gain of the 3 op-amp instrumentation circuit in Figure 72. This combination is used instead of one large valued potentiometer to increase gain trim accuracy and reduce error due to vibration.

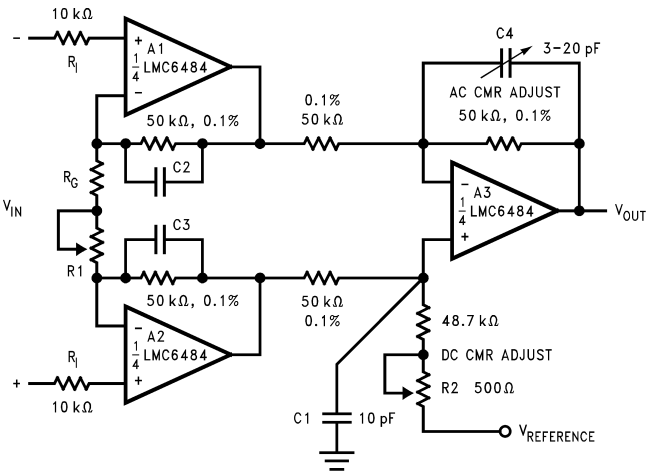


Figure 72. Low Power 3 Op-Amp Instrumentation Amplifier

A 2 op-amp instrumentation amplifier designed for a gain of 100 is shown in Figure 73. Low sensitivity trimming is made for offset voltage, CMRR and gain. Low cost and low power consumption are the main advantages of this two op-amp circuit.

Higher frequency and larger common-mode range applications are best facilitated by a three op-amp instrumentation amplifier.

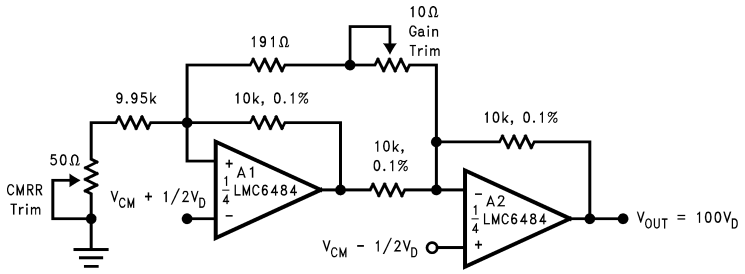


Figure 73. Low-Power Two-Op-Amp Instrumentation Amplifier

SPICE MACROMODEL

A spice macromodel is available for the LMC6484. This model includes accurate simulation of:

- input common-mode voltage range
- frequency and transient response
- GBW dependence on loading conditions
- quiescent and dynamic supply current
- output swing dependence on loading conditions

and many more characteristics as listed on the macromodel disk.

Contact your local Texas Instruments sales office to obtain an operational amplifier spice model library disk.

Typical Single-Supply Applications

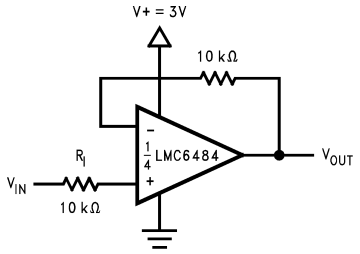


Figure 74. Half-Wave Rectifier with Input Current Protection (R_I)

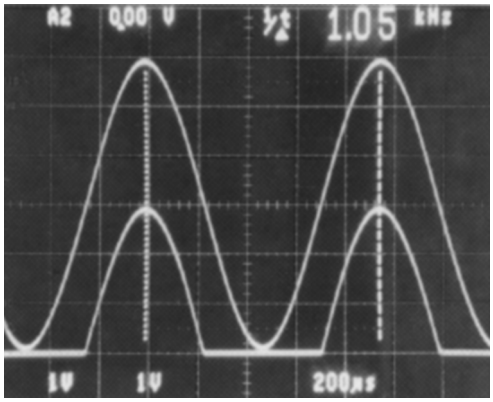


Figure 75. Half-Wave Rectifier Waveform

The circuit in Figure 74 use a single supply to half wave rectify a sinusoid centered about ground. R_I limits current into the amplifier caused by the input voltage exceeding the supply voltage. Full wave rectification is provided by the circuit in Figure 76.

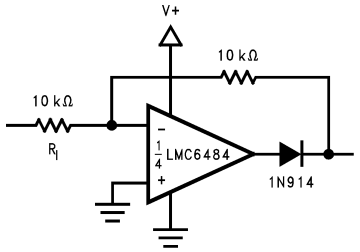


Figure 76. Full Wave Rectifier with Input Current Protection (R_I)

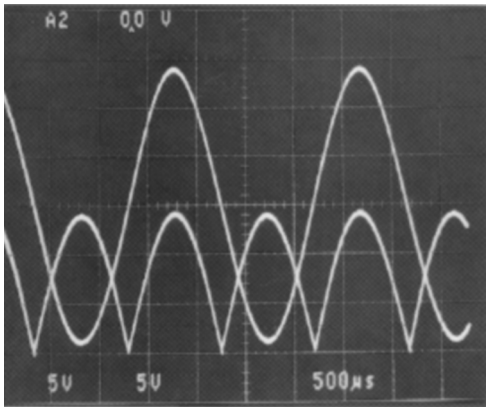


Figure 77. Full Wave Rectifier Waveform

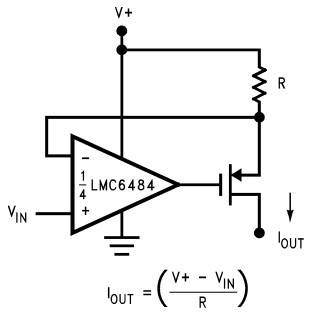


Figure 78. Large Compliance Range Current Source

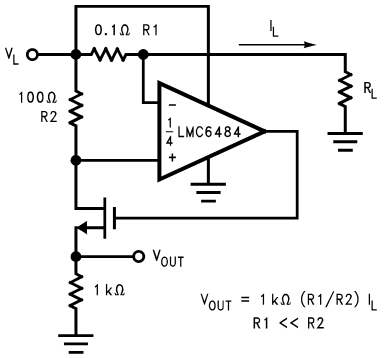


Figure 79. Positive Supply Current Sense

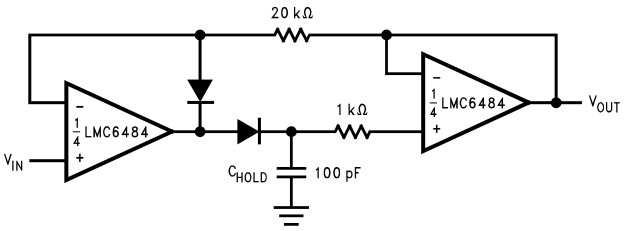


Figure 80. Low Voltage Peak Detector with Rail-to-Rail Peak Capture Range

In Figure 80 dielectric absorption and leakage is minimized by using a polystyrene or polyethylene hold capacitor. The droop rate is primarily determined by the value of C_H and diode leakage current. The ultra-low input current of the LMC6484 has a negligible effect on droop.

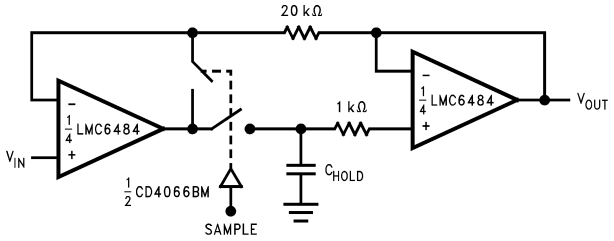
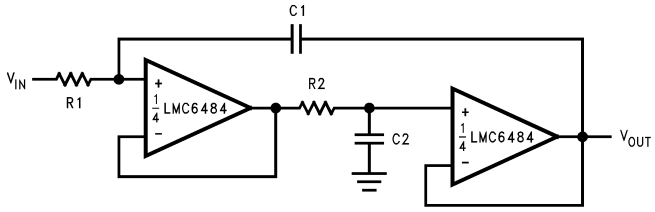


Figure 81. Rail-to-Rail Sample and Hold

The LMC6484's high CMRR (85 dB) allows excellent accuracy throughout the circuit's rail-to-rail dynamic capture range.



$$R1 = R2,\ C1 = C2;\ f = \frac{1}{2\pi R1C1};\ DF = \frac{1}{2}\sqrt{\frac{C_2}{C_1}}\sqrt{\frac{R_2}{R_1}}$$

Figure 82. Rail-to-Rail Single Supply Low Pass Filter

The low pass filter circuit in Figure 82 can be used as an anti-aliasing filter with the same voltage supply as the A/D converter.

Filter designs can also take advantage of the LMC6484 ultra-low input current. The ultra-low input current yields negligible offset error even when large value resistors are used. This in turn allows the use of smaller valued capacitors which take less board space and cost less.

Table 2. Revision History

Released	Revision	Section	Changes
10/26/2010	A	New Release, Corporate format	1 MDS data sheet converted into one Corp. data sheet format. The drift table was eliminated from the 883 section since it did not apply; MNLMC6484AM-X Rev 1A2 will be archived.
03/27/2013	A	All	Changed layout of National Data Sheet to TI format.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9453402MCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LMC6484AMJ/883 5962-9453402MCA Q	Samples
5962-9453402QXA	ACTIVE	CFP	NAC	14	42	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LMC6484AMWG /883 Q 5962-94534 02QXA ACO 02QXA >T	Samples
LMC6484AMJ/883	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LMC6484AMJ/883 5962-9453402MCA Q	Samples
LMC6484AMWG/883	ACTIVE	CFP	NAC	14	42	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LMC6484AMWG /883 Q 5962-94534 02QXA ACO 02QXA >T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

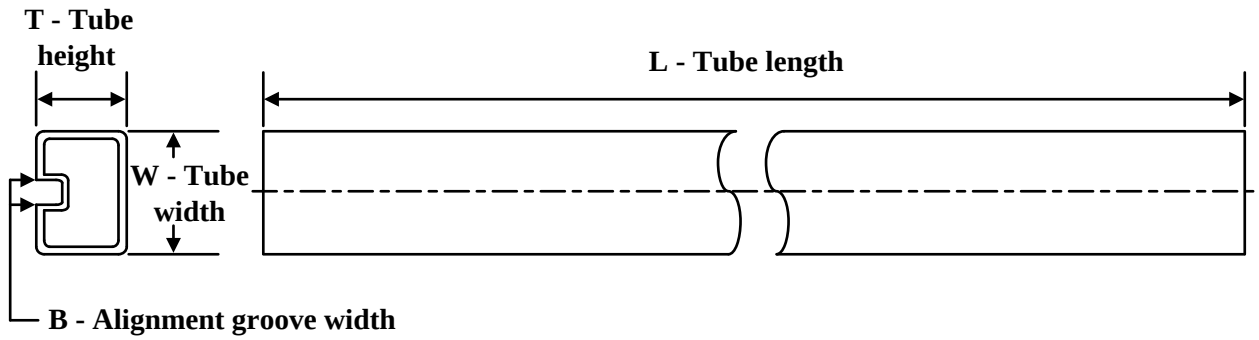
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

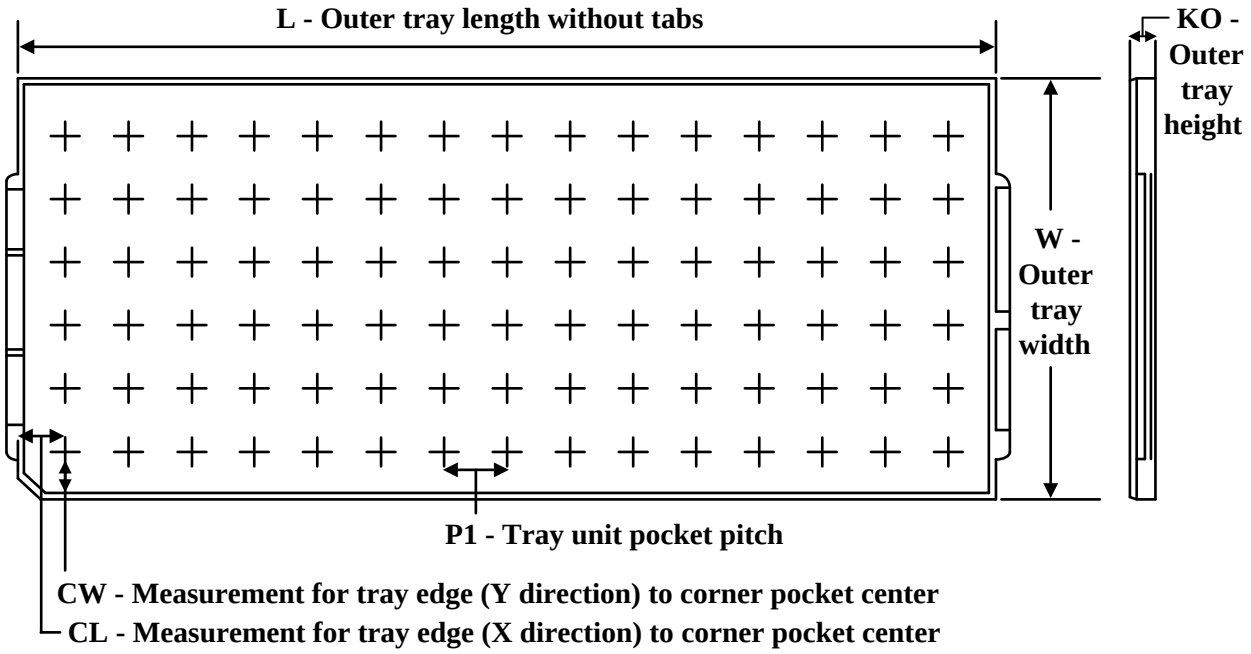
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9453402MCA	J	CDIP	14	25	506.98	15.24	13440	NA
5962-9453402MCA	J	CDIP	14	25	506.98	15.24	13440	NA
LMC6484AMJ/883	J	CDIP	14	25	506.98	15.24	13440	NA
LMC6484AMJ/883	J	CDIP	14	25	506.98	15.24	13440	NA

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

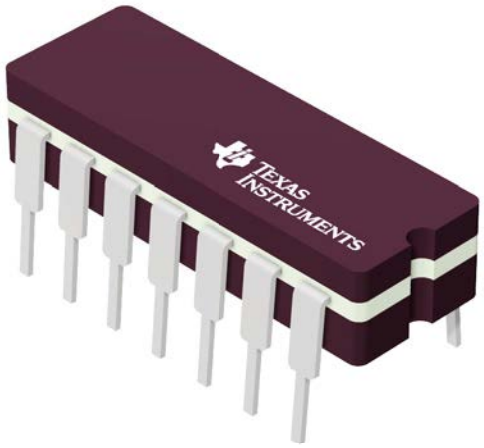
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
5962-9453402QXA	NAC	CFP	14	42	7 X 6	NA	101.6	101.6	8001	2.84	15.24	15.24
LMC6484AMWG/883	NAC	CFP	14	42	7 X 6	NA	101.6	101.6	8001	2.84	15.24	15.24

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

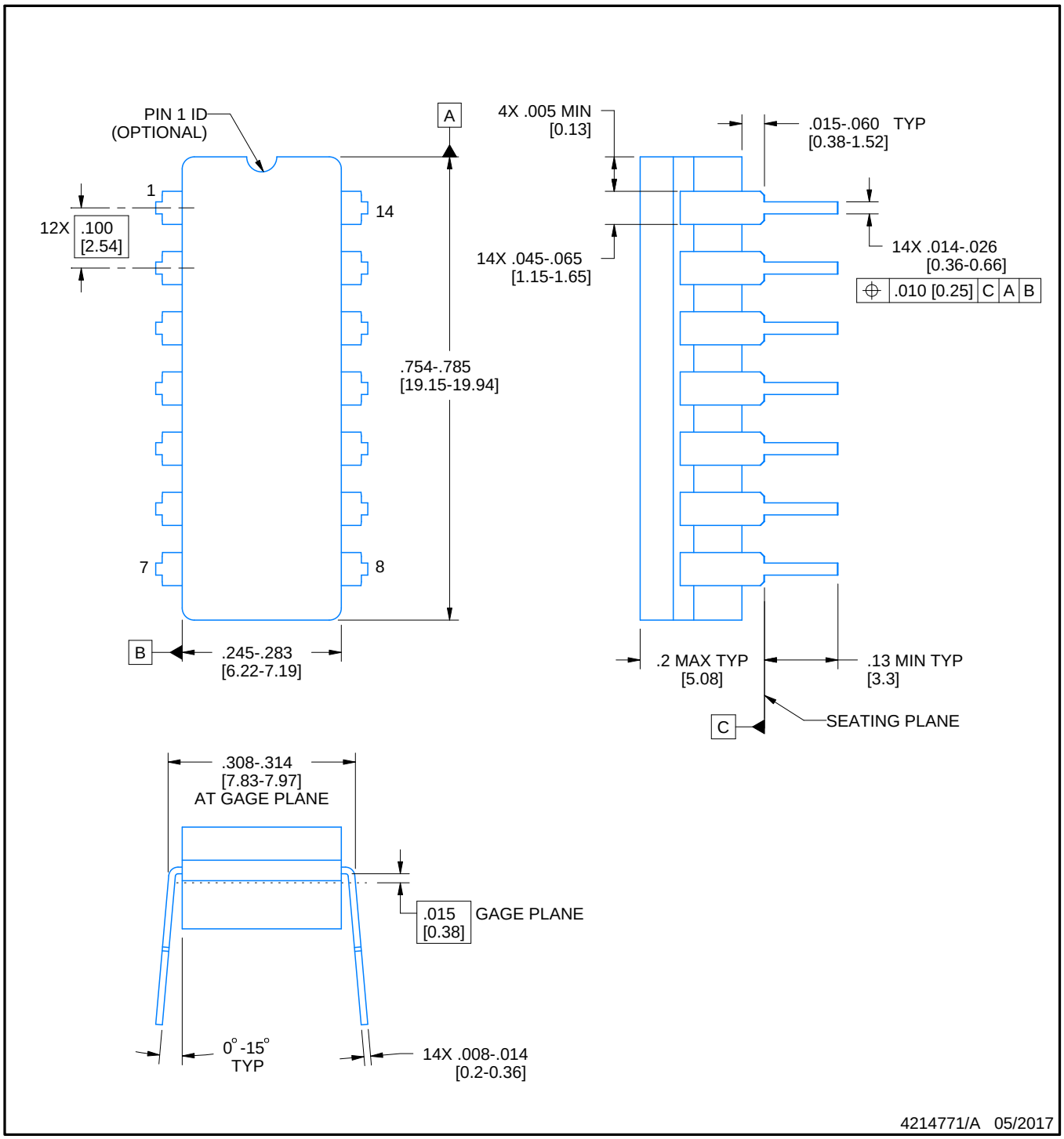
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

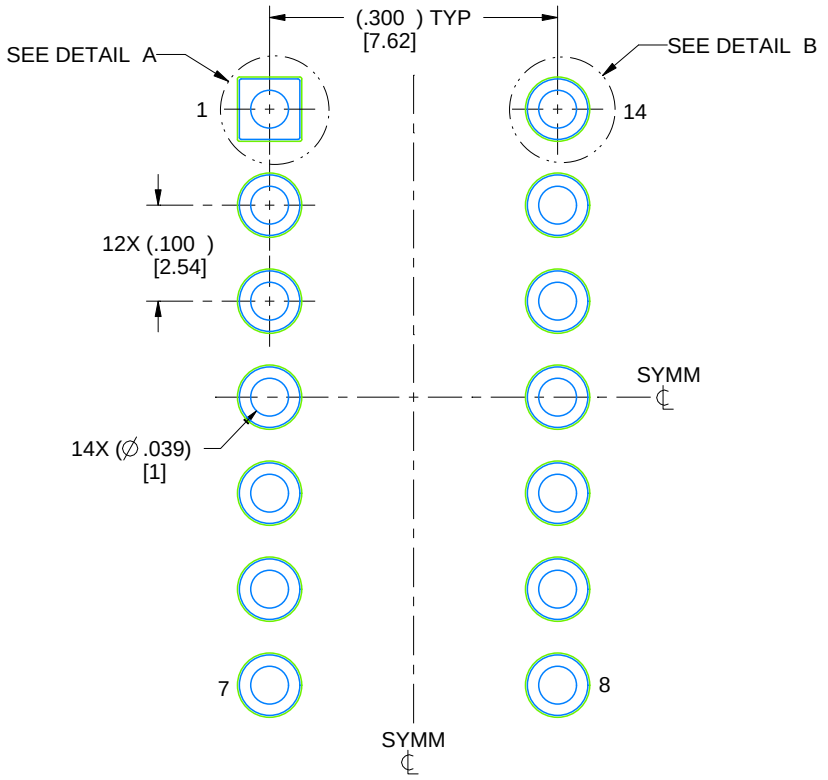
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

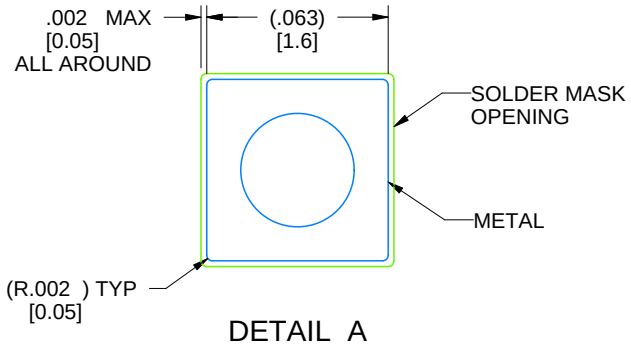
J0014A

CDIP - 5.08 mm max height

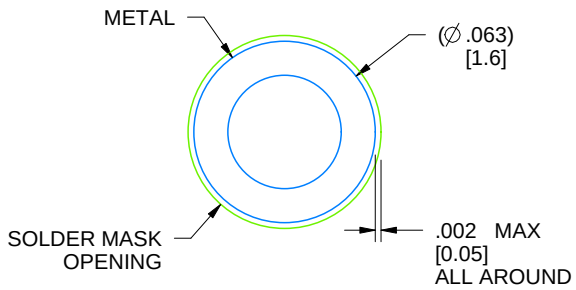
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

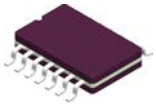


DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

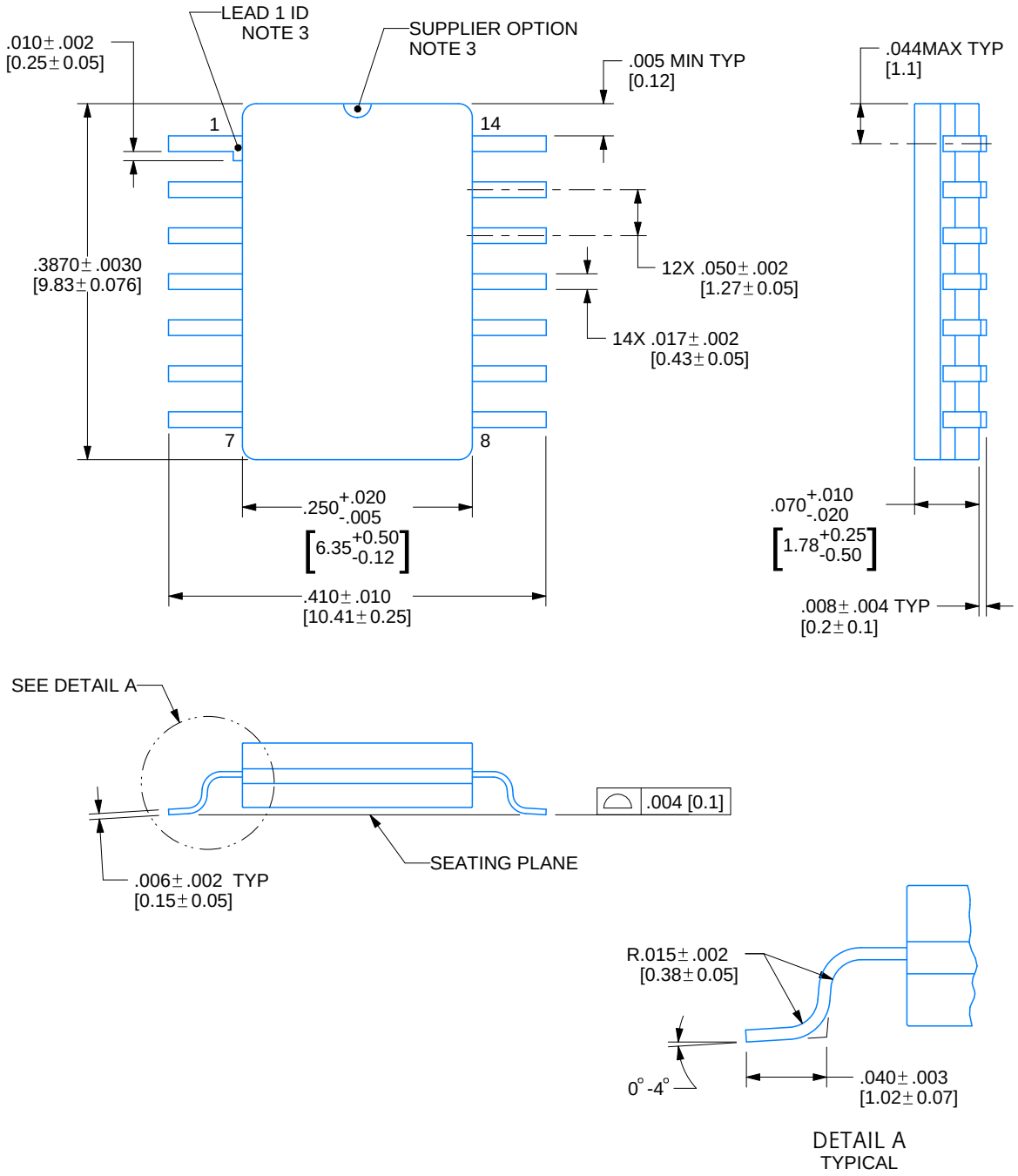


PACKAGE OUTLINE

NAC0014A

CERPACK

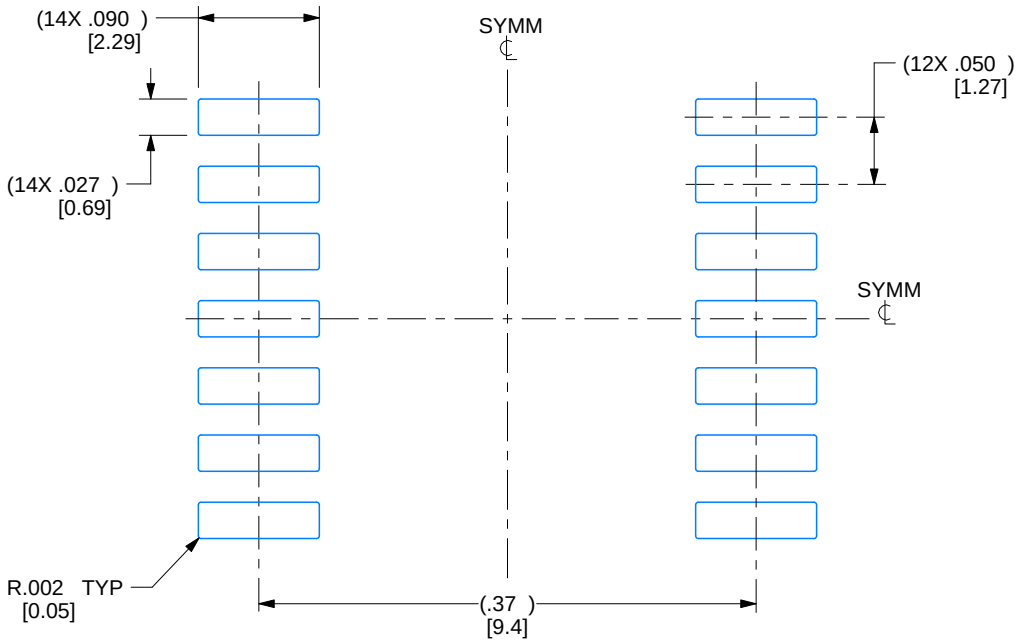
CERAMIC FLATPACK



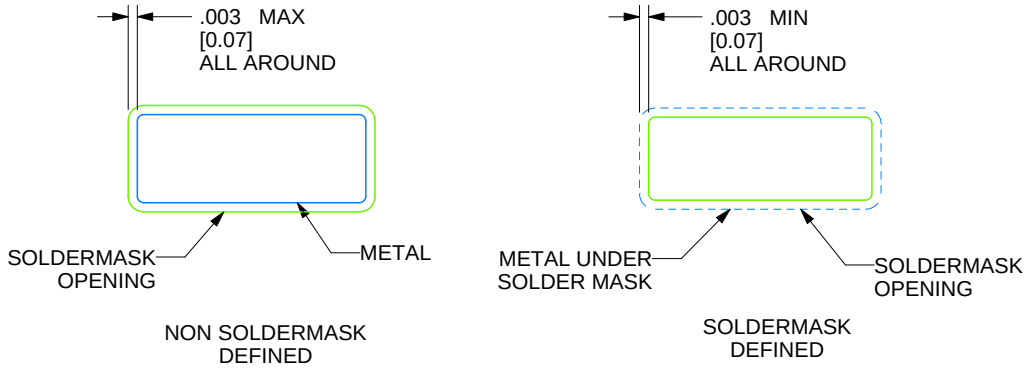
4215197/C 08/2022

NOTES:

1. Controlling dimension is Inch. Values in [ ] are milimeters. Dimensions in ( ) for reference only.
2. For solder thickness and composition, see the "Lead Finish Composition/Thickness" link in the packaging section of the Texas Instruments website
3. Lead 1 identification shall be:
   a) A notch or other mark within this area
   b) A tab on lead 1, either side
4. No JEDEC registration as of December 2021



RECOMMENDED LAND PATTERN



4215197/C 08/2022

REVISIONS

REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	2197878	12/30/2021	DAVID CHIN / ANIS FAUZI
B	NO CHANGE TO DRAWING; REVISION FOR YODA RELEASE;	2198833	02/15/2022	K. SINCERBOX
C	.3870± .0030 WAS .39000± .00012;	2200916	08/08/2022	D. CHIN / K. SINCERBOX

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