Application Report
SLUA931–October 2019

Get the Most Power from a Half-Bridge with High-Frequency Controllable Precision Dead Time

Jeff Mueller, High Power Drivers

ABSTRACT

To prevent the high-side and low-side FETs from turning on simultaneously, dead time is employed between each switching transition when both FETs are turned off. An improper dead time can create shoot-through and short the supply to ground, which can heat up the FETs and decrease efficiency. The fastest GaN Half-Bridge design must have controllable dead time to keep the efficiency high. Increasing the switching frequency helps reduce the solution size, but increases the overall amount of time spent with both FETs turned off if the dead time does not decrease as a percentage of the switching frequency. The gate driver, the closest point of contact to the FET, must be the controller of dead time. This application note explores how the precise dead-time control circuit of the LMG1210 can help minimize dead-time loss and protect the high-side FET in a half-bridge design.

Contents

List of Figures

List of Tables

Trademarks

1 Importance of Dead Time in a Half-Bridge

Dead-time loss consists of three sources: source to drain reverse conduction loss, output capacitance loss, and reverse recovery charge loss. Reverse conduction loss is the main focus for this discussion since GaN has zero Q_{rr} and much lower Q_{coss} when compared to a MOSFET with equal R_{DSON}. During dead time, current conduction happens in the low-side of a half-bridge when the gate is off. This is known as third-quadrant conduction, and is found in Figure 1. GaN FETs do not have the body diode of an

intrinsic MOSFET to clamp the source to drain voltage, and can turn on in reverse. When the drain potential is below the gate from the larger source to drain the voltage drop, the GaN turns on in reverse. The third-quadrant conduction loss of the GaN is higher than the MOSFET due to this. For further details of GaN third-quadrant conduction, see section 2 of *Does GaN Have a Body Diode? - Understanding the Third Quadrant Operation of GaN*. Dead-time conduction loss is directly proportional to:

- Frequency
- Load current
- Voltage drop
- Dead time duration

Reducing any of these helps minimize dead-time loss.

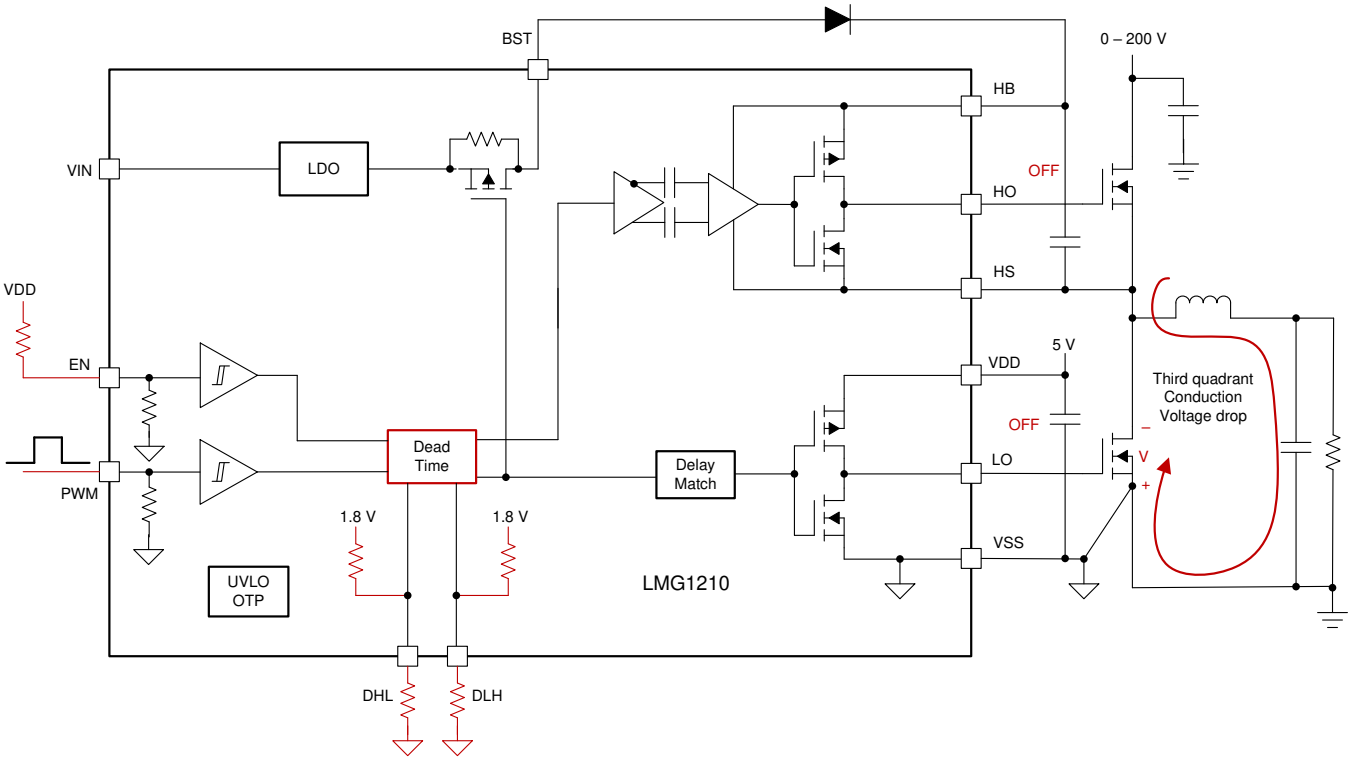

Figure 1. DHL/DLH Pin and Dead-time Conduction Enabled in PWM Mode

2 How to Activate DHL and DLH for Dead Time in PWM Mode

In PWM mode, the LMG1210 has the ability to create a 0.8 ns–20 ns dead time. In PWM mode, the PWM pin is used to switch both outputs with a dead time defined by the DHL and DLH pins. To activate PWM mode, resistors must be placed at both DHL and DLH pins and tied to V_{SS}. The resistor values placed at the DHL and DLH pins set the dead time for high-to-low and low-to-high switching transitions, respectively. Figure 1 shows the LMG1210 enabled in PWM mode with DHL/DLH resistors tied to ground for a fixed dead-time. To control the LMG1210 with an adjustable dead time, replace these resistors with a potentiometer or drive the pins directly with a DAC. In PWM mode, the EN or enable pin is pulled high to enable the output. The PWM pin controls both low-side and high-side outputs, which reduces the number of traces and drive complexity from the controller.

Operating Mode	DHL	DLH
PWM Mode		
Independent Input Mode (IIM)	Leave Floating or Tie to VSS	

Figure 2. DHL and DLH Pin Operating Mode

NOTE: In PWM Mode, the HI and LI pins are referred to as EN and PWM respectively where the EN pin is used to enable the outputs. In IIM, when leaving the controller to take care of the dead time, use the separate HI and LI pins to control the HO and LO outputs directly. To unlock IIM, tie DLH to VDD and DHL to VSS, or leave floating as found in Figure 2. Since the dead-time circuit of the LMG1210 is no longer active in IIM, interlock or external dead-time circuits can be implemented to prevent shoot-through.

3 How to Use DHL and DLH in PWM Mode

For a desired dead time (t_{dt}), the corresponding required DHL and DLH pin resistance can be calculated in Equation 1 with t_{dt} in ns and R_{ext} in kΩ. The maximum dead time is 20 ns, which gives a minimum resistor value of 20 kΩ. The minimum dead time is 0.5 ns, which gives a maximum resistor value of 1.8 MΩ.

$$R_{ext} = (900/t_{dt}) - 25 \quad (1)$$

The internal pullup resistors at the DHL and DLH pins form a voltage divider with R_{ext} referenced to 1.8 V. After being filtered by an internal 10 kHz low-pass-filter, the voltage on V_{DHL} and V_{DLH} sets the dead-time. The calculation between the dead-time t_{DT} in ns and the voltage on V_{DHL} and V_{DLH} is found in Equation 1. Figure 5 illustrates this relationship in which the voltage on the DHL and DLH pins versus dead time is linear.

$$t_{dt} = (1.8\text{-}V_{DT}) \times 20 \quad (2)$$

Combining Equation 1 and Equation 2 reveal that the relationship of the DHL and DLH dead-time resistor values get larger for a smaller dead time or DHL and DLH pin voltage, as shown in Figure 3. The dead-time resistor equation is a factor of $1/R_{ext}$, so the higher the resistor value, the smaller the distance between each dead-time value. This results in more granularity at shorter dead times, where it is needed most.

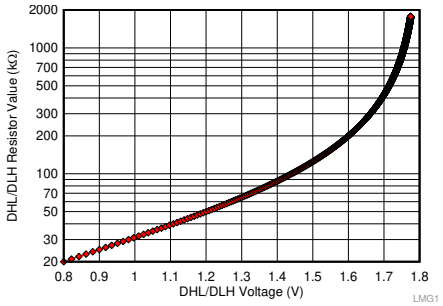

Figure 3. DHL and DLH Pin Voltage Versus Resistor Value

4 Using a DAC for Setting the Dead Time

To achieve an optimal efficiency for different output loads, driving the DHL and DLH pins with a DAC to control the dead time in real time can be done. Typically, the switch node or gate signal can be fed back to the microcontroller to determine when third-quadrant conduction occurs to achieve a minimal dead time. In PWM mode, the LMG1210 can have a fixed dead time or can change dead time without having to power cycle the part. This allows a DC voltage from a DAC to be directly applied to the DHL and DLH pins to easily fine tune the dead time for a better efficiency. If driving the voltage on the DHL and DLH pins from a DAC, the LMG1210 dead time responds like a 10 kHz first-order R-C low-pass filter. Within 100 µs, the dead time settles to the new value. The internal 10-kHz filter allows for sufficient rejection, however if more noise rejection or a lower cutoff frequency is required, then an external filter can be added. If using a external R-C filter as shown in Figure 4, the DAC needs to compensate the correct voltage since the circuit causes the voltage on the DHL and DLH pin to be above the commanded voltage due to the 1.8-V reference voltage. Therefore, an external filter mus be an active one with low output impedance, since the DC signal source has to appropriately drive the DHL and DLH pins. The internal 20-kΩ series resistor is 1% precision trimmed, and if the external resistor is also 1% trimmed, then the transfer function for the DHL and DLH pin drive voltage versus the DAC drive voltage is well known.

In Figure 4, the internal pullup resistor $R_{internal}$ and external pullup resistor $R_{external}$ form a voltage divider referenced to 1.8 V and the DAC voltage respectively. The equation for the voltage on the DLH pin according to the applied DAC voltage can be found in Equation 3. For example, to achieve 12-ns dead time with 1.2 V on the DLH pin, drive the DAC with 0.6 V to produce the correct 1.2 V on the DLH pin and therefore the correct dead time.

$$V_{DAC} = V_{DHL} + (V_{DHL} - 1.8) (R_{external} / R_{internal}) \quad (3)$$

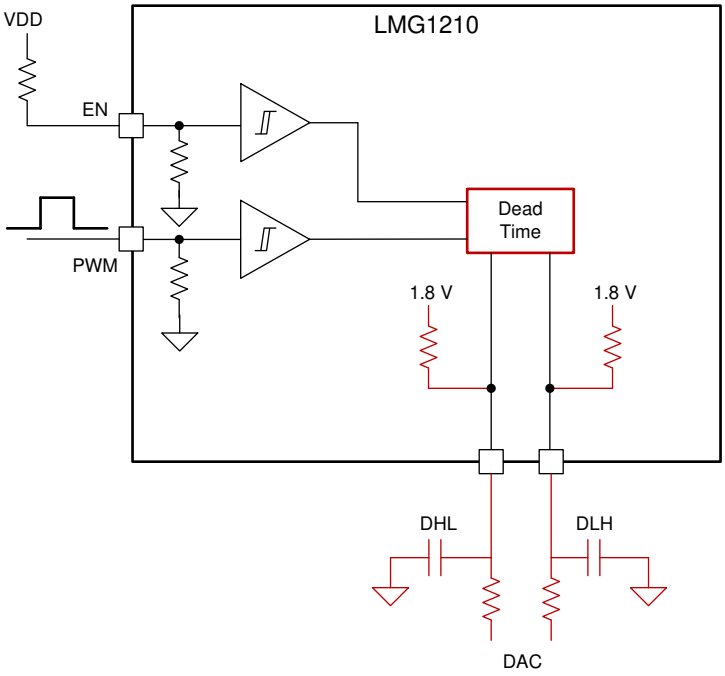

Figure 4. LMG1210 Driving DAC on DHL Pin

5 Preventing Dead-time Variation

The LMG1210 can achieve a short and precise dead time from 0.8 ns to 20 ns for each individual PWM pin switching edge with DHL and DLH pins. The accuracy of the LMG1210 dead time allows the driver to predictably turn on to prevent further dead-time conduction loss. The precision of the dead time depends on propagation delay and delay mismatch variation. The resistor value over temperature can also contribute to small variations in dead time, so the resistor temperature coefficient must be low to allow a constant value across temperature. CMTI and bootstrap voltage can also vary the propagation delay; the maximum variance only adds 300 ps for a 4-V bootstrap voltage and 200 ps during a 100 V/ns CMTI event. The typical propagation delay for the LMG1210 in PWM mode is 11 ns and increases to 13 ns

across temperature, as depicted in Figure 7 of the *LMG1210 200-V, 1.5-A, 3-A Half-Bridge GaN Driver with Adjustable Dead Time* Data Sheet (SNOSD12). The propagation delay can also vary from part to part, and can be approximated by the LMG1210 data sheet spec difference of $t_{PHL/PLH}$ max and typical, which is 8 ns. For further information on the dead time of the LMG1210, see the *Dead Time Optimization LMG1210 GaN Driver* Application Note.

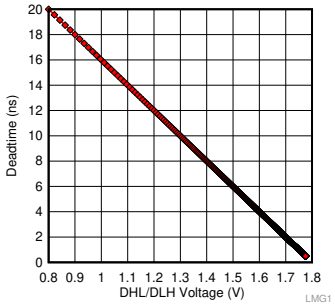

Figure 5. DHL and DLH Pin Voltage Versus Dead Time

6 Bootstrap Charging Circuit

During dead time, the switch-node can become most negative and overcharge the bootstrap. The LMG1210 uses a unique bootstrap charging mechanism that prevents overcharging the bootstrap to protect the high-side FET. In PWM mode, the charging mechanism allows the bootstrap to conduct only after the low-side turns on and not during dead time. The BST switch, which is part of the bootstrap mechanism, typically turns on 8–10 ns after LO turns on and turns off 2–3 ns after the gate driver starts pulling down the GaN gate. The BST switch is off before the low-side GaN shuts off, which prevents the LO dead time from affecting the bootstrap charging voltage. During start-up, HB gets charged through the 1 kΩ with a time constant of about R * C, with R equal to 1 kΩ and C is the bootstrap cap. However, HB does not completely charge because of the high-side quiescent current. The 500-uA quiescent current of the high-side drops about 0.5 V across the 1-kΩ resistor, so it can only charge to about 4.5 V through the 1-kΩ resistor. So in some applications, with very negative HS voltages, there can still be bootstrap diode conduction and bootstrap capacitor over-charging, even with the BST switch off. The BST switch only allows bootstrap conduction during LO on time, although it is possible that, during dead time, excessive negative HS voltage below -6 V can cause the ESD diode to conduct and overcharge the bootstrap capacitor.

7 Synchronous Bootstrap Charging Circuit

The BST switch takes up to 10 ns to turn on, which then determines the maximum switching frequency with a 50% duty cycle as limited to 50 MHz. To reach a 50-MHz switching frequency requires a synchronous bootstrap using a GaN FET, as found in Figure 6. The synchronous bootstrap operates when LO goes high and the gate of the GaN FET is charged through a 20-Ω resistor. The 22-nF capacitor is already charged to 5 V, so the gate goes 5 V above this. When LO turns off, the diode quickly discharges the gate back to LO to make sure the bootstrap switch is off before LO dead time. It is important that the HB-HS voltage does not overcharge due to negative HS voltage or the GaN FET being on during dead-times. All the Rs and Cs must be tuned to not turn on the GaN FET or bootstrap switch too quickly. However, turn it off as quick as possible to prevent bootstrap charging during LO dead time, which may potentially overcharge the HB-HS voltage.

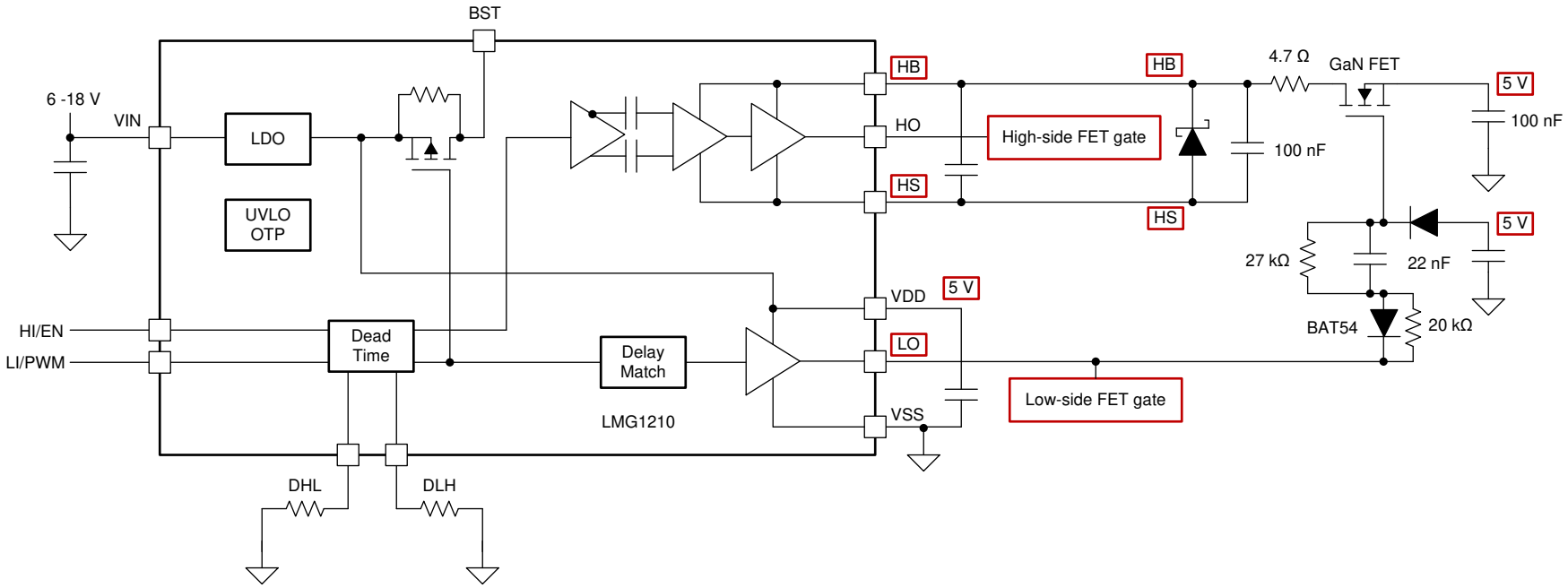

Figure 6. Synchronous Bootstrap Using GaN FET LMG1210 Diagram

8 Summary

In PWM mode, the LMG1210 can control a fixed or adjustable dead time with the DHL and DLH pins. GaN has a larger third-quadrant conduction voltage drop during dead time compared to MOSFETs. A shorter dead time using the LMG1210 and a smaller drain to source voltage drop using a Schottky diode can help reduce dead-time conduction loss. Equation 1 helps calculate the required DHL and DLH resistor value for a given dead time and Equation 2 helps calculate the required DHL and DLH voltage for a given dead-time. The LMG1210 can also protect the high-side FET using a unique bootstrap charging mechanism that is resistant to the negative switch-node voltage that develops during dead time and overcharges the bootstrap. The fastest GaN Half-Bridge design must have controllable dead time in the gate driver to maximize efficiency. The controllable precision dead-time of the LMG1210 can help achieve minimal dead-time conduction loss, as well as protect the high-side FET gate with a unique bootstrap charging mechanism.

9 Related Documentation

- Texas Instruments, *LMG1210 200-V Half-Bridge MOSFET and GaN FET Driver Data Sheet*
- Texas Instruments, *Using the LMG1210EVM-012 User's Guide*
- Texas Instruments, *Design Considerations for LMG1205 GaN FET Driver for High-Frequency Operation Application Report*
- Texas Instruments, *Dead Time Optimization LMG1210 GaN Driver Application Report*
- Texas Instruments, *Achieve Cooler Thermals and Less Power Loss of Your GaN Half-Bridge Design with the LMG1210 Application Report*
- Texas Instruments, *Does GaN Have a Body Diode? - Understanding the Third Quadrant Operation of GaN Application Report*

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265