Direct-drive configuration for GaN devices

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The benefits of direct drive for GaN devices are achieving higher switching power efficiencies and better system level reliability due to the integration of device protections.

The switching characteristics of high-voltage (600-V) gallium nitride (GaN) high-electron-mobility transistors (HEMTs) enable new topologies that increase switched-mode power supply efficiency and density. GaN has low terminal capacitances (Ciss, Coss, Crss) and no third-quadrant reverse recovery. These characteristics enable higher-frequency hard-switched topologies such as totem-pole bridgeless power factor controllers (PFCs) that cannot be realized by MOSFETs and insulated-gate bipolar transistors (IGBTs) due to their high switching losses. In this paper, we will highlight the benefits offered by directly driving a GaN transistor, including lower switching losses, better slew-rate control and improved device protections.

Introduction

When designing switched-mode power supplies, the main figures of merit (FOM) are cost, size and efficiency. [1] These three FOMs are coupled and require that many factors be taken into consideration. For example, increasing switching frequency can reduce the size and cost of the magnetics, but will increase losses in the magnetics and switching losses in the power devices. Because GaN has low terminal capacitances and no diode reverse recovery, GaN HEMTs have the potential to significantly lower losses compared to MOSFETs and IGBTs.

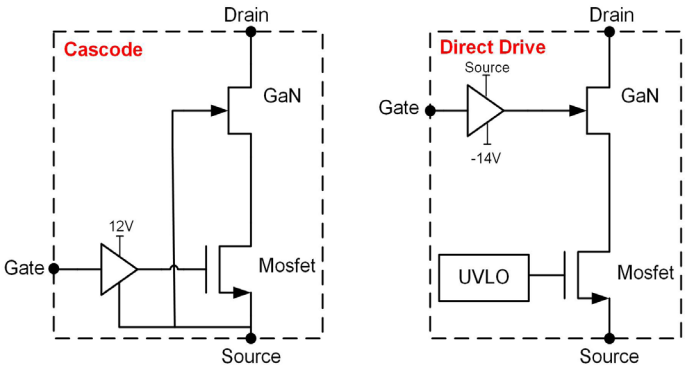

Figure 1: *Cascode drive and direct-drive configurations.*

Normally, MOSFET/IGBT drivers provide suitable turn-on and turn-off current to support the input capacitance. External resistors between the driver output and device gate control the slew rate and dampen power and gate-loop ringing. With GaN's increased slew rate, external components add too much parasitic inductance to control the switching. Integrating the driver into the package with the GaN device minimizes parasitic inductances, lowers switching losses and optimizes drive control.

Direct drive advantages

The presence of a native two-dimensional electron gas (2-DEG) layer in GaN between the source and drain makes the device conduct at a zero gate-source voltage. For safety reasons, power devices used in switched-mode power supplies must be turned off to disconnect the input from the output when bias power is not available. To emulate an enhancement-mode device, a low-voltage MOSFET is placed in series with the GaN source. **Figure 1** shows two distinct configurations to achieve this: cascode drive and direct drive.

Now we will compare and contrast the power losses and describe the concerns related to the caveats associated with each approach.

In the cascode configuration, the GaN gate is grounded and the MOSFET gate is being driven to control a GaN device. Because MOSFETs are silicon devices, many gate drivers are readily available. However, this configuration exhibits higher combined Coss since the GaN gate-to-source capacitance (Cgs) and the MOSFET Coss must be charged to the GaN threshold voltage before the GaN device turns off.

In a direct-drive configuration, the MOSFET is on and the GaN gate, which is being driven by a gate driver between ground and a negative voltage (VNEG), turns on/off the combined device. Additionally, the MOSFET Coss does not need to be charged. The current to turn off the GaN Cgs comes from a lower voltage bias supply. Lower supply voltages deliver the same GaN gate-to-source charge (Qgs) that results in lower power dissipations. These power-efficiency differences are magnified even more at higher switching frequencies.

Reverse-recovery Qrr losses come into play for the cascode configuration. This is because in the third-quadrant conduction, the MOSFET is off and conducting through the body diode. There are stored charges in the MOSFET due to load current flowing in the reverse direction. The current to overcome the reverse-recovery charge comes from a high-voltage supply, resulting in substantial losses. However, in a direct-drive configuration, the MOSFET is always on and its parasitic diodes do not turn on due to its low R_{DSON}. As a result, there are no Qrr-related power losses in a direct-drive configuration.

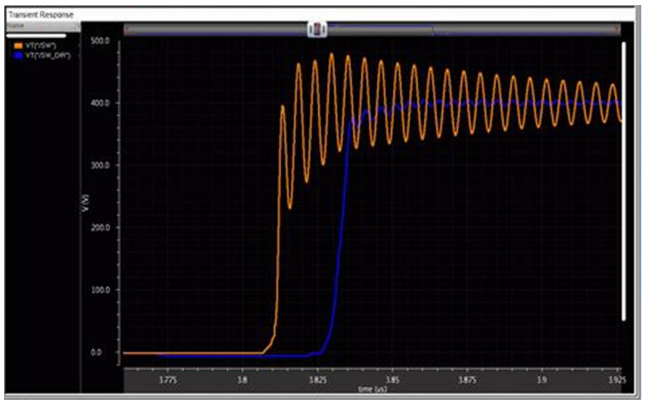

Figure 2: *Excessive ringing due to a hard-switched operation.*

In a cascode configuration, the voltage distribution between the GaN and MOSFET in off-mode can cause the MOSFET to avalanche due to high GaN drain-to-source capacitance (Cds) [2, 3]. One solution could be to add a capacitor in parallel with the MOSFET's drain and source [4]. However, this only works for soft-switched applications and causes high power losses in hard-switched applications.

Given that the GaN gate is connected to the MOSFET's source, the switching slew rate in cascode drive cannot be controlled. In a hard-switched operation, the increased effective Coss from the GaN Cgs, MOSFET Coss, MOSFET Qrr, and possibly some current conduction due to MOSFET avalanche prevention, can cause higher drain currents during initial charging. This higher drain currents can result in higher power losses in cascode drive.

After the drain of the MOSFET charges high enough to turn the GaN device off, the sudden drop in Coss seen from the drain – combined with the higher drain currents flowing through the power-loop inductance – causes excessive ringing of the switch node in a cascode configuration. A switching waveform during a hard-switching event is shown in **Figure 2** (orange trace = cascode drive; blue trace = direct drive). In this simulation, a direct-drive configuration dissipates less energy per each hard-switching event, even though its slew rate is lower and rings less (4.2 W at 50 V/ns for direct drive

versus 4.6 W at 150 V/ns for cascode drive, all with 5-A load current).

On the other hand, the direct-drive configuration drives the gate of the GaN device directly during the switching operation. When the bias supply is not present, the MOSFET gate is pulled to ground and turns off the GaN device in the same manner as a cascode configuration. Once the bias supplies are

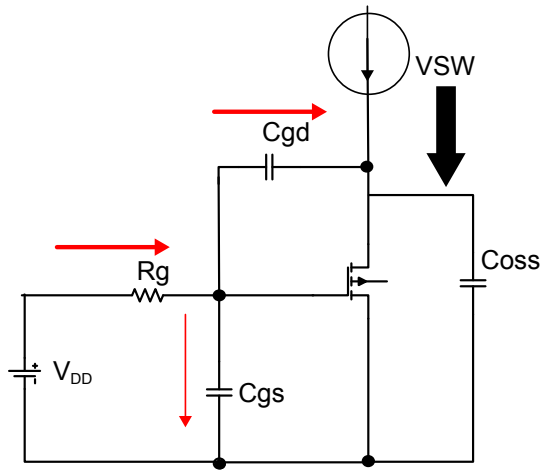

Figure 3: *Model of the drive path for a direct-drive configuration.*

$$\frac{dV}{dt} \sim \frac{V_{DD} - Vt}{\frac{C_{OSS}}{g_m} + R_g C_{gd}} \quad \textbf{(1)}$$

present, the MOSFET remains turned on and its parasitic capacitance and body diode are removed from the circuit. The advantage of driving the GaN gate directly is that you can control the slew rate by setting the current that charges the GaN gate.

For a boost converter, a simple model for the driver circuit is shown in **Figure 3.** Equation [1] can be derived using this model.

Equation 1 demonstrates that when the GaN device has enough gate-to-drain capacitance (Cgd), the slew rate of the switching event can be controlled by the Miller feedback by using the gate current. For low Cgd devices, the feedback is lost and the transconductance (gm) of the device controls the slew rate.

Another advantage of a direct-drive configuration is that you can add impedance to the gate loop to dampen its parasitic resonances. Dampening the gate loop also reduces ringing in the power loop. This lowers the voltage stress on the GaN device and reduces electromagnetic interference (EMI) concerns during hard switching.

Figure 2 is a simulation showing the difference in switch-node ringing in a buck converter modeled with power- and gate-loop parasitic inductances. The direct-drive configuration has a controlled turn-on with very little overshoot. Whereas a cascode drive has significantly higher ringing and hard-switching losses due to higher initial Coss, Qrr and lower impedance in the gate loop.

75-mΩ GaN device with an integrated gate drive

TI's LMG341x family of 600-V GaN devices is the industry's first to integrate a GaN FET plus driver and protection features. It is an 8-mm-by-8-mm quad flat no-lead (QFN) multichip module (MCM) comprising a GaN FET and driver with an integrated 20-V series FET. The total R_{DSON} is 75 mΩ.

Figure 4 is a block diagram of this device. The gate driver provides direct-driving capability of the GaN FET and has a built-in buck-boost converter to generate the negative voltage needed to turn-off the GaN FET. The gate driver runs off of a single 12-V supply and has an internal low-dropout regulator (LDO) to generate a 5-V rail that powers the driver and other control circuits. An internal undervoltage lockout (UVLO) circuit keeps the safety FET turned off until the input voltage goes above 9.5 V. Once the UVLO crosses its own threshold, the buck-boost converter turns on and charges the negative rail (VNEG). The driver is enabled once the VNEG supply voltage crosses its own UVLO.

The LMG341x family's integrated direct-drive implementation has many advantages over a discrete GaN and driver. An essential aspect of the gate driver is controlling the slew rate during hard-switching events. The LMG341x family uses a programmable

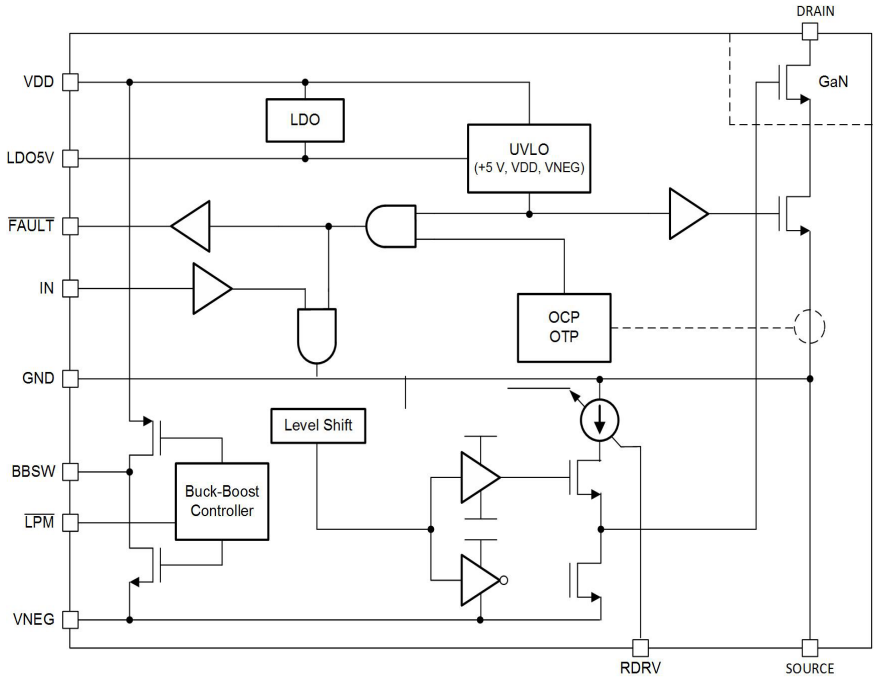

Figure 4: *Block diagram of a single-channel 600 V, 76-Ω GaN FET power stage.*

current source to drive the GaN gate. The current source provides impedance to dampen the gate loop and allows the user to program the slew rate in a controlled fashion from 30 V/ns to 100 V/ns for board-parasitic and EMI concerns.

By integrating the series FET into the driver's integrated circuit (IC), a sense FET and current-sensing circuit provide overcurrent protection to the GaN FET. This is a key feature that enhances the overall system reliability. This kind of current-sense scheme is not possible when using enhancement-mode GaN devices. The current-protection circuit trips when currents greater than 40 A flow through the GaN FET. The GaN FET is turned off within 60 ns of an overcurrent event, preventing the die from overheating.

By packaging the driver die on the same die-attach-pad (DAP) as the GaN FET, the lead frame at the driver die can sense the temperature of the GaN device. The driver can protect the device by disabling the GaN drive during an overtemperature event. The integrated GaN device also provides a FAULT output to inform the controller that switching has stopped due to a fault event.

To verify operation using the direct-drive approach, we built a half-bridge board and configured it as a buck converter **(Figure 5)**. Further, we used the ISO7831 bidirectional level-shifter to feed the high-side drive signals and get back the level-shifted FAULT signal.

In **Figure 6**, the GaN half-bridge configuration is switching at 1.5 A from a 480-V bus with a slew rate of 100 V/ns. The blue trace is the switch-node waveform

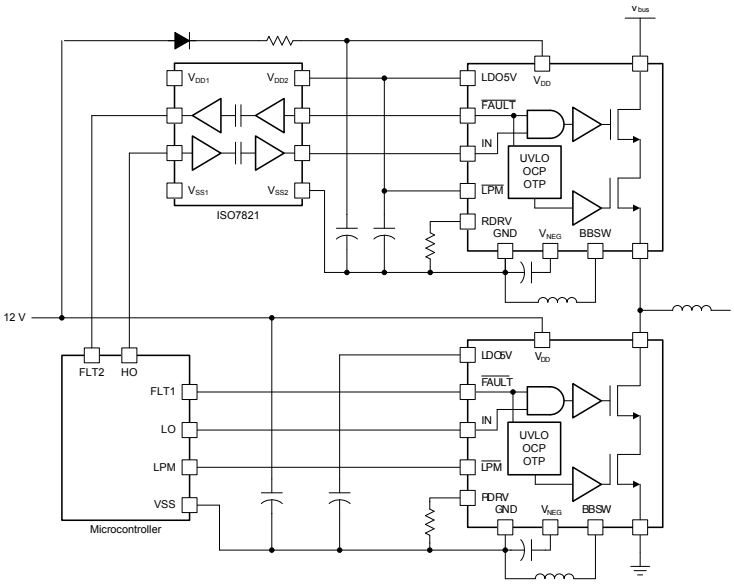

Figure 5: *Typical half-bridge configuration.*

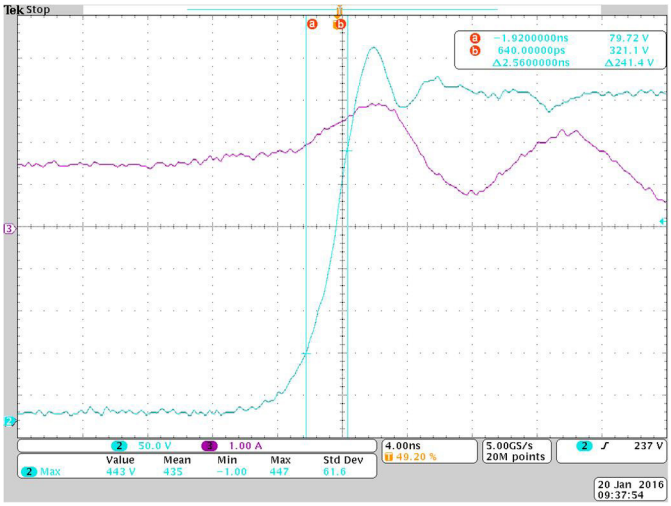

Figure 6: *Example of buck-switching waveforms.*

and the purple trace is the inductor current. The hard-switched turn on is clean and has an overshoot of ~50 V. This waveform was taken using a 1 GHz scope and probe to see any high-frequency ringing. The fast turn-on times, coupled with reduced terminal capacitances and a lack of reverse-recovery charge, enable the GaN-based half-bridge configuration to switch at high efficiencies, even as a hard-switched converter.

Summary

The benefits that GaN offers in terms of reduced terminal capacitances and no reverse recovery open up the possibility of using hard-switched topologies while maintaining high efficiencies. Maximizing the benefits that GaN provides require controlled high-switching slew rates, which in turn demand an optimized co-packaged driver and careful board-layout techniques. Co-packaging the driver helps minimize gate-loop parasitics to reduce gate ringing.

With a carefully laid-out printed circuit board (PCB), an optimized driver allows a designer to control the slew-rate of the switching event with minimal ringing and EMI. This is enabled by the direct-drive configuration of the GaN device rather than the cascode-drive configuration.

The LMG341x family of devices gives designers the ability to control the switching of various devices at slew rates from 30 V/ns to 100 V/ns. Additionally, the driver provides overcurrent, overtemperature and undervoltage protection.

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4. X. Huang et al., "Characterization and Enhancement of 600V Cascode GaN Device," Virginia Tech 2015 CPES Industry Webinar, March 11, 2015.

5. Download these data sheets: LMG3410R050. LMG3410R070 and LMG3411R070

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