LMG352xR030-Q1 650-V 30-mΩ GaN FET with Integrated Driver, Protection, and Temperature Reporting

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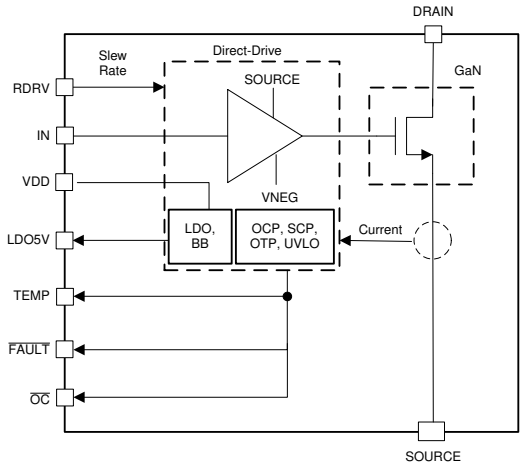
1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: –40 °C To +125 °C, T_J
- Qualified for JEDEC JEP180 for hard-switching topologies
- 650-V GaN-on-Si FET with Integrated gate driver
  - Integrated high precision gate bias voltage
  - 200-V/ns CMTI
  - 2.2-MHz switching frequency
  - 30-V/ns to 150-V/ns slew rate for optimization of switching performance and EMI mitigation
  - Operates from +12-V unregulated supply
- Robust protection
  - Cycle-by-cycle overcurrent and latched short-circuit protection with < 100-ns response
  - Withstands 720-V surge while hard-switching
  - Self-protection from internal overtemperature and UVLO monitoring
- Advanced power management
  - Digital temperature PWM output
  - Ideal diode mode reduces third-quadrant losses in LMG3525R030-Q1
- Top-side cooled 12-mm × 12-mm VQFN package separates electrical and thermal paths for lowest power loop inductance

2 Applications

- On-board (OBC) & wireless charger
- DC/DC converter
- Merchant network & server PSU



Simplified Block Diagram

3 Description

The LMG352xR030-Q1 GaN FET with integrated driver and protection enables designers to achieve new levels of power density and efficiency in power electronics systems.

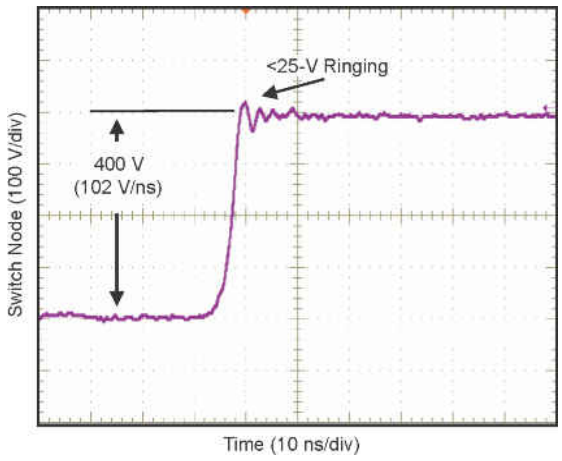
The LMG352xR030-Q1 integrates a silicon driver that enables switching speed up to 150 V/ns. TI's integrated precision gate bias results in higher switching SOA compared to discrete silicon gate drivers. This integration, combined with our low-inductance package, delivers clean switching and minimal ringing in hard-switching power supply topologies. Other features, including adjustable gate drive strength for EMI control, overtemperature, and robust overcurrent protection with fault indication, provide optimized BOM cost, board size, and footprint.

Advanced power management features include digital temperature reporting and TI's ideal diode mode. The temperature of the GaN FET is reported through a variable duty cycle PWM output, which enables the system to optimally manage loading. Ideal diode mode maximizes efficiency by reducing third-quadrant losses by enabling adaptive dead-time control.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
LMG352xR030-Q1	VQFN (52)	12.00 mm × 12.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Switching Performance at > 100 V/ns

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2021) to Revision B (June 2021)	Page
• Added LMG3525R030-Q1 to the data sheet	1

Changes from Revision * (October 2020) to Revision A (February 2021)	Page
• Updated the Pin Configuration and Functions section	3
• Updated Specifications tables	5
• Updated the Application and Implementation section	21
• Updated the Layout section	28
• Updated the Mechanical, Packaging, and Orderable Information section	32

5 Device Comparison

Table 5-1. Device Comparison Table

DEVICE NAME	DUAL OVERCURRENT / SHORT-CIRCUIT PROTECTION	TEMPERATURE REPORTING	IDEAL DIODE MODE
LMG3522R030-Q1	Yes	Yes	No
LMG3525R030-Q1	Yes	Yes	Yes

6 Pin Configuration and Functions

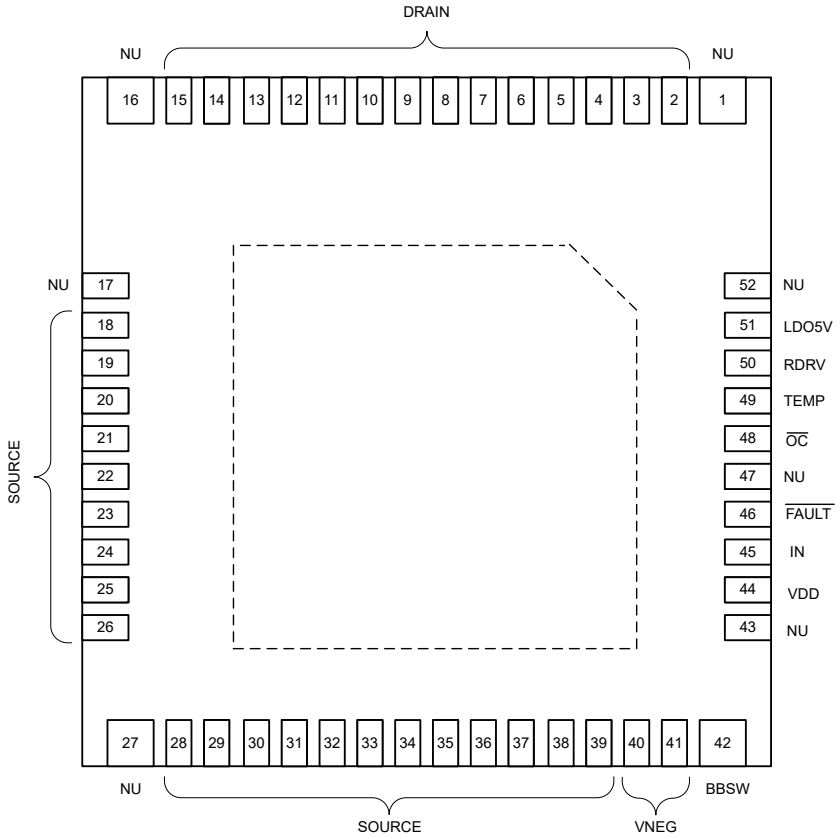

Figure 6-1. RQS (VQFN) Package 52 Pins (Top View)

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Table 6-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
LDO5V	51	P	5-V LDO output for external digital isolator.
RDRV	50	I	Drive strength selection pin. Connect a resistor from this pin to ground to set the turn-on drive strength to control slew rate. Tie the pin to GND to enable 150 V/ns and tie the pin to LDO5V to enable 100 V/ns.
TEMP	49	O	Temperature-sensing output.
$\overline{OC}$	48	O	Overcurrent and short-circuit fault output, push-pull, active low. Refer to Section 9.3.6 for details.
$\overline{FAULT}$	46	O	Fault output, push-pull, active low. Refer to Section 9.3.6 for details.
IN	45	I	CMOS-compatible noninverting gate drive input.
VDD	44	P	12-V power input, relative to source. Supplies 5-V rail and gate drive supply.
BBSW	42	P	Internal buck-boost converter switch pin. Connect an inductor from this point to power ground.
VNEG	40, 41	P	Negative supply output, bypass to ground with ceramic capacitors.
SOURCE	18-26, 28-39	P	Power transistor source, die-attach pad, thermal sink, power ground.
NU	17, 27, 43, 47, 52	NU	These pins must be soldered onto the PCB's landing pads. The PCB's landing pads are non-solder mask defined pads and not to be electrically connected to any electrical signals on the PCB. The pins are electrically connected internally to the SOURCE of the power device.
DRAIN	2-15	P	Power transistor drain.
NU	1, 16	NU	These pins must be soldered onto the PCB's landing pads. The PCB's landing pads are non-solder mask defined pads and not to be electrically connected to any electrical signals on the PCB. The pins are electrically connected internally to the DRAIN of the power device.
Thermal Pad		—	Thermal pad on top (Internally connected to SOURCE).

(1) I = input, O = output, P = power, NU = make no external connection

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7 Specifications

7.1 Absolute Maximum Ratings

Unless otherwise noted: voltages are respect to SOURCE connected to reference ground(1)

			MIN	MAX	UNIT
V_{DS}	Drain-source voltage (FET Off)			650	V
$V_{DS(surge)}$	Drain-source surge voltage (FET Switching)(2)			720	V
$V_{DS,tr}$	Drain-source transient ringing peak voltage (FET Off)(3)			800	V
	Pin voltage	V_{DD}	-0.3	20	V
		LDO5V	-0.3	5.5	V
		VNEG	-16	0.5	V
		BBSW	V_{VNEG}–1	V_{VDD}+0.5	V
		VIN	-0.3	20	V
		/FAULT, /OC, /TEMP	-0.3	V_{5V}+0.5	V
		RDRV	-0.3	5.5	V
$I_{D(RMS)}$	Drain RMS current (FET On)(4)			55	A
$I_{D(pulse)}$	Drain pulsed current (FET On, tp < 10 µs)		-125	Internally Limited	A
$I_{S(pulse)}$	Source pulsed current (FET Off, tp < 10 µs)			80	A
T_{STG}	Storage temperature		-55	150	°C
T_J	Operating Junction Temperature		-40	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Voltage while operating under surge conditions for 50 strikes (per VDE 0884-11) of the IEC61000-4-5 surge waveform applied to a half-bridge hard-switching at 100 kHz.
(3) Transient ringing peak voltage after device turn-off while operating under surge conditions in (2) above. Peak voltage damped to ≤ 720 V within 1 µs.
(4) The positive pulsed current must remain below the overcurrent threshold to avoid the FET being automatically shut off. The FET drain intrinsic positive pulsed current rating for tp < 10 µs is 125 A.

7.2 ESD Ratings

PARAMETER				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100–002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100–011	All pins	±500	
			Corner pins (1, 16, 17, 26, 27, 42, 43, and 52)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

7.3 Recommended Operating Conditions

Unless otherwise noted: voltages are respect to SOURCE connected to reference ground.

			MIN	NOM	MAX	UNIT
V_{DS}	Drain-source voltage (FET Switching)				520	V
$V_{DS(tr)}$	Drain-source transient ringing peak voltage (FET Off)(1)				650	V
V_{DS} dv/dt	Drain-source edge rate immunity for FET to remain off (half-bridge configuration)(2)				200	V/ns
	Supply voltage	V_{DD} (Maximum switching frequency derated for VVDD < 9 V)	7.5	12	18	V
	Input voltage	IN	0	5	18	V

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7.3 Recommended Operating Conditions (continued)

Unless otherwise noted: voltages are respect to SOURCE connected to reference ground.

			MIN	NOM	MAX	UNIT
$I_{D(RMS)}$	Drain RMS current				38	A
	Positive source current	LDO5V			25	mA
R_{RDRV}	RDRV to GND resistance from external slew-rate control resistor		0		500	kΩ
C_{VNEG}	VNEG to GND capacitance from external bypass capacitor at bias		1		10	uF
L_{BBSW}	BBSW to GND inductance from external buck-boost inductor		3	4.7	10	uH
T_J	Operating Junction temperature		-40		125	°C

(1) Transient ringing peak voltage after device turn-off. Peak voltage damped to ≤ 520 V within 1 µs.
(2) Driver must be ready to operate and IN pin must be kept at logic "0" during the common mode transient.

7.4 Thermal Information

THERMAL METRIC(1)		DEVICE	UNIT
		PKG DES (PKG FAM)	
		PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.13	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.19	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

Unless otherwise noted: voltage, resistance, capacitance, and inductance are respect to SOURCE connected with reference ground; –40 °C ≤ T_J ≤ 125 °C; 9 V ≤ V_{VDD} ≤ 18 V; V_{IN} = 5 V; RDRV connected to LDO5V; L_{BBSW} = 4.7 µH

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GAN POWER TRANSISTOR						
$R_{DS(on)}$	Total on-state resistance	T_J = 25°C		30	39	mΩ
		T_J = 125°C		56	73	mΩ
V_{SD}	Third-quadrant mode source-drain voltage	IN = 0 V, I_{SD} = 0.1 A		5		V
		IN = 0 V, I_{SD} = 20 A		7		V
I_{DSS}	Drain leakage current	V_{DS} = 650 V, T_J = 25°C		1	5	uA
		V_{DS} = 650 V, T_J = 125°C		10		uA
C_{OSS}	GaN output capacitance	IN = 0 V, V_{DS} = 400 V		218		pF
$C_{O(er)}$	Energy related effective output capacitance	IN = 0 V, VDS = 0-400 V		276		pF
$C_{O(tr)}$	Time related effective output capacitance			438		pF
E_{OSS}	Energy in output capacitance.		21	22	24.4	uJ
Q_{OSS}	Output charge			175		nC
Q_{RR}	Reverse recovery charge(1)			0		nC
SUPPLY CURRENTS						
I_Q	V_{DD} quiescent current (LMG3522)	V_{VDD} = 12 V, V_{IN} = 0 V or 5V, RDRV shorted to LDO5V		700	1200	uA

7.5 Electrical Characteristics (continued)

Unless otherwise noted: voltage, resistance, capacitance, and inductance are respect to SOURCE connected with reference ground; –40 ℃ ≤ T_J ≤ 125 ℃; 9 V ≤ V_{VDD} ≤ 18 V; V_{IN} = 5 V; RDRV connected to LDO5V; L_{BBSW} = 4.7 µH

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_Q	V_{DD} quiescent current (LMG3525)	V_{VDD} = 12 V, V_{IN} = 0 V or 5V, RDRV shorted to LDO5V		780	1300	uA
$I_{(op)}$	V_{DD} operating current	V_{VDD} = 12 V, f_{IN} = 140 kHz, soft-switching		16	19	mA
BUCK BOOST CONVERTER						
	VNEG average output voltage	VNEG sinking 50 mA	-14.6	-14	-13.4	V
	BBSW switching frequency	V_{VDD} = 9 V, VNEG sinking 150 mA, L_{BBSW} = 4.7 µH, L_{BBSW} peak current = 1 A		900		kHz
	Peak BBSW sourcing current at low peak current mode setting	VNEG sinking 25 mA, L_{DCDC} = 4.7 µH, C_{VNEG} = 2.2 µF	0.3	0.4	0.5	A
	Peak BBSW sourcing current at high peak current mode setting	VNEG sinking 100 mA, L_{BBSW} = 4.7 µH, C_{VNEG} = 2.2 µF	0.8	1	1.2	A
	High peak current mode setting enable – BBSW positive-going input threshold frequency		280	400	515	kHz
5 V LDO						
	Output voltage	LDO5V sourcing 25 mA	4.75	5	5.25	V
	Short-circuit current		25	50	100	mA
DIGITAL INPUT PINS						
$V_{IN,IT+}$	Positive-going input threshold voltage		1.7		2.45	V
$V_{IN,IT-}$	Negative-going input threshold voltage		0.7		1.3	V
	Input threshold hysteresis		0.8	0.83	1.5	V
	Input pull-down resistance	V_i = 2 V	100	150	200	kΩ
FAULT PINS						
	Low-level output voltage	Output sinking 8 mA		0.16	0.4	V
	High-level output voltage	Output sourcing 8 mA, Measured as $V_{LDO5V} – V_O$		0.2	0.4	V
UNDER VOLTAGE LOCKOUT						
$V_{VDD,IT+(UVLO)}$	VDD UVLO – positive-going input threshold voltage		6.6	7	7.6	V
$V_{VDD,IT-(UVLO)}$	VDD UVLO – negative-going input threshold voltage		6.1	6.5	6.8	V
	VDD UVLO – Input threshold voltage hysteresis			680		mV
$V_{VNEG,IT-(UVLO)}$	VNEG UVLO – negative-going input threshold voltage		-13.6	-13.0	-12.4	V
$V_{VNEG,IT+(UVLO)}$	VNEG UVLO – positive-going input threshold voltage		-13.2	-12.75	-12.2	V
GATE DRIVER						

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7.5 Electrical Characteristics (continued)

Unless otherwise noted: voltage, resistance, capacitance, and inductance are respect to SOURCE connected with reference ground; –40 ℃ ≤ T_J ≤ 125 ℃; 9 V ≤ V_{VDD} ≤ 18 V; V_{IN} = 5 V; RDRV connected to LDO5V; L_{BBSW} = 4.7 µH

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Turnon drain slew rate	From V_{DS} < 320 V to V_{DS} < 80 V, RDRV connected to R_{RDRV} = 200 kΩ, TJ = 25 ℃, V_{BUS} = 400 V, L_{HB} current = 10 A, see Figure 8-1		20		V/ns
		From V_{DS} < 320 V to V_{DS} < 80 V, RDRV directly connected to LDO5V, TJ = 25 ℃, V_{BUS} = 400 V, L_{HB} current = 10 A, see Figure 8-1		100		V/ns
		From V_{DS} < 320 V to V_{DS} < 80 V, RDRV connected to ground, TJ = 25 ℃, V_{BUS} = 400 V, L_{HB} current = 10 A, see Figure 8-1		150		V/ns
	Slew rate variation	From V_{DS} < 320 V to V_{DS} < 80 V, RDRV directly connected to LDO5V, TJ = 25 ℃, V_{BUS} = 400 V, L_{HB} current = 10 A, see Figure 8-1		25		%
$F_{IN(max)}$	Maximum GaN FET switching frequency.	VNEG rising to > –13.25 V, soft-switched, maximum switching frequency derated for V_{VDD} < 9 V	2.2			MHz
FAULTS						
$I_{IT(OC)}$	DRAIN overcurrent fault – input threshold current			70		A
$I_{TRIP,SC}$	DRAIN short-circuit fault – input threshold current			95		A
	di/dt threshold between overcurrent and short-circuit faults		150			A/µs
	Short-circuit current to overcurrent fault trip difference			25		A
	GaN temperature fault – postive-going input threshold temperature			165		°C
	Driver temperature fault – positive-going input threshold temperature			185		°C
	GaN / Driver Temperature fault – input threshold temperature hysteresis			20		°C
PWM TEMPERATURE OUTPUT						
	Digital Temperature Report Output Frequency		6	11	18	kHz
	Output PWM Duty Cycle	GaN T_J = 150 ℃		80		%
	Output PWM Duty Cycle	GaN T_J = 125 ℃		65		%
	Output PWM Duty Cycle	GaN T_J = 85 ℃		40		%
	Output PWM Duty Cycle	GaN T_J = 25 ℃		3		%
THIRD QUADRANT TURN ON (LMG3525x, 26x)						
$V_{IT(3rd)}$	Drain-source third-quadrant detection – input threshold voltage	V_{IN} = 0 V	-0.15	0	0.15	V
$I_{IT(ZC)}$	Drain zero-current detection – input threshold current	V_{IN} = 0 V	-0.2	0	0.2	A

(1) Excluding Qoss

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7.6 Switching Characteristics

Unless otherwise noted: voltage, resistance, capacitance, and inductance are respect to SOURCE connected with reference ground; –40 ℃ ≤ T_J ≤ 125 ℃; 9 V ≤ V_{VDD} ≤ 18 V; V_{IN} = 5 V; RDRV connected to LDO5V; L_{BBSW} = 4.7 µH

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWITCHING TIMES						
$t_{pd(on)}$	Driver turn-on propagation delay	From VIN > VIN,IT+ to ID > 1 A, VBUS = 400 V, LHB current = 10 A, see Figure 8-1 and Figure 8-2		30	50	ns
$t_{d(on)}$	Turn-on delay	From ID > 1 A to VDS < 320 V, VBUS = 400 V, LHB current = 10 A, see Figure 8-1 and Figure 8-2		5	6	ns
$t_{r(on)}$	Turn-on rise time	From VDS < 320 V to VDS < 80 V, VBUS = 400 V, LHB current = 10 A, see Figure 8-1 and Figure 8-2		2.5	3	ns
$t_{pd(off)}$	Driver turn-off propagation delay	From VIN < VIN,IT– to VDS > 10 V, VBUS = 400 V, LHB current = 10 A, see Figure 8-1 and Figure 8-2		32	50	ns
$t_{d(off)}$	Turn-off delay	From VDS > 10 V to VDS > 80 V, VBUS = 400 V, LHB current = 10 A, see Figure 8-1 and Figure 8-2		6	10	ns
$t_{f(off)}$	Turn-off fall time(1)	From VDS > 80 V to VDS > 320 V, VBUS = 400 V, LHB current = 10 A, see Figure 8-1 and Figure 8-2			23	ns
	Minimum IN high pulse-width for FET turn-on	VIN rise/fall times < 1 ns, VDS falls to < 200 V, VBUS = 400 V, LHB current = 10 A, see Figure 8-1			24	ns
STARTUP TIMES						
	Driver start-up delay time	From V_{VDD} > $V_{VDD,IT+(UVLO)}$ to /FAULT high, C_{LDO5V} = 100 nF, C_{VNEG} = 2.2 µF at 0-V bias linearly decreasing to 1.5 µF at 15-V bias			400	us
FAULT TIMES						
$t_{d(OC)}$	Overcurrent fault FET turn-off delay, FET on before overcurrent	From ID > IIT(OC) to FET off, ID di/dt = 100 A/µs		90	135	ns
$t_{d(SC)}$	Short-circuit current fault FET turn-off delay, FET on before short circuit	From ID > IIT(SC) to FET off, ID di/dt = 700 A/µs		90	135	ns
	Overcurrent fault FET turn-off delay, FET turning on into overcurrent	From FET turn-on to FET off, dv/dt = 100 V/ns		200	280	ns
	Short-circuit fault FET turn-off delay, FET turning on into short circuit	From FET turn-on to FET off, dv/dt = 100 V/ns		105	217	ns
$t_{d(reset)}$	IN reset delay time to clear /FAULT latch	From V_{IN} < $V_{IN,IT–}$ to /FAULT high	250	350	580	us
THIRD QUADRANT TURN ON (LMG3525)						
$t_{d(idm\_on)}$	Ideal diode mode FET turn-on delay time	V_{DS} < $V_{IT(3rd)}$ to FET turn-on, V_{DS} dv/dt = –100 V/ns created with a half-bridge configuration inductor at 5 A		35	75	ns
$t_{d(idm\_off)}$	Ideal diode mode FET turn-off delay time	I_D > $I_{IT(ZC)}$ to FET turn-off, ID di/dt = 100 A/µs created with a half-bridge configuration		30	68	ns
t_{3rd_Blank}	Blanking time after IN falling for ideal-diode-mode.		80	115	180	ns

(1) During turn off, V_{DS} rise time is the result of the resonance of C_{OSS} and loop inductance, as well as load current.

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8 Parameter Measurement Information

8.1 Switching Parameters

The circuit used to measure most switching parameters is shown in Figure 8-1. The top LMG352xR030-Q1 device in this circuit is used to re-circulate the inductor current and functions in third-quadrant mode only. The bottom device is the active device that turns on to increase the inductor current to the desired test current. The bottom device is then turned off and on to create switching waveforms at a specific inductor current. Both the drain current (at the source) and the drain-source voltage is measured. The specific timing measurement is shown in Figure 8-2. TI recommends to use the half-bridge as double pulse tester. Excessive third-quadrant operation may overheat the top device.

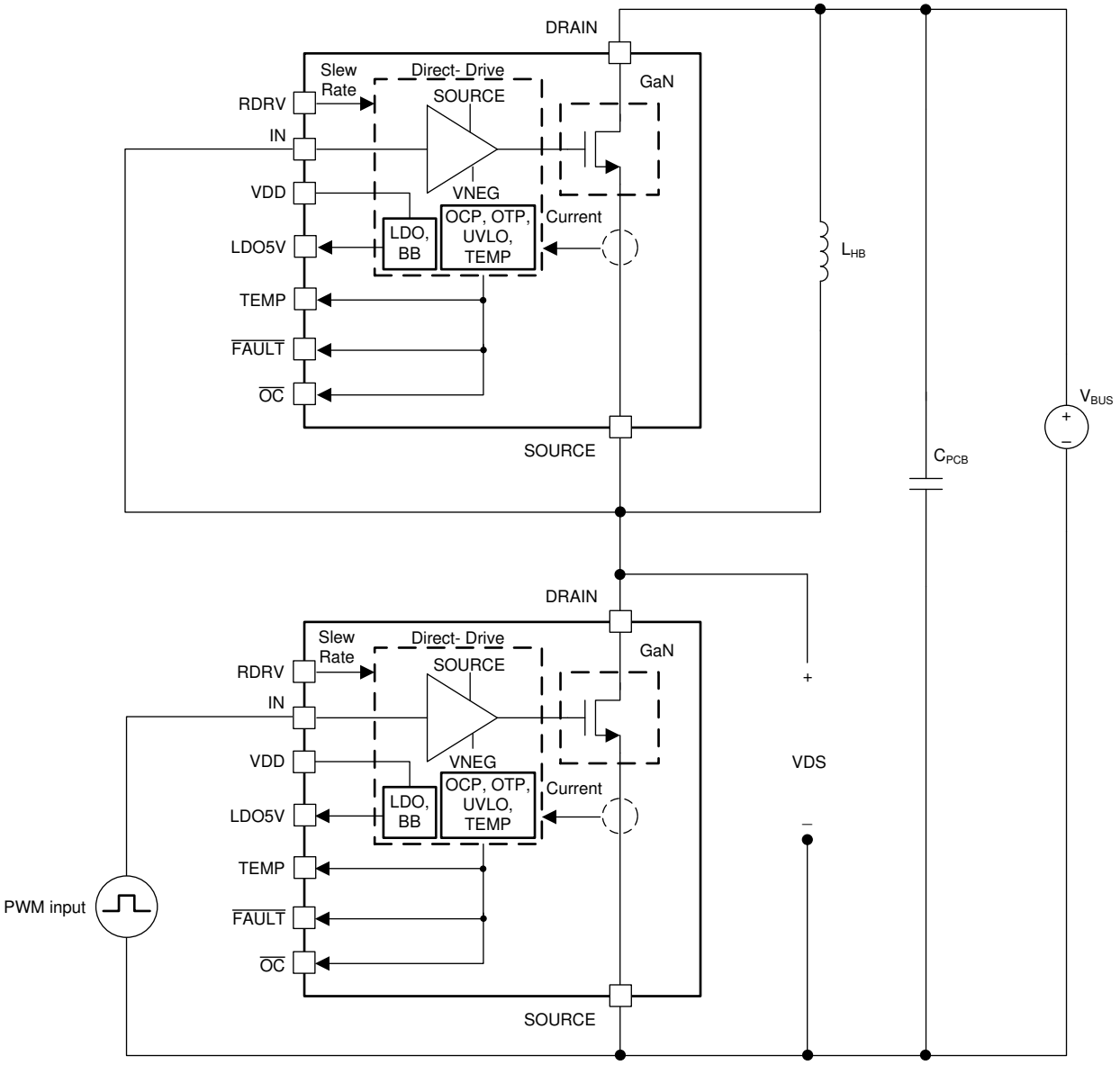

Figure 8-1. Circuit Used to Determine Switching Parameters

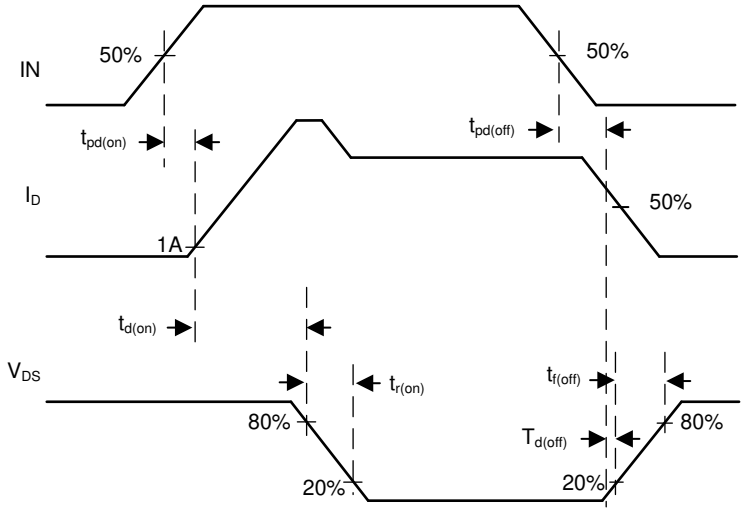

Figure 8-2. Measurement to Determine Propagation Delays and Slew Rates

8.1.1 Turn-On Delays

The timing of the turn-on transition has three components: propagation delay, turn-on delay, and fall time. The first component is the propagation delay of the driver from when the input goes high to when the GaN FET starts turning on (represented by 1-A drain current). The turn-on delay is the delay from when the FET starts turning on to when the drain voltage swings down by 20 percent. Finally, the V_{DS} fall time is the time it takes the drain voltage to slew between 80 percent and 20 percent of the bus voltage. The drive-strength resistor value has a large effect on turn-on delay and V_{DS} fall time, but does not affect the propagation delay significantly.

8.1.2 Turn-Off Delays

The timing of the turn-off transition has three components: propagation delay, turn-off delay, and rise time. The first component is the propagation delay of the driver from when the input goes low to when the GaN FET starts turning off. The turn-off delay is the delay from when the FET starts turning of (represented by the drain rising above 10 V) to when the drain voltage swings up by 20 percent. Finally, the V_{DS} rise time is the time it takes the drain voltage to slew between 20 percent and 80 percent of the bus voltage. The turn-off delays of the LMG352xR030-Q1 are independent of the drive-strength resistor, but the turn-off delay and the V_{DS} rise time are heavily dependent on the load current.

8.1.3 Drain Slew Rate

The slew rate, measured in volts per nanosecond, is measured on the turn-on edge of the LMG352xR030-Q1. The slew rate is considered over the V_{DS} fall time, which is when the drain falls from 80 percent to 20 percent of the bus voltage. The drain slew rate is thus given by 60 percent of the bus voltage divided by the V_{DS} fall time. This drain slew rate is dependent on the R_{DRV} value and is only slightly affected by the drain current.

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9 Detailed Description

9.1 Overview

The LMG352xR030-Q1 is a high-performance power IC, GaN device with integrated gate driver. The GaN device offers zero reverse recovery and ultra-low output capacitance, which enables premium efficiency in bridge-based topologies. A Direct Drive architecture is applied to control the GaN device within the power IC. When the driver is powered up, the GaN device is controlled directly by the integrated gate driver. This architecture provides superior switching performance compared with the traditional cascode approach. The integrated driver solves a number of challenges in GaN applications.

The integrated driver ensures the device stays off for high drain slew rates. It also helps protect GaN device from overcurrent, short-circuit, undervoltage, and overtemperature. Regarding fault signal reporting, LMG352xR030-Q1 provides different reporting method which is shown in Table 9-1. Refer to Section 9.3.6 for more details. The integrated driver is also able to sense the die temperature and send out the temperature signal through a modulated PWM signal.

Unlike Si MOSFETs, there is no p-n junction from source to drain in GaN devices. That is why GaN devices have no reverse recovery charge. However, the GaN device can still conduct from source to drain in third-quadrant of operation similar to a body diode, but with higher voltage drop and higher conduction loss. Third-quadrant operation can be defined as follows: when the GaN device is turned off and negative current pulls the drain node voltage to be lower than its source, the voltage drop across the GaN device during third-quadrant operation is high. Therefore, TI recommends to operate with synchronous switching and keep the duration of third-quadrant operation at minimum.

9.2 Functional Block Diagram

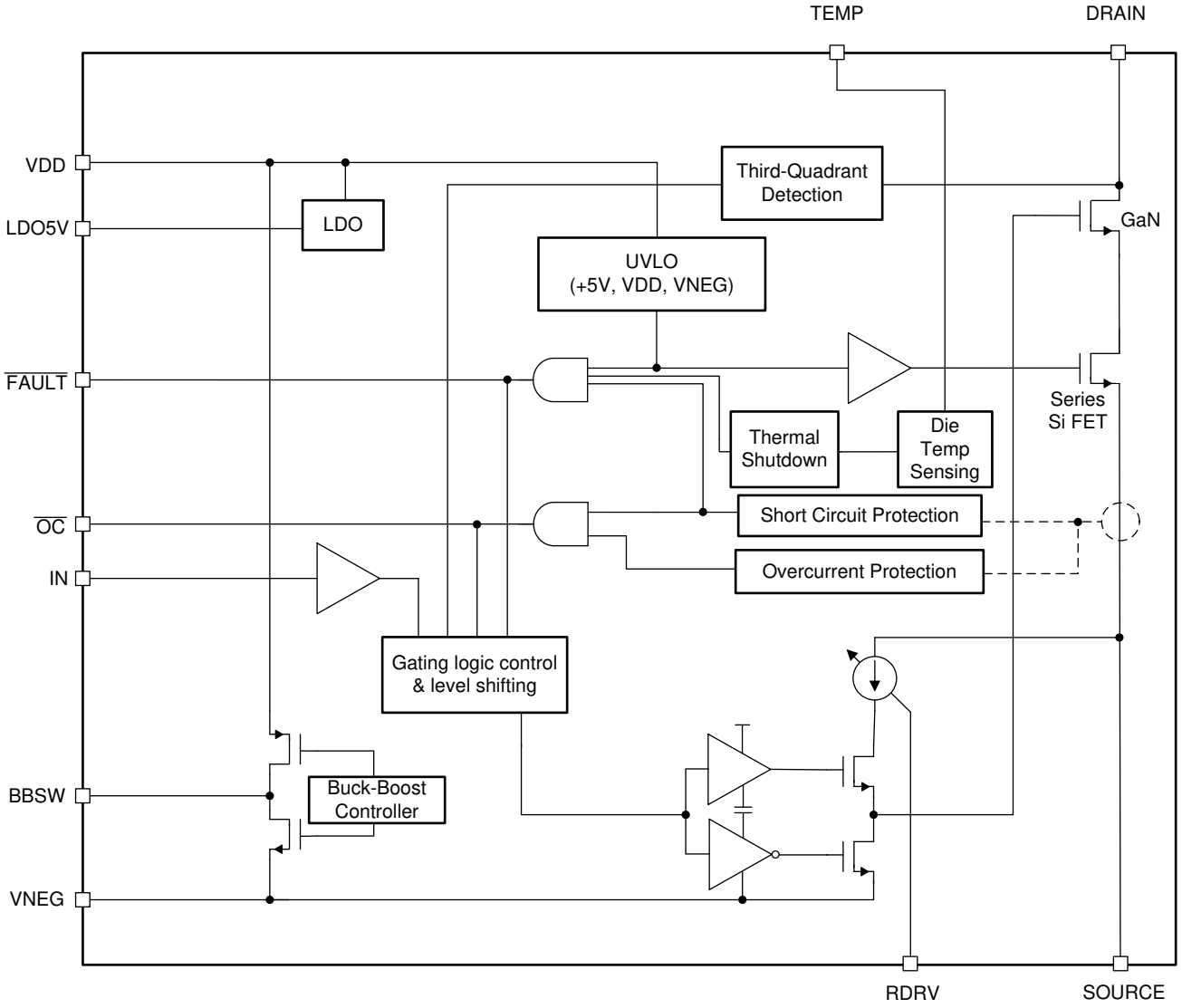

Figure 9-1. Simplified Block Diagram of LMG352xR030-Q1

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9.3 Feature Description

The LMG352xR030-Q1 includes advanced features to provide premium switching performance and converter efficiency.

9.3.1 Direct-Drive GaN Architecture

The LMG352xR030-Q1 uses a series Si FET to ensure the power IC stays off when VDD bias power is not applied. When the VDD bias power is off, the series Si FET is interconnected with the GaN device in a cascode mode, which is shown in Figure 9-1. The gate of the GaN device is held within a volt of the series Si FET's source. When a high voltage is applied on the module and the silicon FET blocks the drain voltage, the V_{GS} of the GaN device decreases until the GaN device passes the threshold voltage. Then, the GaN device is turned off and blocks the remaining major part of drain voltage. There is an internal clamp to make sure that the VDD does not exceed its maximum rating. This avoids the avalanche of the series Si FET when there is no bias power.

When LMG352xR030-Q1 is powered up with VDD bias power, the internal buck-boost converter generates a negative voltage (V_{VNEG}) that is sufficient to directly turn off the GaN device. In this case, the series Si FET is held on and the GaN device is gated directly with the negative voltage. During operation, this removes the switching loss of the series Si FET.

9.3.2 Drain-Source Voltage Capability

Due to the silicon FET's long reign as the dominant power-switch technology, many designers are unaware that the headline drain-source voltage cannot be used as an equivalent point to compare devices across technologies. The headline drain-source voltage of a silicon FET is set by the avalanche breakdown voltage. The headline drain-source voltage of a GaN FET is set by the long term reliability with respect to data sheet specifications.

Exceeding the headline drain-source voltage of a silicon FET can lead to immediate and permanent damage. Meanwhile, the breakdown voltage of a GaN FET is much higher than the headline drain-source voltage. For example, the breakdown voltage of the LMG352xR030-Q1 is more than 800 V.

A silicon FET is usually the weakest link in a power application during an input voltage surge. Surge protection circuits must be carefully designed to ensure the silicon FET avalanche capability is not exceeded because it is not feasible to clamp the surge below the silicon FET breakdown voltage. Meanwhile, it is easy to clamp the surge voltage below a GaN FET breakdown voltage. In fact, a GaN FET can continue switching during the surge event which means output power is safe from interruption.

The LMG352xR030-Q1 drain-source capability is explained with the assistance of Figure 9-2. The figure shows the drain-source voltage versus time for a GaN FET for a single switch cycle in a switching application. No claim is made about the switching frequency or duty cycle.

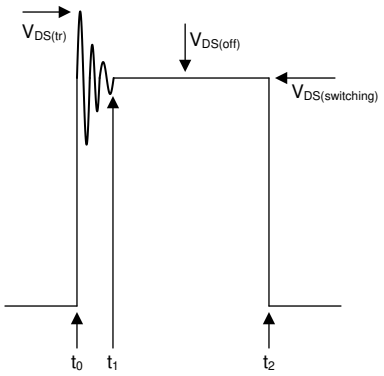

Figure 9-2. Drain-Source Voltage Switching Cycle

The waveform starts before t_0 with the FET in the on state. At t_0 the GaN FET turns off and parasitic elements cause the drain-source voltage to ring at high frequency. The peak ring voltage is designated $V_{DS(tr)}$. The high frequency ringing has damped out by t_1. Between t_1 and t_2 the FET drain-source voltage is set by

the characteristic response of the switching application. The characteristic is shown as a flat line, but other responses are possible. The voltage between t_1 and t_2 is designated $V_{DS(off)}$. At t_2 the GaN FET is turned on at a non-zero drain-source voltage. The drain-source voltage at t_2 is designated $V_{DS(switching)}$. Unique $V_{DS(tr)}$, $V_{DS(off)}$ and $V_{DS(switching)}$ parameters are shown because each can contribute to stress over the lifetime of the GaN FET.

The LMG352xR030-Q1 drain-source surge voltage capability is seen with the absolute maximum ratings $V_{DS(tr)}$ and $V_{DS(surge)}$ in Absolute Maximum Ratings where $V_{DS(surge)}$ is the same as $V_{DS(off)}$ and $V_{DS(switching)}$ in Figure 9-2. More information about the surge capability of TI GaN FETs is found in A New Approach to Validate GaN FET Reliability to Power-line Surges Under Use-conditions.

9.3.3 Internal Buck-Boost DC-DC Converter

An internal inverting buck-boost converter generates a regulated negative rail for the turn-off supply of the GaN device. The buck-boost converter is controlled by a peak current mode, hysteretic controller. In normal operation, the converter remains in discontinuous-conduction mode, but may enter continuous-conduction mode during start-up and overload the conditions. The converter is controlled internally and requires only a single surface-mount inductor and output bypass capacitor.

The LMG352xR030-Q1 supports the GaN operation up to 2.2 MHz. As power consumption is very different in a wide switching frequency range enabled by the GaN device, two peak current limits are used to control the buck-boost converter. When switching frequency is in the lower range, the peak current is set to the lower value (around 0.4 A) so a smaller inductor can be selected. When switching frequency is in the higher range, the peak current will be raised to the higher value (around 1 A) and will require a larger inductor. There is a filter on this frequency detection logic, therefore the LMG352xR030-Q1 requires 5 consecutive cycles at the higher frequency before it is set to the higher buck-boost peak current limit. Remember that the current limit will not go down again until power off once the higher limit is set. It will not change even when switching frequency goes back to the lower range.

For recommendations on the required passives, see Section 10.2.2.3.

9.3.4 VDD Bias Supply

With a LDO to supply internal low voltage circuits and a buck-boost converter to regulate the gate voltage, the input is able to support wide VDD voltage range from 7.5 V to 18 V. However, the maximum switching frequency is de-rated for input voltages less than 9 V. TI recommends to have a 12-V unregulated power supply to supply VDD. No specific external LDO is needed.

9.3.5 Auxiliary LDO

There is a 5-V voltage regulator inside the part used to supply external loads, such as digital isolators for the high-side drive signal. The digital outputs of the part use this rail as their supply. No capacitor is required for stability, but transient response will be poor if no external capacitor is provided. If the application uses this rail to supply external circuits, TI recommends to have a capacitor of at least 0.1 µF for improved transient response. A larger capacitor can be used for further transient response improvement. The decoupling capacitor used here should be a low-ESR ceramic type.

9.3.6 Fault Detection

The GaN power IC integrates overcurrent protection (OCP), short-circuit protection (SCP), overtemperature protection (OTP) and undervoltage lockout (UVLO).

9.3.6.1 Overcurrent Protection and Short-Circuit Protection

There are two types of current faults which can be detected by the driver: overcurrent fault and short-circuit fault.

The overcurrent protection (OCP) circuit monitors drain current and compares that current signal with an internally set limit. Upon detection of the overcurrent, the LMG352xR030-Q1 conducts cycle-by-cycle overcurrent protection as shown in Figure 9-3. In this mode, the GaN device is shut off when overcurrent happens, but the overcurrent signal will clear after the input PWM goes low. In the next cycle, the GaN device can turn on as normal. The cycle-by-cycle function can be used in cases where steady-state operation current is below the OCP level but transient response can still reach current limit, while the circuit operation cannot be paused. It also prevents the GaN device from overheating by having overcurrent induced conduction loss.

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The short-circuit protection (SCP) monitors drain current and compares that current signal with a internally set limit higher than that of OCP as shown in Figure 9-4. It is designed to protect the GaN device from high-current short-circuit fault. When SCP happens at high current, the driver is intentionally slowed down to obtain lower di/dt. Therefore, lower overshoot voltage and ringing can be achieved during the turn-off event.On detection of the overcurrent, LMG352xR030-Q1 conduct latched turn-off. This fast response circuit could protect the GaN device even under a hard short-circuit condition. In this protection, the GaN device is shut off and held off until the fault is reset by either holding the IN pin low for a period of time defined in Section 7 or removing power from VDD.

During OCP or SCP in a half bridge, after the current reaches the upper limit and the device is turned off by protection, the PWM input of the device could still be high and the PWM input of the complementary device could still be low. In this case, the load current can flow through the third quadrant of the complementary device with no synchronous rectification. The extra high negative voltage drop (–6 V to –8 V) from drain to source could lead to high third-quadrant loss, similar to dead time loss but with much longer time. Section 9.3.9 offers adaptive dead time and reduces third-quadrant loss.

For safety considerations, OCP allows cycle-by-cycle operation while SCP will latch the device until reset. By reading the $\overline{\text{FAULT}}$ and $\overline{\text{OC}}$ pins, the exact current fault type can be determined. Refer to Section 9.3.6.4 for detailed information.

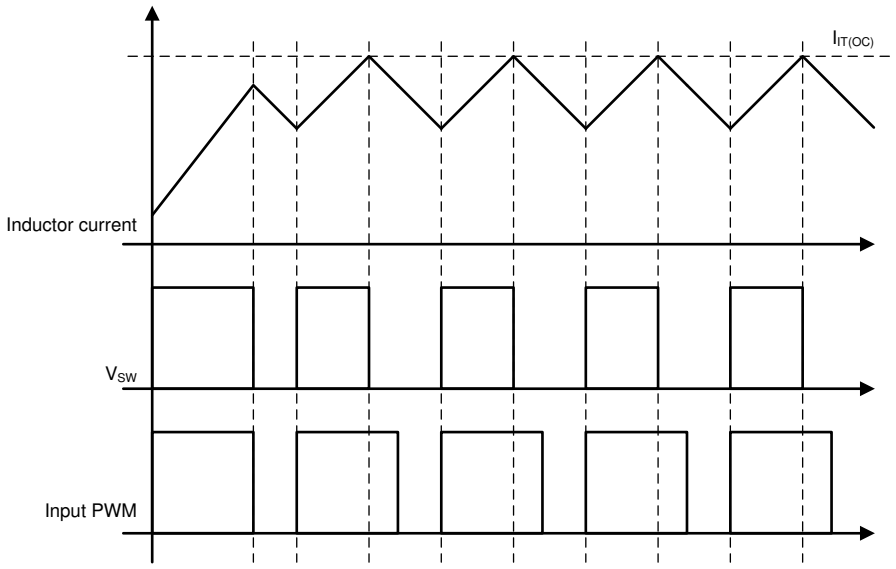

Figure 9-3. Cycle-by-Cycle OCP Operation

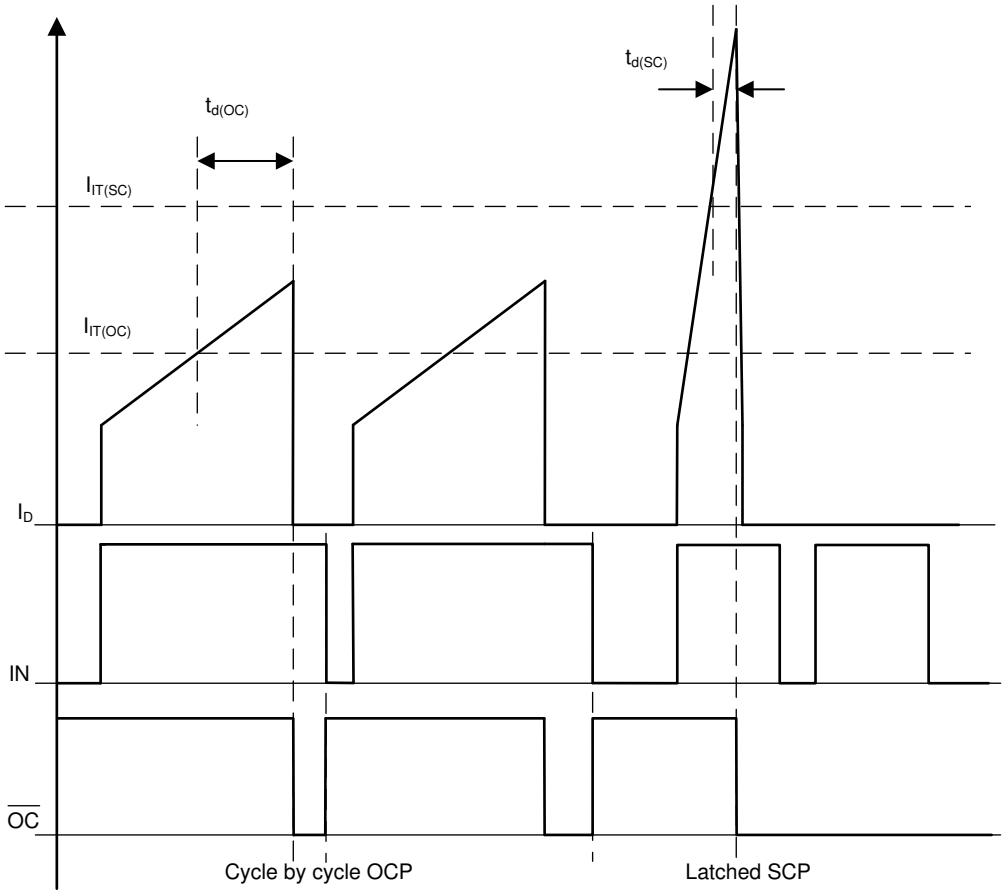

Figure 9-4. Overcurrent Detection vs. Short-Circuit Detection

9.3.6.2 Overtemperature Shutdown

There are two overtemperature shutdown thresholds in the part. The first one measures the GaN die temperature and trips around 165 °C. When it trips, the power IC disables switching and asserts the $\overline{\text{FAULT}}$ pin, but maintains the buck-boost and external LDO. During the overtemperature shutdown, the GaN device is held off until the temperature falls below the hysteresis limit, typically 20 °C below the turn-off threshold. This is not a latched protection scheme. In most applications, disabling the switching will allow the device to cool off. However, if there is instead a short circuit in the VNEG rail or the external 5-V LDO, the driver die temperature will continue to rise. If the silicon driver die temperature exceeds 185 °C, it will also shut down the buck-boost and the external LDO.

If the GaN die is over 165 °C and the overtemperature shutdown is active, but the driver is not over 185 °C where the buck-boost shuts down, the part will operate as an ideal diode that ignores the input and turns on and off automatically when it detects third-quadrant current. This is to lower the power dissipated in the GaN in third-quadrant operation.

9.3.6.3 UVLO Protection

The LMG352xR030-Q1 supports a wide range of VDD voltage. However, when the device is below UVLO threshold, the GaN device will stop switching and be held off. The $\overline{\text{FAULT}}$ pin will be pulled low as an indication of UVLO. The LDO is turned on by the rising-edge of the VIN UVLO and shut off around 5 V to 6 V.

9.3.6.4 Fault Reporting

The $\overline{\text{FAULT}}$ and $\overline{\text{OC}}$ outputs form a fault reporting scheme together. They are both push-pull outputs indicating the readiness and fault status of the driver. These two pins are logic high in normal operation, and will change logic according to Table 9-1.

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Table 9-1. Fault Types and Reporting

	NORMAL	UVLO, OT, and RDRV-OPEN	OVERCURRENT	SHORT-CIRCUIT
$\overline{\text{FAULT}}$	1	0	1	0
$\overline{\text{OC}}$	1	1	0	0

$\overline{\text{FAULT}}$ is held low when starting up until the series Si FET is turned on. During operation, if the power supplies go below the UVLO thresholds or the device temperature go above the OT thresholds, power device is disabled and $\overline{\text{FAULT}}$ is held low until the power supplies or the device temperature recover. If RDRV is open, $\overline{\text{FAULT}}$ is also held low. In an short-circuit or overtemperature fault condition, $\overline{\text{FAULT}}$ is held low until the fault latches are reset or fault is cleared. The $\overline{\text{OC}}$ pin will be held low if there is a short-circuit or overcurrent fault. The signals help notify the controller the exact type of faults by reading the truth table. If a combined reporting of the faults on a single pin is desired, one can short the $\overline{\text{OC}}$ pin to ground during power up. All faults will assert the $\overline{\text{FAULT}}$ pin then and the $\overline{\text{OC}}$ pin will not be used. Internal protection happens regardless the connection of pin outputs, however.

9.3.7 Drive Strength Adjustment

The LMG352xR030-Q1 allows users to adjust the drive strength of the device and obtain desired slew rate, which provides the flexibility to optimize switching loss and noise coupling.

To adjust drive strength, a resistor can be placed between the RDRV pin and GND pin. The resistance determines the slew rate of the device, from 30 V/ns to 150 V/ns, during turn-on. On the other hand, there are two dv/dt values that can be selected without the resistor: shorting the RDRV pin to ground provides 150 V/ns of slew rate, and shorting the RDRV pin to 5 V provides 100 V/ns of slew rate.

9.3.8 Temperature-Sensing Output

The integrated driver senses the GaN die temperature and outputs the information through a modulated PWM signal on the TEMP pin. The typical PWM frequency is 11 kHz with the same refresh rate. The minimum PWM duty cycle is around 1%, which can be observed at temperature below 25 °C. The target temperature range is from 25 °C to 150 °C, and the corresponding PWM duty cycle is typically from 3% to 80%. At temperatures above 150 °C, the duty cycle will continue to increase linearly until overtemperature fault happens. When overtemperature happens, the TEMP pin will be pulled high to indicate this fault until the temperature is reduced to the normal range. There is a hysteresis to clear overtemperature fault.

9.3.9 Sync-FET Mode Operation

GaN devices do not have body diodes, but is still able to conduct current in third-quadrant (source to drain) when it is OFF. However, the voltage drop of GaN devices is higher than that of Si diodes during third-quadrant conduction. This results in higher power loss if not handled properly. The excessive loss can be observed in prolonged dead time or cycle-by-cycle current limit mode, leading to overtemperature, which could trigger protective shut down. To mitigate this problem, a Sync-FET Mode operation is implemented in the power IC.

Figure 9-5 shows how Sync-FET Mode operation achieves adaptive dead time and reduces third-quadrant loss in a boost converter. Before IN Pin of the free-wheeling IC goes high, the IC is able to detect the third-quadrant current and automatically turn ON GaN device after $t_{d(idm\_on)}$, typically around 35ns. When IN Pin of the free-wheeling IC goes low, GaN device is turned OFF. After turn-off transient, there is a blanking time, t_{3rd_Blank}, typically around 115ns, to prevent the unwanted re-turn on during dead time.

A state machine has been also used to summarize the Sync-FET Mode operation. Please see Figure 9-6. In a half bridge:

- For the hard-switching IC in a half bridge
  - When IN Pin goes high, GaN device is always turned ON, and the hard-switching IC starts conducting first-quadrant current.
  - When IN Pin goes low, GaN device is turned OFF, and the hard-switching IC starts blocking positive V_{DS}.
  - When t_{3rd_Blank} expires, GaN device stays OFF, and the hard-switching IC starts detecting first-quadrant current, including both conduction and leakage current.

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  - When leakage current and positive V_{DS} presents, GaN device stays OFF and keeps blocking before IN Pin of the hard-switching IC goes high.
- For the free-wheeling IC in a half bridge
  - When IN Pin goes high, GaN device is always turned ON, and the free-wheeling IC starts conducting third-quadrant current at negative V_{DS}, product of negative I_D and $R_{DS(on)}$.
  - When IN Pin goes low, GaN device is turned OFF, and the free-wheeling IC starts conducting third-quadrant current at V_{SD}, third-quadrant mode source-drain voltage.
  - When t_{3rd_Blank} expires, GaN device stays OFF and continues third-quadrant conduction, and the free-wheeling IC starts detecting first-quadrant current, including both conduction and leakage current.
  - When first-quadrant current and positive V_{DS} presents at turn ON of the hard-switching IC, GaN device stays OFF but starts blocking, and the free-wheeling IC starts detecting third-quadrant current.
  - When third-quadrant current and negative V_{DS} presents at turn OFF of the hard switching IC, GaN device stays OFF during detection, t_{3rd_Det}, and then is turned ON by Sync-FET Mode. In Sync-FET Mode, the free-wheeling IC keeps detecting first-quadrant current, including both conduction and leakage current, before IN Pin goes high.
  - If first-quadrant current presents before IN Pin goes high, GaN device will be turned OFF, and the free-wheeling IC will NOT be turned ON again by Sync-FET Mode before IN Pin goes high.

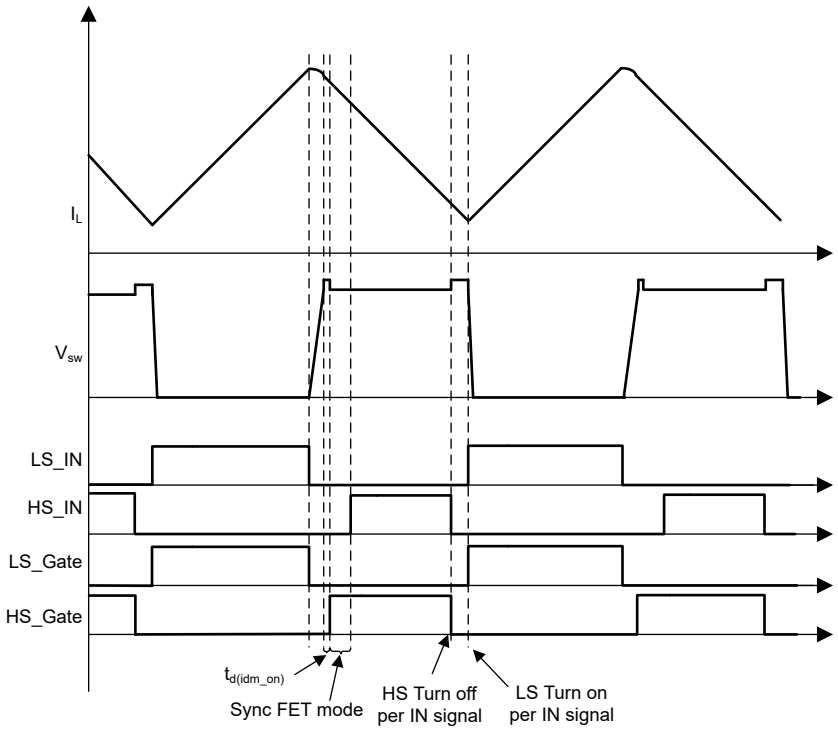

Figure 9-5. Dead Time Reduction In Sync Mode Operation

ADVANCE INFORMATION

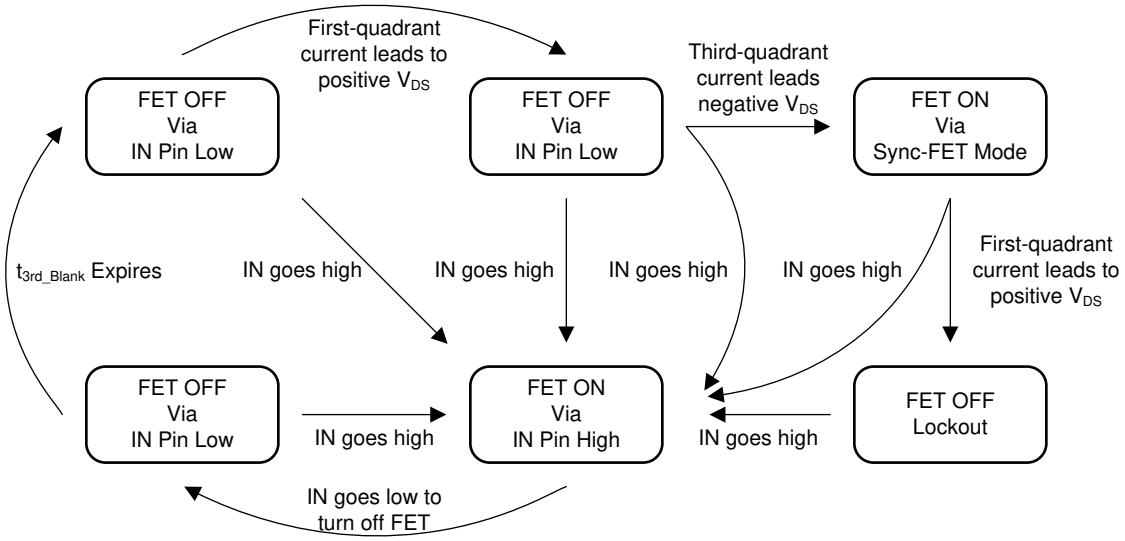

Figure 9-6. Sync FET Mode State Machine

9.4 Device Functional Modes

The device has one mode of operation that applies when operated within the Recommended Operating Conditions.

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10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The LMG352xR030-Q1 is a power IC targeting hard-switching and soft-switching applications running up to 520V bus voltage. GaN devices offer zero reverse-recovery charge enabling high-frequency, hard-switching applications like the totem-pole PFC. Low Q_{oss} of GaN devices also benefits soft-switching converters, such as the LLC and phase-shifted full-bridge configurations. As half-bridge configurations are the foundation of those applications, this section will describe how to use the LMG352xR030-Q1 in half-bridge configuration.

ADVANCE INFORMATION

10.2 Typical Application

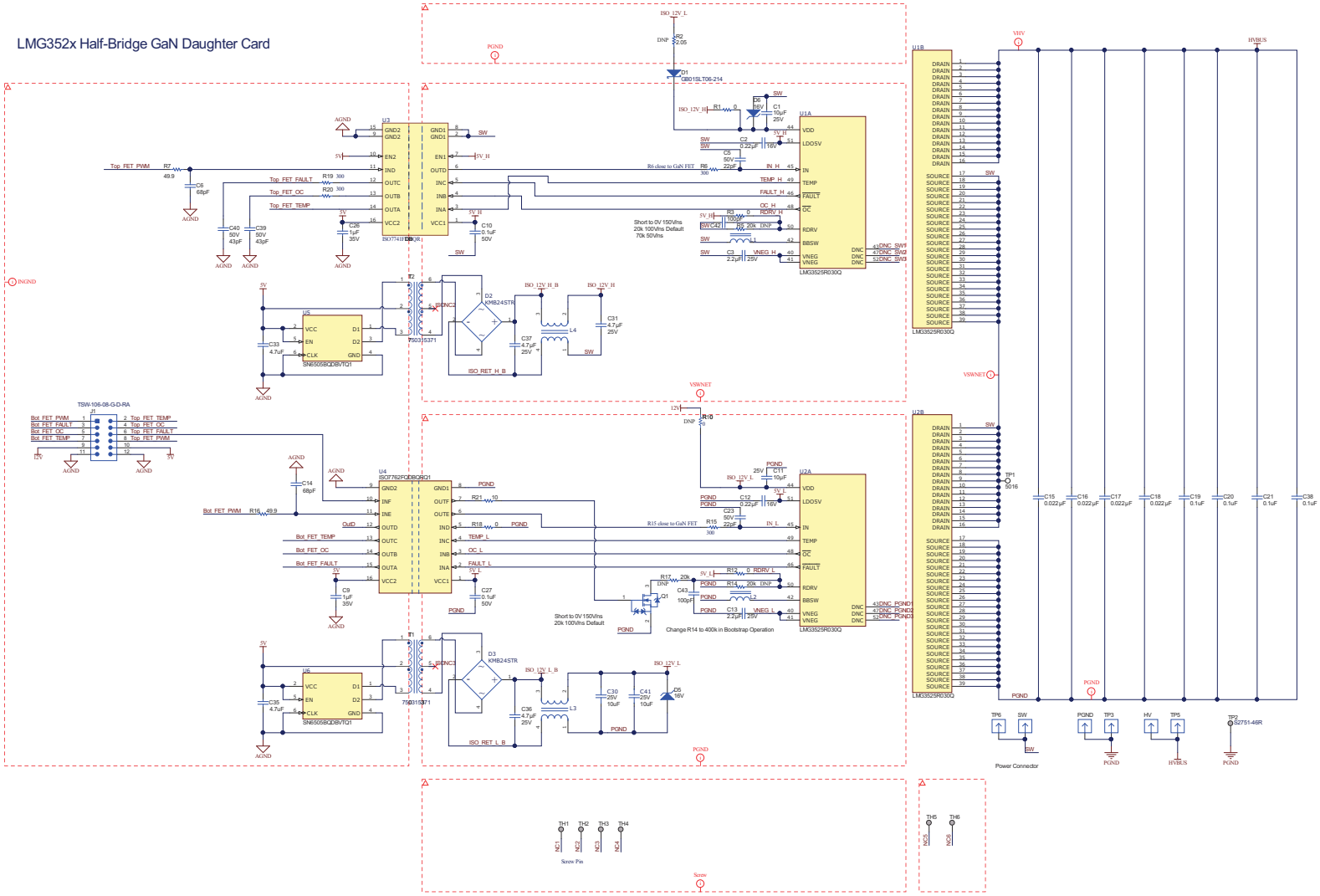

Figure 10-1. Typical Half-Bridge Application

10.2.1 Design Requirements

This design example is for a hard-switched boost converter which is representative of PFC applications. The system parameters for this design are shown in Table 10-1.

Table 10-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	200 VDC
Output voltage	400 VDC
Input (inductor) current	20 A
Switching frequency	100 kHz

10.2.2 Detailed Design Procedure

In high-voltage power converters, circuit design and PCB layout are essential for high-performance power converters. As designing a power converter is out of the scope of this document, this data sheet describes how to build well-behaved half-bridge configurations with the LMG352xR030-Q1.

10.2.2.1 Slew Rate Selection

The slew rate of LMG352xR030-Q1 can be adjusted between approximately 20 V/ns and 150 V/ns by connecting a resistor, R_{DRV}, from the RDRV pin to GND. The slew rate affects GaN device performance in terms of:

- Switching loss
- Voltage overshoot
- Noise coupling
- EMI emission

Generally, high slew rates provide low switching loss, but high slew rates can also create higher voltage overshoot, noise coupling, and EMI emission. Following the design recommendations in this data sheet will help mitigate the challenges caused by a high slew rate. The LMG352xR030-Q1 offers circuit designers the flexibility to select the proper slew rate for the best performance of their end equipment.

10.2.2.1.1 Start-Up and Slew Rate With Bootstrap High-Side Supply

Using a bootstrap supply introduces additional constraints on the start-up of the high-side LMG352xR030-Q1. Prior to powering up, the GaN device operates in cascode mode with reduced performance. In some circuits, a proper slew rate may be required for the start-up of a bootstrap-supplied half-bridge configuration.

10.2.2.2 Signal Level-Shifting

In half-bridges, high-voltage level shifters or digital isolators must be used to provide isolation for signal paths between the high-side device and control circuit. Using an isolator is optional for the low-side device. But, it will equalize propagation delays between the high-side and low-side signal path, and provide the ability to use different grounds for the GaN device and the controller. If an isolator is not used on the low-side device, the control ground and the power ground must be connected at the device and nowhere else on the board. See Section 12.1 for more information. With the fast-switching GaN device, common ground inductance could easily cause noise issues without the use of an isolator.

Choosing a digital isolator for level-shifting is important for improvement of noise immunity. As GaN device can easily create high dv/dt, >50 V/ns, in hard-switching applications, it is highly recommended to use isolators with high common-mode transient immunity (CMTI). Isolators with low CMTI can easily generate false signal, which could cause shoot-through. On the other hand, it is strongly encouraged to select isolators which are not edge-triggered. In an edge-triggered isolator, a high dv/dt event can cause the isolator to flip states and cause circuit malfunctioning.

Generally, ON/OFF keyed isolators are preferred, such as the TI ISO77xxF series, as a high CMTI event would only cause a very short false pulse, a few nanoseconds, which can be filtered out. To filter these false pulses, a low pass filter, like 1 kΩ and 22 pF R-C filter, is recommended to be placed at the driver input.

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10.2.2.3 Buck-Boost Converter Design

The buck-boost converter generates the negative voltage to turn off the direct-drive GaN device. While it is controlled internally, it requires an external power inductor and output capacitor. The converter is designed to use a 4.7-µH inductor and a 2.2-µF output capacitor.

As the peak current of the buck-boost is subject to two different peak current limits which are 0.4 A and 1 A for low and high frequencies (see Section 9.3.3), the inductor must have a saturation current well above the rated peak current limit. Once the higher limit is established at higher switching frequency, the current limit will not go down again even when GaN device is back to lower switching frequency. Therefore, it is critical to select the inductor according to maximum GaN switching frequency.

The buck-boost converter uses a peak current hysteretic control. As shown in Figure 10-2, the inductor current increases at the beginning of a switching cycle until the inductor reaches the peak current limit. The inductor current will go down to zero. The idle time between each current pulse is determined automatically by the output current, and can be reduced to zero. Therefore, the maximum output current happens when the idle time is zero, and is decided by the peak current but irrelevant to the inductor value.

A minimum inductance value of 3 µH is preferred for the buck-boost converter so that the di/dt across the inductor is not too high. This leaves enough margin for the control loop to respond. As a result, the maximum di/dt of the inductor is limited to 6 A/µs. On the other hand, large inductance also limits the transient response for stable output voltage, and it is preferred to have inductors less than 10 µH.

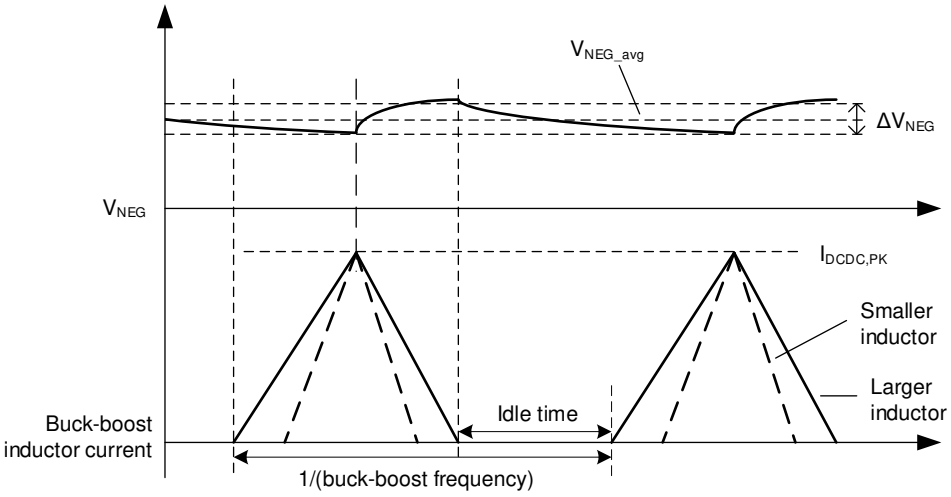

Figure 10-2. Buck-Boost Converter Inductor Current

10.3 Do's and Don'ts

The successful use of GaN devices in general and the LMG352xR030-Q1 in particular depends on proper use of the device. When using the LMG352xR030-Q1, **DO**:

- Read and fully understand the datasheet, including the application notes and layout recommendations.
- Use a four-layer board and place the return power path on an inner layer to minimize power-loop inductance.
- Use small, surface-mount bypass and bus capacitors to minimize parasitic inductance.
- Use the proper size decoupling capacitors and locate them close to the IC as described in Section 12.1.
- Use a signal isolator to supply the input signal for the low-side device. If not, ensure the signal source is connected to the signal GND plane which is tied to the power source **only** at the LMG352xR030-Q1 IC.
- Use the $\overline{\text{FAULT}}$ pin to determine power-up state and to detect overcurrent and overtemperature events and safely shut off the converter.

To avoid issues in your system when using the LMG352xR030-Q1, **DON'T**:

- Use a single-layer or two-layer PCB for the LMG352xR030-Q1 as the power-loop and bypass capacitor inductances will be excessive and prevent proper operation of the IC.
- Reduce the bypass capacitor values below the recommended values.
- Allow the device to experience drain transients above 600 V as they may damage the device.
- Allow significant third-quadrant conduction when the device is OFF or unpowered, which may cause overheating. Self-protection feature cannot protect the device in this mode of operation.
- Ignore the $\overline{\text{FAULT}}$ pin output.

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11 Power Supply Recommendations

The LMG352xR030-Q1 only requires an unregulated 12-V supply. The low-side supply can be obtained from the local controller supply. The supply of the high-side device must come from an isolated supply or a bootstrap supply.

11.1 Using an Isolated Power Supply

Using an isolated power supply to power the high-side device has the advantage that it will work regardless of continued power-stage switching or duty cycle. It can also power the high-side device before power-stage switching begins, eliminating the power-loss concern of switching with an unpowered LMG352xR030-Q1 (see Section 10.2.2.1.1 for details). Finally, a properly-selected isolated supply will introduce less parasitics and reduce noise coupling.

The isolated supply can be obtained with a push-pull converter, a flyback converter, a FlyBuck™ converter, or an isolated power module. When using an unregulated supply, the input of LMG352xR030-Q1 should not exceed the maximum supply voltage. A 16-V TVS diode could be used to clamp the VDD voltage of LMG352xR030-Q1. Minimizing the inter-winding capacitance of the isolated power supply or transformer is necessary to reduce switching loss in hard-switched applications.

11.2 Using a Bootstrap Diode

In half-bridge configuration, a floating supply is necessary for the high-side device. To obtain the best performance of LMG352xR030-Q1, Section 11.1 is highly recommended. A bootstrap supply can be used with the recommendations of this section.

11.2.1 Diode Selection

The LMG352xR030-Q1 offers no reverse-recovery charge and very limited output charge. Hard-switching circuits using the LMG352xR030-Q1 also exhibit high voltage slew rates. A compatible bootstrap diode should not introduce high output charge and reverse-recovery charge.

A silicon carbide diode, like the GB01SLT06-214, can be used to avoid reverse-recovery effects. The SiC diode has an output charge of 3 nC. Althought there is additional loss from its output charge, it does not dominate the losses of the switching stage.

11.2.2 Managing the Bootstrap Voltage

In a synchronous buck or other converter where the low-side switch occasionally operates in third-quadrant, the bootstrap supply charges through a path that includes the third-quadrant voltage drop of the low-side LMG352xR030-Q1 during the dead time as shown in Figure 11-1. This third-quadrant drop can be large, which may over-charge the bootstrap supply in certain conditions. The V_{DD} supply of LMG352xR030-Q1 must be kept below 18 V.

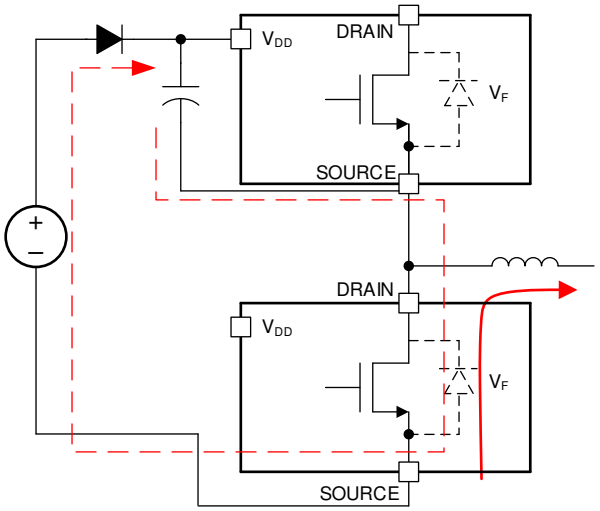

Figure 11-1. Charging Path for Bootstrap Diode

As shown in Figure 11-2, the recommended bootstrap supply includes a bootstrap diode, a series resistor, and a 16-V TVS or zener diode in parallel with the V_{DD} bypass capacitor to prevent damaging the high-side LMG352xR030-Q1. The series resistor limits the charging current at start-up. and when the low-side device is operating in third-quadrant mode. This resistor must be selected to allow sufficient current to power the LMG352xR030-Q1 at the desired operating frequency. At 100-kHz operation, a value of approximately 2 Ω is recommended. At higher frequencies, this resistor value should be reduced or the resistor omitted entirely to ensure sufficient supply current.

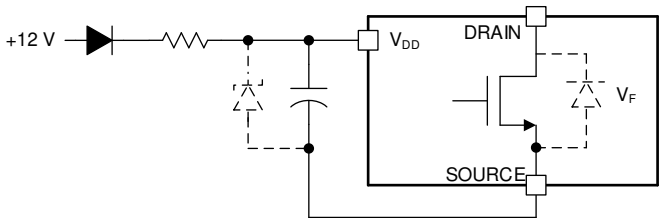

Figure 11-2. Suggested Bootstrap Regulation Circuit

ADVANCE INFORMATION

12 Layout

12.1 Layout Guidelines

The layout of the LMG352xR030-Q1 is critical to its performance and functionality. Because the half-bridge configuration is typically used with these GaN devices, layout recommendations will be considered with this configuration. A four-layer or higher layer count board is required to reduce the parasitic inductances of the layout to achieve suitable performance.

12.1.1 Power Loop Inductance

The power loop, comprising the two devices in the half bridge and the high-voltage bus capacitance, undergoes high *di/dt* during switching events. By minimizing the inductance of this loop, ringing and electro-magnetic interference (EMI) can be reduced, as well as reducing voltage stress on the devices.

Place the power devices as close as possible to minimize the power loop inductance. The decoupling capacitors are positioned in line with the two devices. They can be placed close to either device. In Section 12.2, the devices are placed on the bottom layer and the decoupling capacitors are placed on top layer. The PGND is placed on top layer, the HVBUS is located on top and third layer, and the switching node is on top layer. They are connected to the power devices on bottom layer with vias. Area of traces close to the devices are minimized at bottom layer in order to keep clearance between heatsink and conductors.

12.1.2 Signal Ground Connection

The LMG352xR030-Q1's SOURCE pins are internally connected to the power IC signal ground. The return path for the passives associated to the driver (for example, bypass capacitance) must be connected to the SOURCE pins. Local signal ground planes should be connected to SOURCE pins with low impedance star connection. In Section 12.2, local signal ground planes are located on third layer to act as the return path for the local circuitry, and connected to the SOURCE pins with vias between the third layer and the bottom layer.

12.1.3 Bypass Capacitors

The gate drive loop impedance must be minimized to obtain good performance. Although the gate driver is integrated on package, the bypass capacitance for the driver is placed externally. As the GaN device is turned off to a negative voltage, the impedance of the path to the external VNEG capacitor is included in the gate drive loop. The VNEG capacitor must be placed close to VNEG and SOURCE pins. In the Section 12.2, the bypass capacitors , C3 and C13, are located at top layer and connected to VNEG pins with vias and SOURCE pins through local signal ground plane.

The bypass capacitors for the input supply , C1 and C11, and the 5-V regulator , C2 and C12, must also be placed close to the power IC with low impedance connections.

12.1.4 Switch-Node Capacitance

GaN devices have very low output capacitance and switch quickly with a high *dv/dt*, yielding very low switching loss. To preserve this low switching loss, additional capacitance added to the output node must be minimized. The PCB capacitance at the switch node can be minimized by following these guidelines:

- Minimize overlap between the switch-node plane and other power and ground planes.
- Thin the GND return path under the high-side device somewhat while still maintaining a low-inductance path.
- Choose high-side isolator ICs and bootstrap diodes with low capacitance.
- Place the power inductor as close to the GaN device as possible.
- Power inductors should be constructed with a single-layer winding to minimize intra-winding capacitance.
- If a single-layer inductor is not possible, consider placing a small inductor between the primary inductor and the GaN device to effectively shield the GaN device from the additional capacitance.
- If a back-side heat-sink is used, restrict the switch-node copper coverage on the bottom copper layer to the minimum area necessary to extract the needed heat.

12.1.5 Signal Integrity

The control signals to the LMG352xR030-Q1 must be protected from the high *dv/dt* caused by fast switching. Coupling between the control signals and the drain may cause circuit instability and potential destruction. Route

the control signals (IN, $\overline{\text{FAULT}}$ and $\overline{\text{OC}}$) over a ground plane placed on an adjacent layer. In Section 12.2, for example, all the signals are routed on layers close to the local signal ground plane.

Capacitive coupling between the traces for the high-side device and the static planes, such as PGND and HVBUS, could cause common mode current and ground bounce. The coupling can be mitigated by reducing overlap between the high-side traces and the static planes. For the high-side level shifter, ensure no copper from either the input or output side extends beneath the isolator or the CMTI of the device may be compromised.

12.1.6 High-Voltage Spacing

Circuits using the LMG352xR030-Q1 involve high voltage, potentially up to 650V. When laying out circuits using the LMG352xR030-Q1, understand the creepage and clearance requirements for the application and how they apply to the GaN device. Functional (or working) isolation is required between the source and drain of each transistor, and between the high-voltage power supply and ground. Functional isolation or perhaps stronger isolation (such as reinforced isolation) may be required between the input circuitry to the LMG352xR030-Q1 and the power controller. Choose signal isolators and PCB spacing (creepage and clearance) distances which meet your isolation requirements.

If a heat sink is used to manage thermal dissipation of the LMG352xR030-Q1, ensure necessary electrical isolation and mechanical spacing is maintained between the heat sink and the PCB.

12.1.7 Thermal Recommendations

The LMG352xR030-Q1 is a lateral device grown on a Si substrate. The thermal pad is connected to the source of device. The LMG352xR030-Q1 may be used in applications with significant power dissipation, for example, hard-switched power converters. In these converter, TI recommends a heat sink connected to the top side of LMG352xR030-Q1. The heat sink can be applied with thermal interface materials (TIMs), like thermal pad with electrical isolation.

Refer to the *High Voltage Half Bridge Design Guide for LMG3410 Smart GaN FET* application note for more recommendations and performance data on thermal layouts.

ADVANCE INFORMATION

12.2 Layout Examples

Correct layout of the LMG352xR030-Q1 and its surrounding components is essential for correct operation. The layouts shown here reflect the GaN device schematic in Figure 10-1. These layouts are shown to produce good results and is intended as a guideline. However, it may be possible to obtain acceptable performance with alternate layout schemes. On the other hand, please refer to land pattern example in Section 14 for the latest recommended PCB footprint of device.

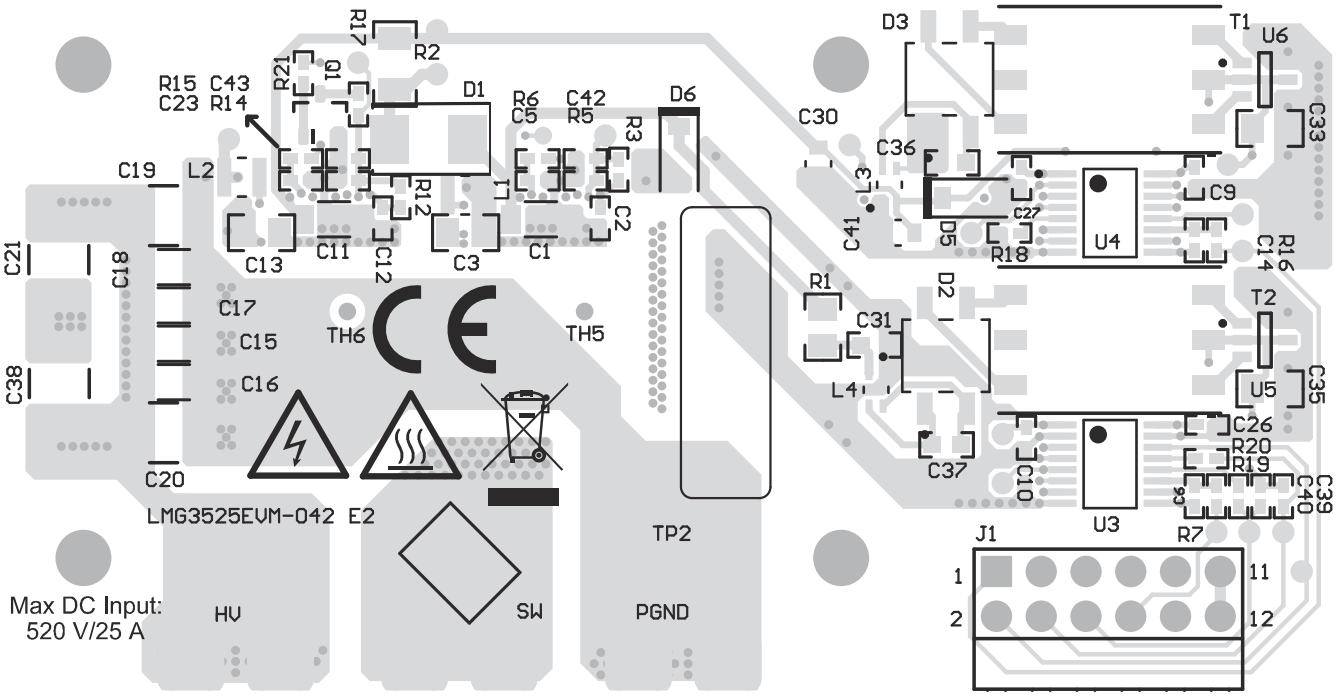

Figure 12-1. Half-Bridge Top Layer Layout

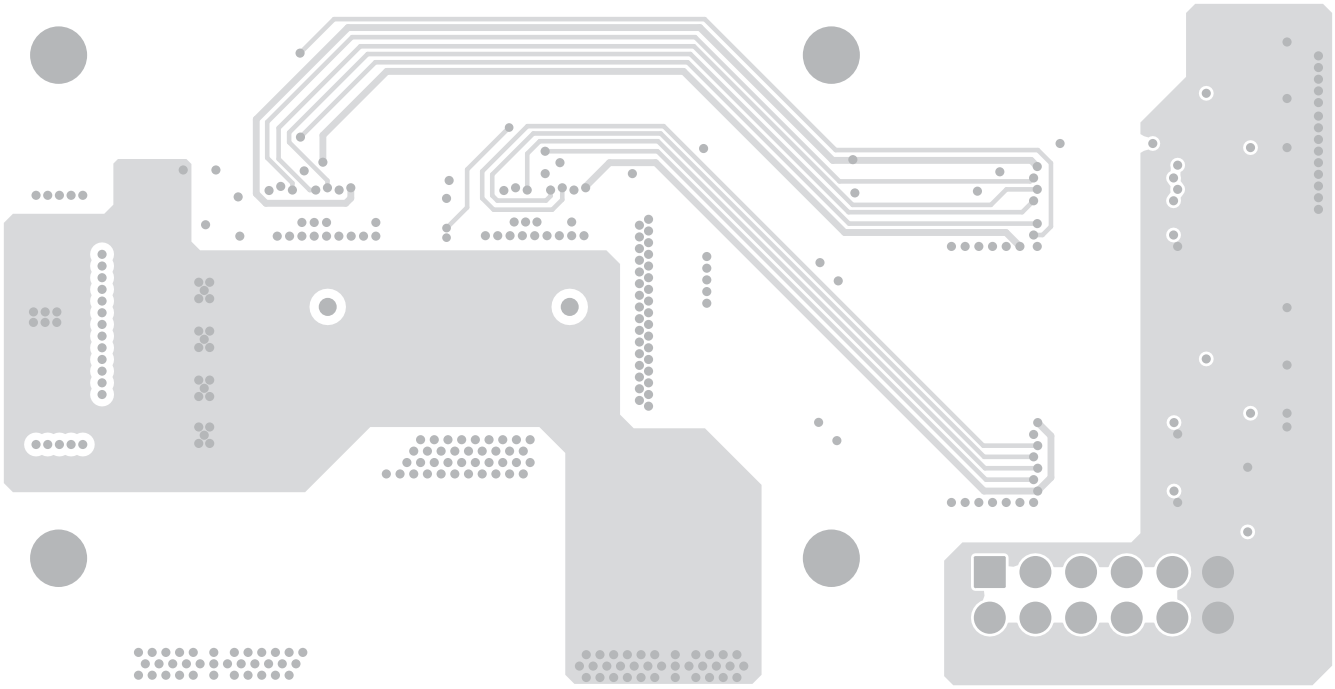

Figure 12-2. Half-Bridge Second Layer Layout

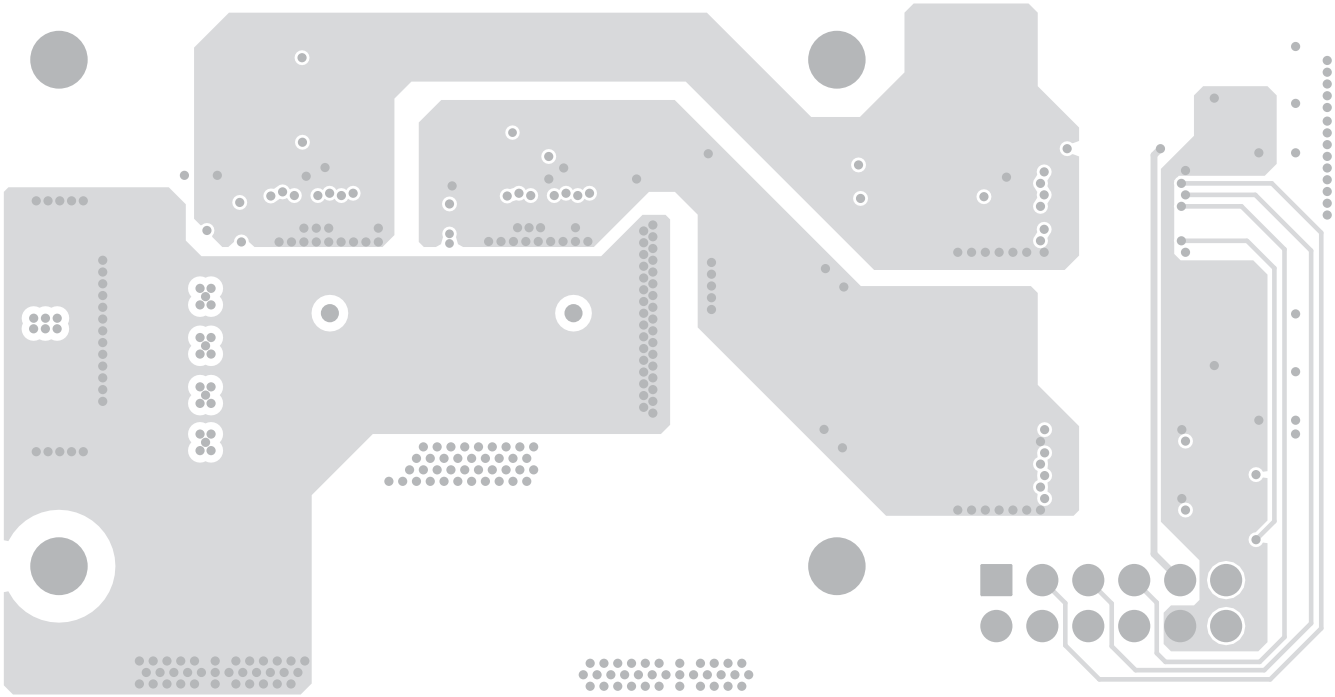

Figure 12-3. Half-Bridge Third Layer Layout

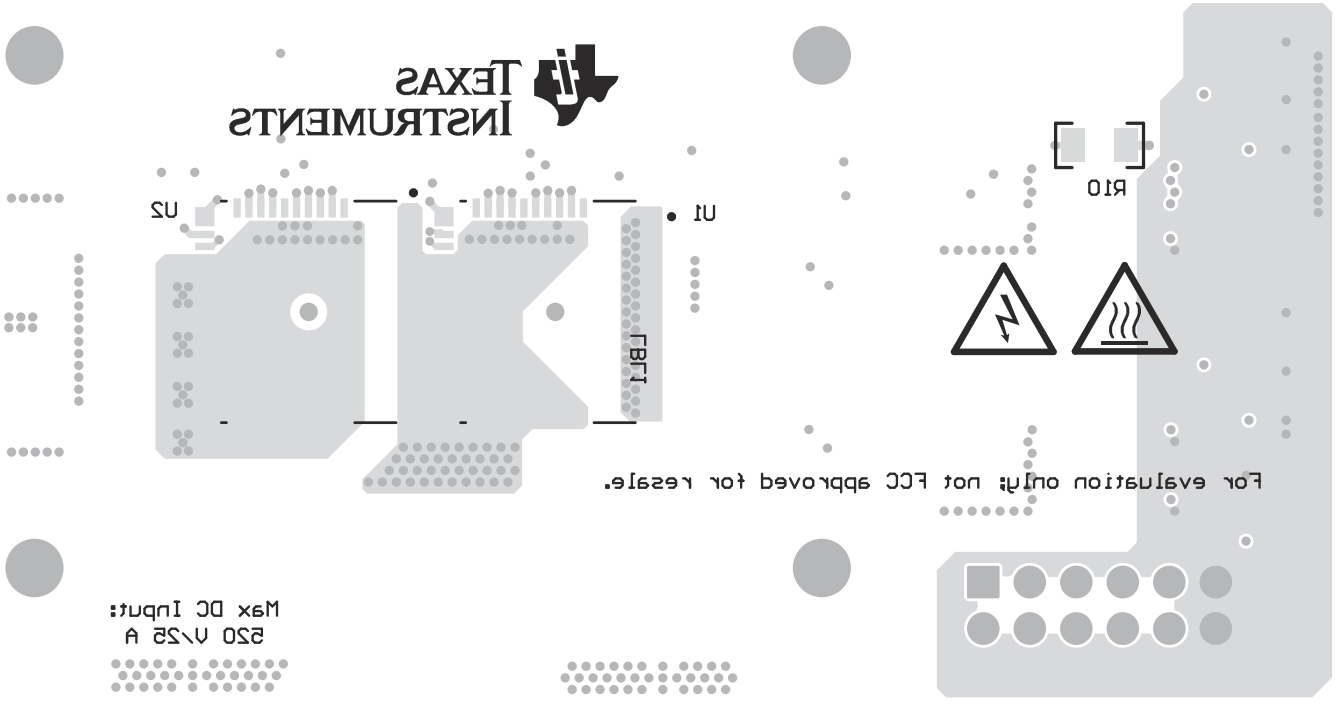

Figure 12-4. Half-Bridge Bottom Layer Layout

ADVANCE INFORMATION

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

High Voltage Half Bridge Design Guide for LMG3410 Smart GaN FET application note.

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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13.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

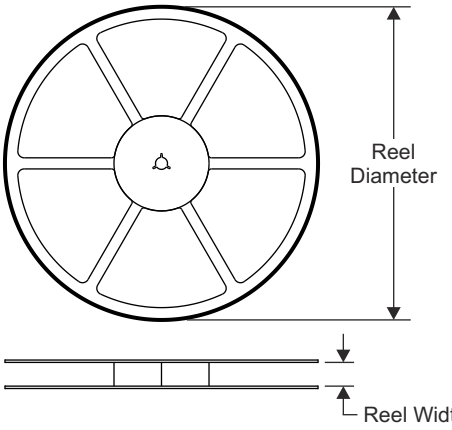
14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

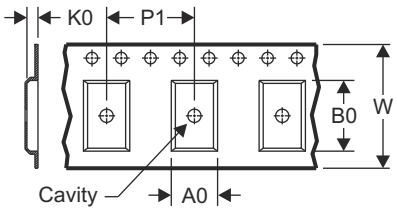
ADVANCE INFORMATION

14.1 Tape and Reel Information

REEL DIMENSIONS

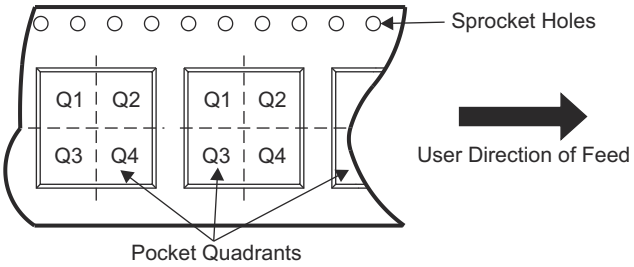


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

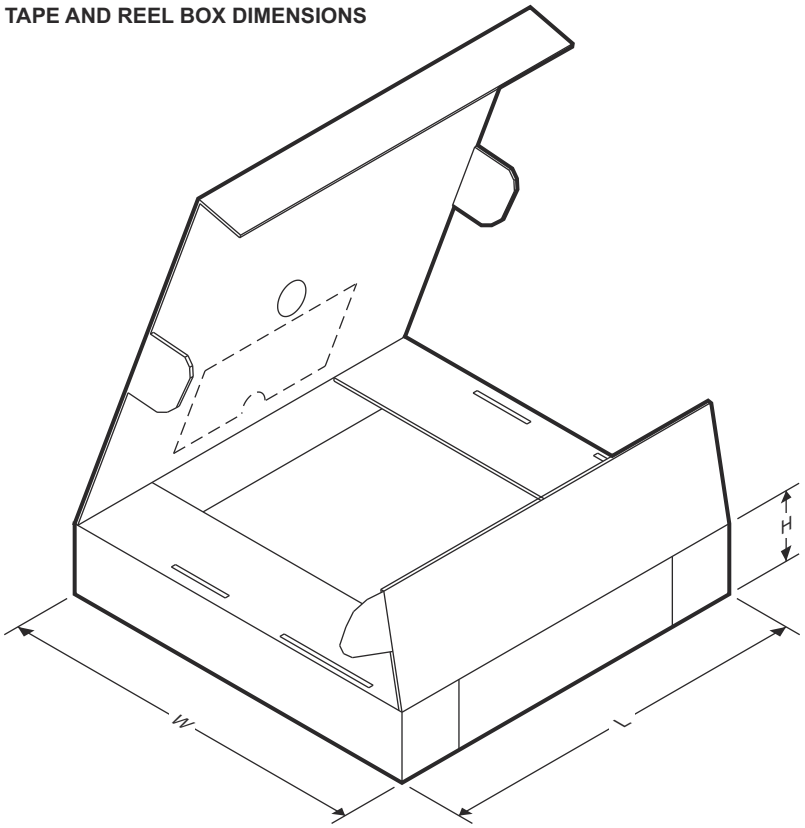


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XMG3522R030QRQST Q1	VQFN	RQS	52	250	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI	Q1
XMG3525R030QRQST Q1	VQFN	RQS	52	250	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI	Q1

ADVANCE INFORMATION

ADVANCE INFORMATION

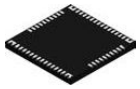
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XMG3522R030QRQSTQ1	VQFN	RQS	52	250	12	12	0.9
XMG3525R030QRQSTQ1	VQFN	RQS	52	250	12	12	0.9

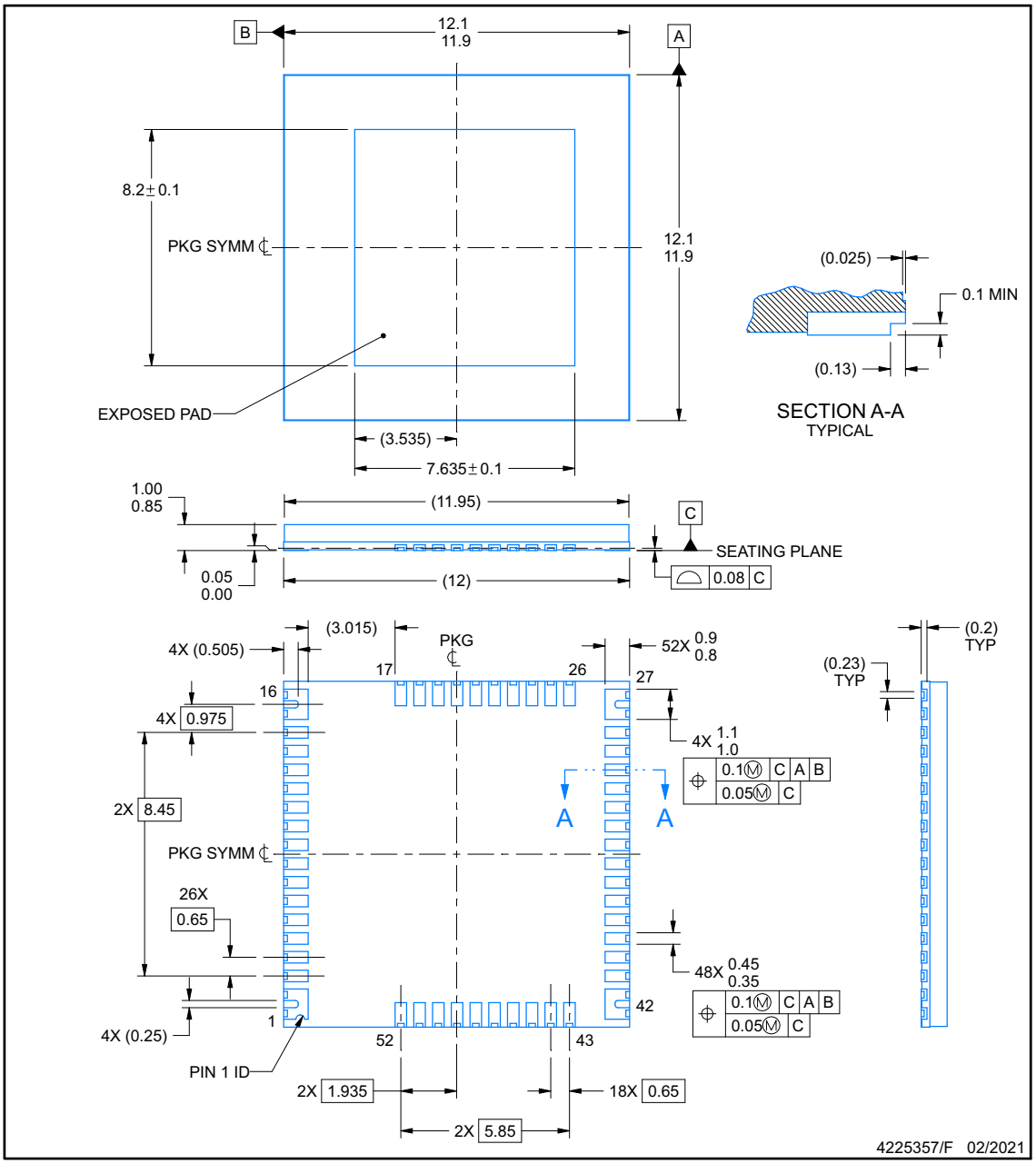
PACKAGE OUTLINE

RQS0052A



VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

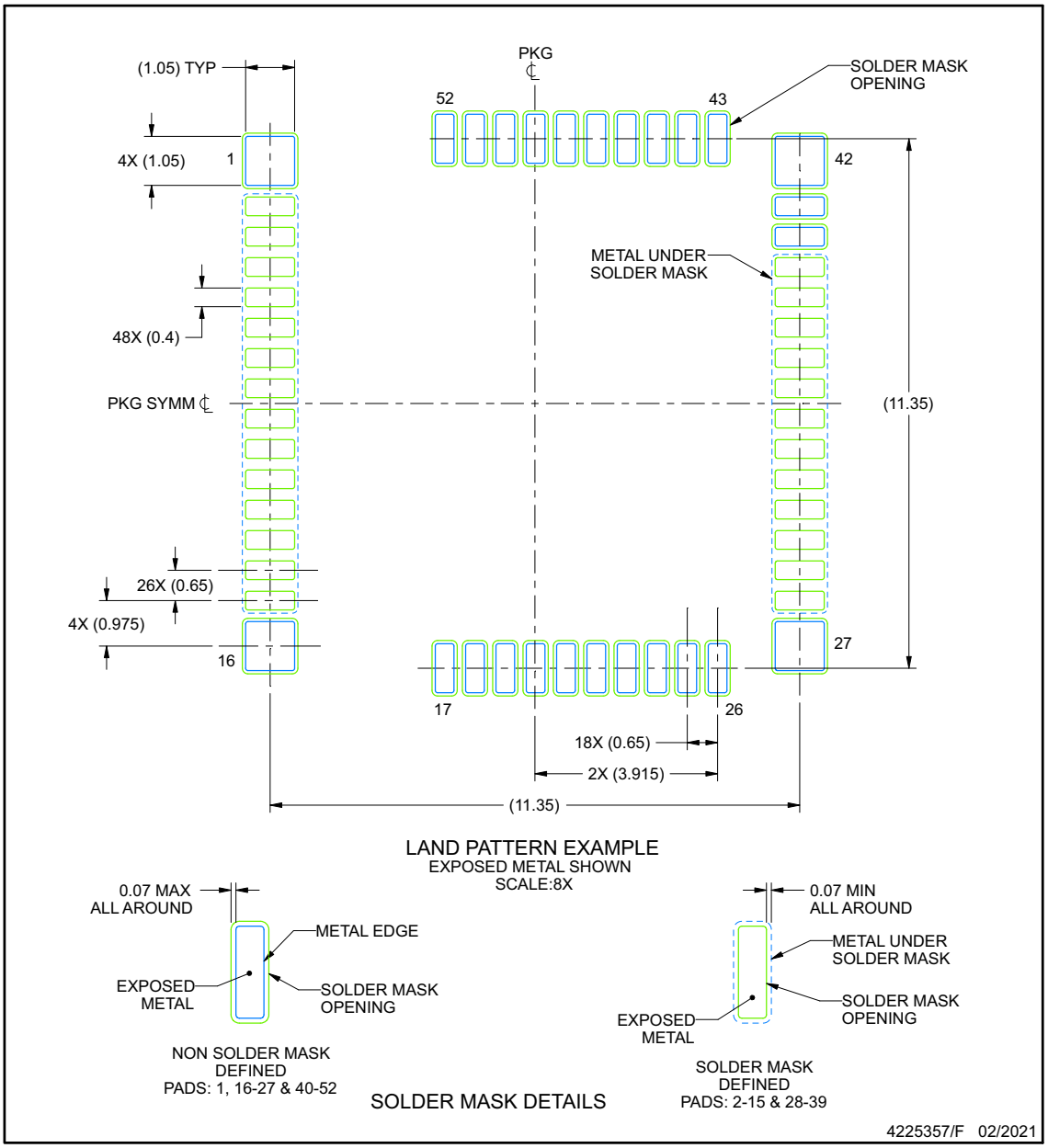
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package incorporates an exposed thermal pad that is designed to be attached directly to an external heat sink. This optimizes the heat transfer from the integrated circuit (IC).

ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

RQS0052A — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



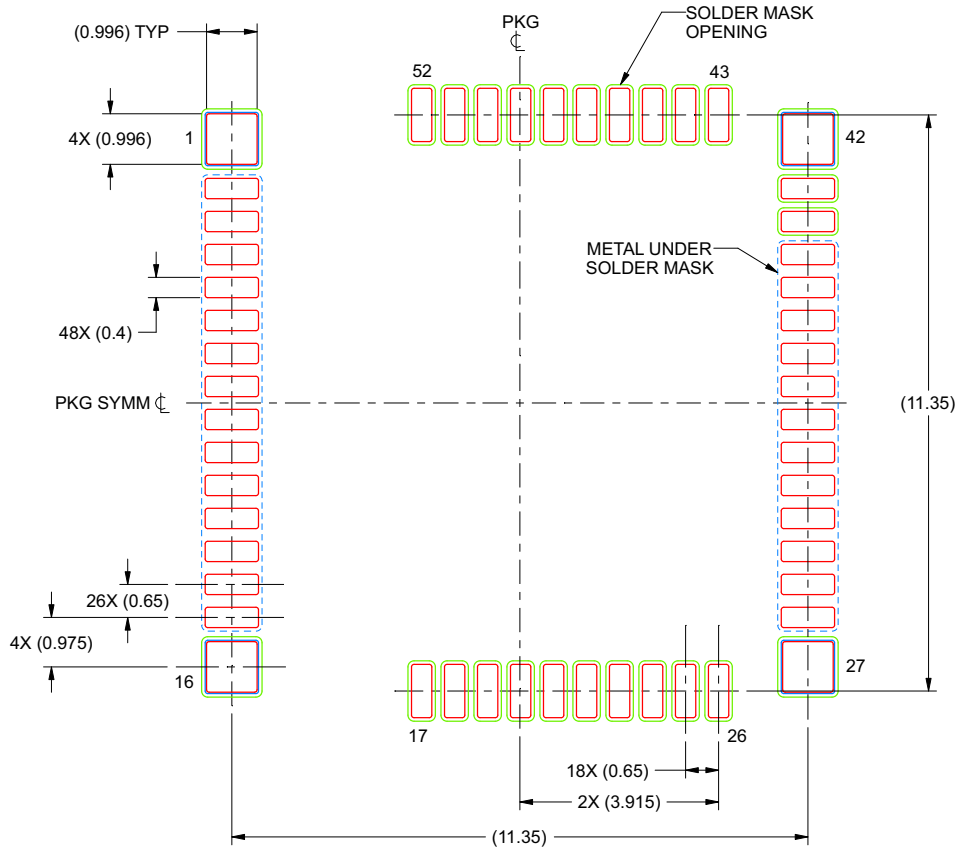
NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RQS0052A — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 1, 16, 27 & 42: 90%
SCALE:8X

4225357/F 02/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XMG3522R030QRQSTQ1	ACTIVE	VQFN	RQS	52	250	TBD	Call TI	Call TI	-40 to 150		Samples
XMG3525R030QRQSTQ1	ACTIVE	VQFN	RQS	52	250	TBD	Call TI	Call TI	-40 to 150		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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