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LMH0394,LMH0395**

*High-Speed Board Layout Challenges in FPGA/SDI Sub-Systems*



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## High-Speed Board Layout Challenges in FPGA/SDI Sub-Systems

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### Introduction

Television and cinema have entered the digital age. Video pictures are used to transport at standard definition rate (270 Mb/s), upgraded to high definition rate (1.485 Gb/s), and are now migrating to 3 Gb/s. The migration to higher speeds enables higher resolution images for entertainment, but it also presents challenges to hardware engineers and physical layout designers. Many video systems are implemented with feature-rich FPGA and multi-rate SDI integrated circuits that support high performance professional video transport over long distances. FPGAs demand high density routing with fine trace width while high-speed analog SDI routing demands impedance matching and signal fidelity. This paper outlines the layout challenges facing hardware engineers and provides recommendations for dealing with these challenges.

### FPGA/SDI Sub-Systems

In a typical FPGA/SDI board, digital video signals are routed between BNC connectors and high-performance

SDI analog integrated circuits with  $75\Omega$  traces. The interconnection between the FPGA and the SDI integrated circuits consists of several pairs of  $100\Omega$  differential signals routed through the fine pitch ball grid of the FPGA. One of the layout challenges is the co-existence of the  $75\Omega$  single-ended trace and the  $100\Omega$  differential traces. Very often, both types of traces are routed on the top layer where the components reside. Trace widths good for  $75\Omega$  may be too wide for running  $100\Omega$  traces. *Figure 1* is a simplified block diagram of a FPGA/SDI board showing the  $75\Omega$  and the  $100\Omega$  domains.

### SDI Layout Challenge

The Society of Motion Pictures and Television Engineers (SMPTE) publishes standards that govern the transport of digital video over coaxial cables. The signal amplitude is specified at  $800\text{ mV} \pm 10\%$ . This amplitude requirement must be met with an off-chip precision termination resistor of  $75\Omega \pm 1\%$ . The SMPTE standards<sup>1</sup> also include input and output return loss requirements which basically specify how well the input or output port resembles a

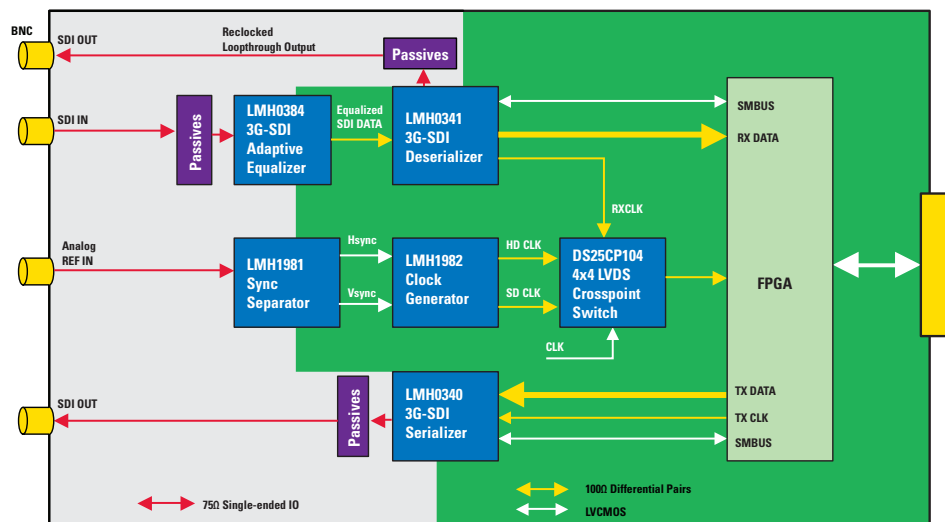


Figure 1. Typical FPGA/SDI Block Diagram

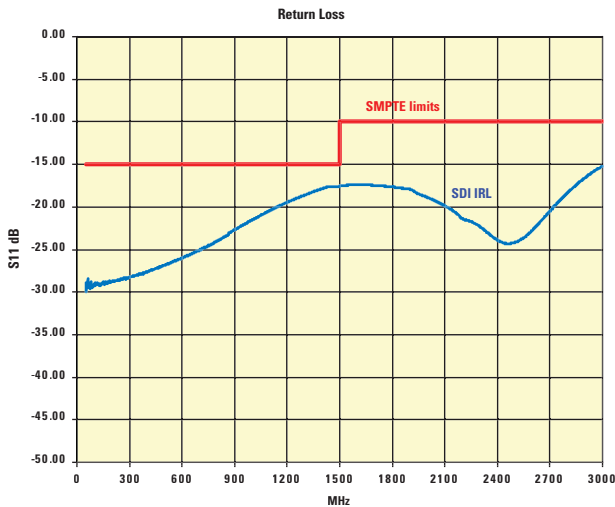


Figure 2. Plot of Input Return Loss of an SDI Port and SMPTE Limits

75Ω network. *Figure 2* shows the SMPTE requirements on return loss specifications.

An off-chip impedance balance network, consisting of an inductor and a shunt resistor, is commonly used to counteract the input or output capacitance of a SDI integrated circuit. A large AC coupling capacitor (4.7 μF) is typically used in transporting SDI serial bit stream to avoid low frequency DC wander. As seen in *Figure 3*, there are several off-chip passive components hanging on the 75Ω trace between a SDI integrated circuit and its BNC connector. Each component introduces series parasitic inductance and each

component pad introduces shunt parasitic capacitance that impact the overall impedance matching to 75Ω. The SDI layout challenge is to find a way to minimize the impedance mismatches from the many external passive components at the 75Ω SDI port.

### Choosing Board Stack-up for FPGA/SDI Sub-Systems

What trace width should be used? At SDI speeds less than 3 Gb/s, copper loss is small and is not a great concern in choosing the trace width. It is more important to choose a trace width slightly smaller than the component landing pad with the goal to minimize impedance mismatches. A passive component of 0402-size requires a landing pad of about 20 mils x 25 mils, so a trace width of about 15 mils to 20 mils is optimal for the 75Ω SDI traces.

For ease of routing and skew matching, the 100Ω differential signals of the FPGA are routed with finer trace width. Loosely coupled traces are commonly used to avoid the bigger impedance changes when tightly coupled traces branch out to termination resistors or AC coupling capacitors.

A board stack-up that works well for both the FPGA and the SDI signal routings is shown in *Figure 4*. In this stack-up, the SDI signal traces are implemented with 75Ω single-end microstrips referenced to GND2 at layer 4. GND2 is a metal island carved out in the signal layer 4. The metal in layer 2 and 3 (GND1 and VCC planes) are removed in the region of the 75Ω traces so they do not lower the traces' characteristic impedance. The 100Ω differential traces of the FPGA are loose-coupled microstrips referenced to GND1

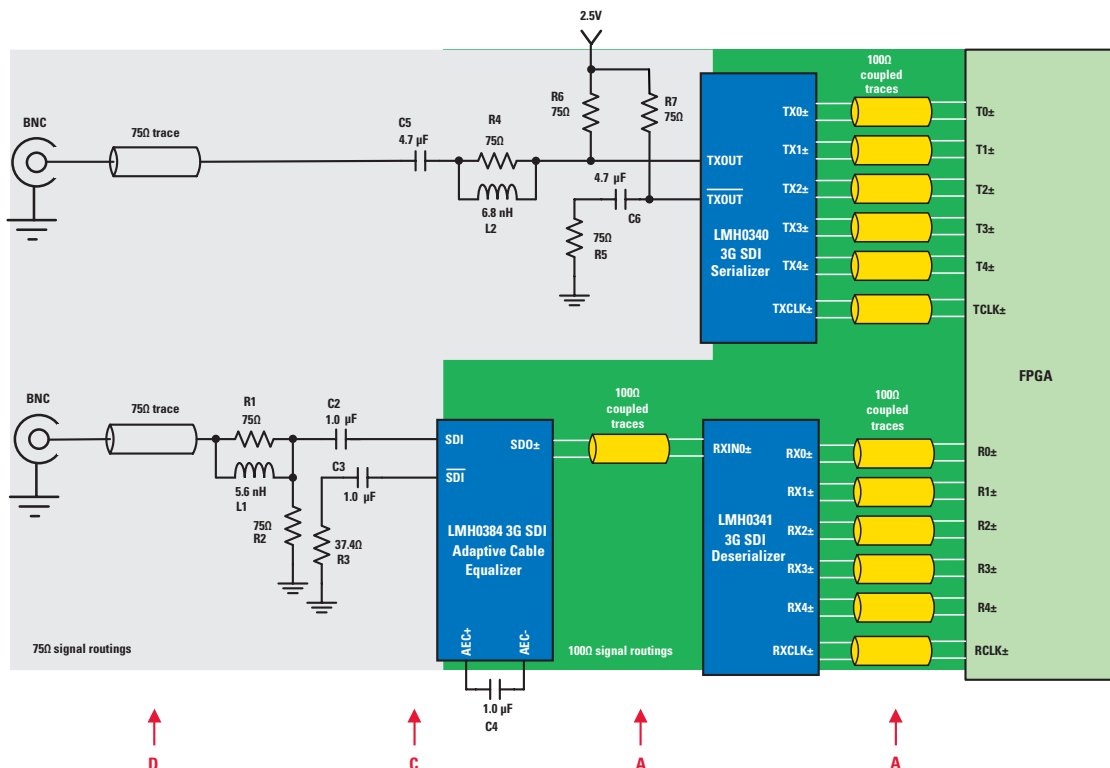


Figure 3. A Typical SDI Circuit (showing high-speed signal paths only)

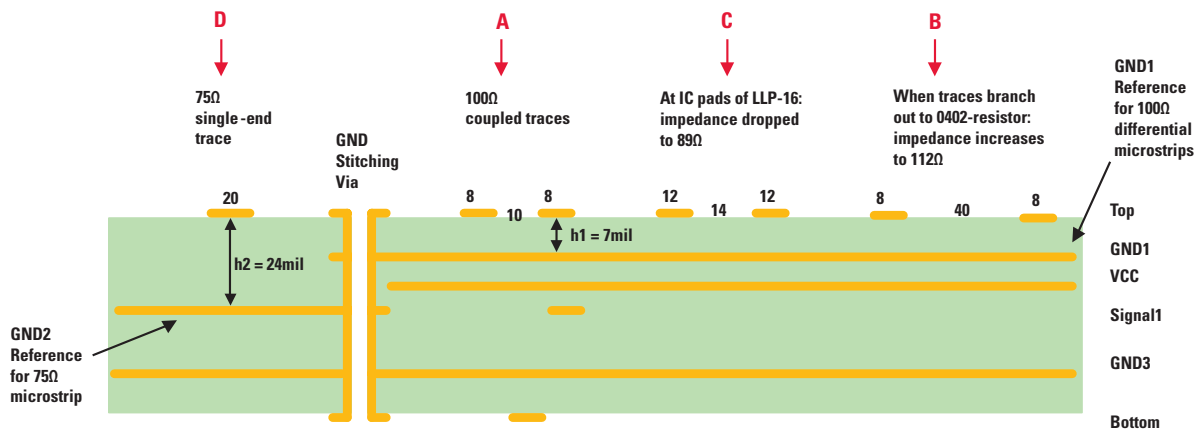


Figure 4. Board Stack-up with Separate Ground References for 75Ω and 100Ω Traces

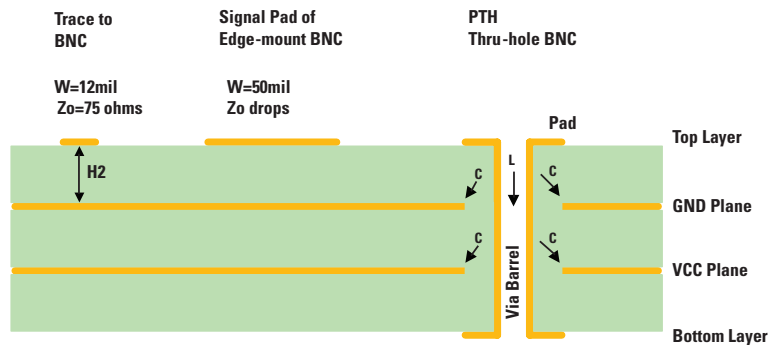


Figure 5. Cross-Sectional Diagram of BNC Footprints

at layer 2. The two ground references (GND1 and GND2) are electrically connected together through ground stitching plated-through holes. This board stack-up arrangement allows the freedom to choose the trace width for the 75Ω traces by adjusting the dielectric distance  $h_2$ , and the trace width for the 100Ω traces by adjusting  $h_1$ .

### Don't Forget the BNC Connector Footprint

A common problem in many SDI boards is the use of non-optimized BNC connector footprints that introduce severe impedance mismatches, failing to meet the return loss requirement and impairing the signal fidelity of the equipment. *Figure 5* illustrates the cross-section of a board with a 12-mil wide microstrip connected to a 50-mil wide pad of an edge-mount BNC. The ground plane is placed at a dielectric distance below the top trace to achieve the target trace impedance. The connector's landing pad is a wide microstrip; therefore the characteristic impedance of the pad is significantly lower than the trace impedance. The pad introduces a severe impedance drop that impacts return loss and limits the trace's transmission bandwidth.

*Figure 5* also illustrates the cross-section of a through-hole BNC footprint. The inner ground and power planes are isolated from the plated-through hole to avoid

short-circuit. The cylindrical barrel introduces a certain amount of inductance. Each ground or power plane introduces parasitic capacitance to the plated-through hole. A large plated-through hole with a small clearance will exhibit excessive capacitance that results in a big drop in impedance. *Figure 6* shows the impedance profile of a poorly designed through-hole BNC with a 60-mil hole and 20-mil clearance. It illustrates the impedance of the plated-through-hole drops to 40Ω from the 75Ω trace.

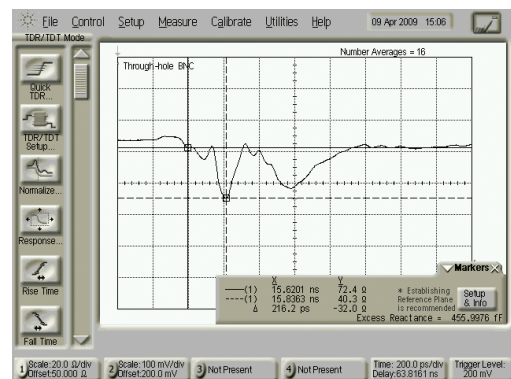


Figure 6. Impedance Profile of a Poorly Designed Through-Hole BNC

## Designing Good BNC Footprints

The objective of designing a good BNC footprint is to avoid excessive impedance mismatches between the footprint and the trace connected to the footprint. It is useful to walk through the signal path and look for the possible impedance mismatches caused by board structure changes. A time domain reflectometer is an instrument capable to identify where the impedance mismatches occur. An electromagnetic simulator can be used to inspect impedance changes during board layout design. If the impedance is too low, design a board structure to shave off excess capacitance. If the impedance is too high, add a bit of extra parasitic capacitance to bring the impedance closer to the target<sup>3</sup>. With the right amount of inductance and capacitance, it is possible to create a through-hole BNC footprint with the desired characteristic impedance. *Figure 7* illustrates an example of a carefully designed through-hole BNC footprint and *Figure 8* illustrates the impedance of this footprint being quite close to the 75Ω target.

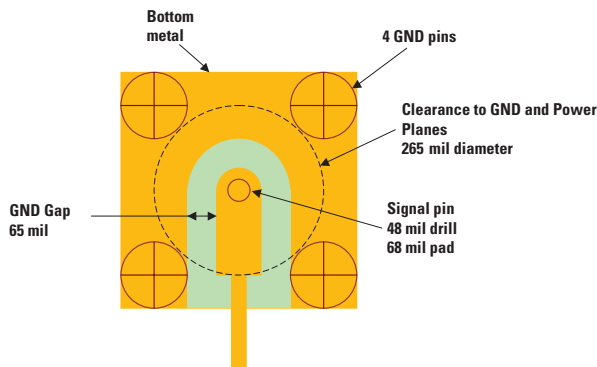


Figure 7. Top View of a Good Through-Hole BNC Footprint

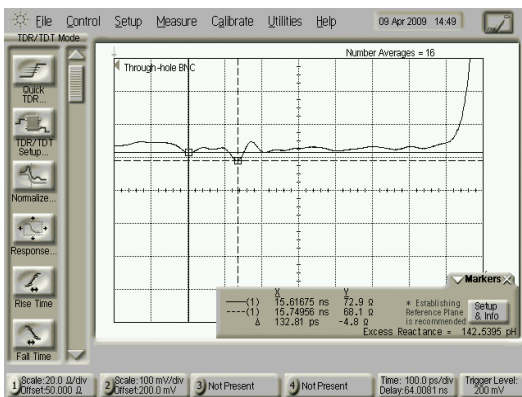


Figure 8. Impedance Profile of a Good Through-Hole BNC Footprint

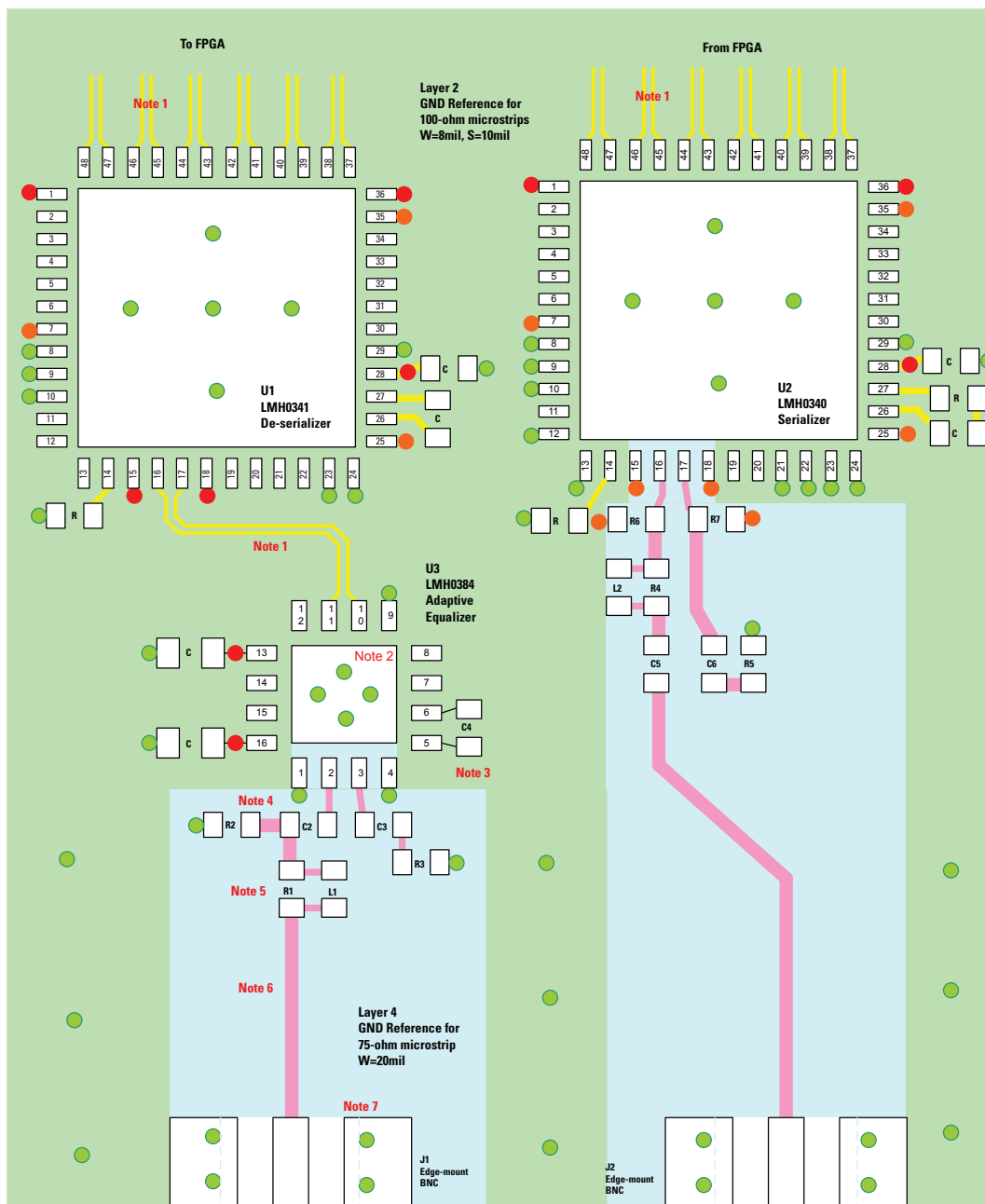
## Layout Guidelines for FPGA/SDI Boards

For FPGA/SDI boards, the data rates are less than 3 Gb/s, and signal transition times are about 100 picoseconds. The challenge in SDI board layout is not in speed, but in devising a layout strategy to minimize the impedance mismatches from the many external components on the 75Ω SDI port, designing a controlled impedance footprint for the large BNC connector, and implementing a board stack-up that supports both 75Ω and 100Ω traces. These challenges can be met by following a few simple layout guidelines:

- Set trace impedances to 75Ω±10%, 100Ω±10%
- Use the smallest size surface mount components and the smallest size landing pads for the passive components
- Select trace widths that minimize impedance mismatches along the signal path
- Select a board stack-up that supports both 75Ω single-end traces and 100Ω loosely coupled differential traces with separate ground references
- Use surface mount ceramic capacitors and RF signal inductors
- Place components that impact return loss (termination resistor, impedance balance network) closest to IC pins
- Use well-designed BNC footprints with 75Ω controlled impedance
- Maintain symmetry on the complimentary signal routings
- Route 100Ω differential traces uniformly (keep trace widths and trace spacing uniform along the trace)
- Avoid sharp bends; use 45-degree bends
- Walk along the signal path, identify geometry changes and estimate their corresponding impedance changes
- Use solid planes. If ground relief is needed to shave off excess parasitic capacitance, use with care; consult a 3D simulation tool to guide layout decisions
- Use the shortest path for VCC and ground connections; connect pin to plane with vias

## Layout Example - National's LMH0384 Equalizer and LMH0340/0341 Serializer/De-serializer

*Figure 9* is a conceptual layout diagram of National's LMH0384 3 Gbps/HD/SD SDI adaptive cable equalizer, LMH0341 SDI de-serializer, LMH0340 SDI serializer and a FPGA (not shown). The stack-up shown in *Figure 4* is used in this example. Layer 2 (shown in green) is the ground reference for the 8-mil wide 100Ω differential trace that goes to the output pins SDO+ and SDO- of the LMH0384, as well as the LVDS signal routings for the LMH0340 and LMH0341. An island of metal on layer 4 (shown in blue) is used as the ground plane for the 75Ω traces. The two ground references are stitched together using the ground via for the device's DAP connection.



- Note 1 – Use coupled traces with 100Ω differential impedance referenced to Layer 2.
- Note 2 – GND stitch for Layer 2 and Layer 4
- Note 3 – C4 placed close IC pins.
- Note 4 – C2 placed closest to IC input pin; R2 75Ω receive termination placed after C2.
- Note 5 – L1, R1 impedance matching network placed close to SDI+ pin through C2.
- Note 6 – Use 75Ω controlled impedance trace referenced to Layer 4. Use 0402 components. Use trace width of 15-25 mils to minimize impedance drop caused by larger component pads.
- Note 7 – Use 75Ω controlled impedance footprint for BNC.

Figure 9. Layout Example for the LMH0384, LMH0340 and LMH0341

The AC coupling capacitor C2 is placed closest to the input pin at SDI+. The impedance matching network L1 and R1 are placed as close as possible to the input pin SDI+ through C2. The 75Ω termination resistor R2 is placed after C2 to minimize the effect of the stud.

This design uses 0402-size components to minimize the impedance change to the 75Ω trace built with 20-mil microstrip referenced to layer 4. The footprint used for the BNC should have good signal launch for achieving good return loss.

### Summary

The challenge in SDI board layout is in devising a layout strategy to minimize impedance mismatches from the many external components on the 75Ω port. Use of 75Ω microstrips with trace widths comparable to the landing pads of the passive components will minimize impedance discontinuities. A second ground reference allows the freedom to choose finer trace widths for the 100Ω differential traces that route to the high pin-count FPGA. Always use well designed BNC footprints with 75Ω controlled impedance. It is recommended to walk along the signal

paths, look for impedance changes due to the change of layout structures, and devise a way to shave off the excess inductance or capacitance in order to maintain the target characteristic impedance. By following a few simple layout guidelines, it is possible to design a board to meet SDI requirements with high signal fidelity and achieve high-density routing to the FPGA.

### Reference

1. The Society of Motion Pictures and Television Engineers publishes many SMPTE standards on the serial digital video interface. Some of these standards are:
  - SMPTE 259M-2006: SDTV Digital Signal/Data – Serial Digital Interface
  - SMPTE 292M-1998: Bit Serial Digital Interface for High Definition Television Systems
  - SMPTE 424M-2006: 3Gb/s Signal/Data Serial Interface
2. Datasheets of LMH0384, LMH0340, LMH0341 and many other SDI devices can be found at [www.national.com/analog/interface/sdi/](http://www.national.com/analog/interface/sdi/)
3. Getting Signal Launch Right for High-Speed Sub-Systems by Tsun-Kit Chin. It can be found in [http://www.national.com/analog/interface/sdi\\_technical\\_archive](http://www.national.com/analog/interface/sdi_technical_archive)

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