LMH0074 SMPTE 259M / 344M Adaptive Cable Equalizer

Check for Samples: LMH0074

FEATURES

- **SMPTE 259M and SMPTE 344M Compliant**
- **Supports DVB-ASI at 270 Mbps**
- **Data Rates: 125 Mbps to 540 Mbps**
- **Equalizes up to 400 Meters of Belden 1694A at 270 Mbps**
- **Manual Bypass and Output Mute with a Programmable Threshold**
- **Single-Ended or Differential Input**
- **50Ω Differential Outputs**
- **Single 3.3V Supply Operation**
- **Industrial Temperature Range: −40°C to +85°C**
- **208mW Typical Power Consumption with 3.3V Supply**
- **Footprint Compatible with the LMH0044 and the GS9074A**

APPLICATIONS

- **SMPTE 259M and SMPTE 344M Serial Digital Interfaces**
- **Serial Digital Data Equalization and Reception**
- **Data Recovery Equalization**

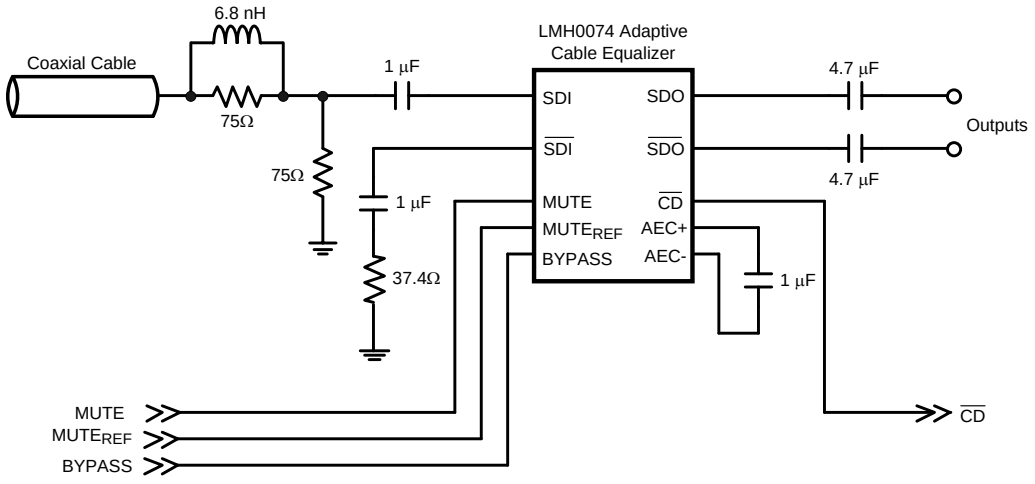
DESCRIPTION

The LMH0074 SMPTE 259M / 344M Adaptive Cable Equalizer is designed to equalize data transmitted over cable (or any media with similar dispersive loss characteristics). The equalizer operates over a wide range of data rates from 125 Mbps to 540 Mbps and supports SMPTE 259M and SMPTE 344M.

The LMH0074 implements DC restoration to correctly handle pathological data conditions. The equalizer may be driven in either a single ended or differential configuration.

Additional features include separate carrier detect and output mute pins which may be tied together to mute the output when no signal is present. A programmable mute reference is provided to mute the output at a selectable level of signal degradation.

Typical Application



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	−0.5V to 3.6V
Input Voltage (all inputs)	−0.3V to V_{CC}+0.3V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (Soldering 4 Sec)	+260°C
Package Thermal Resistance θ_{JA} 16-pin WQFN θ_{JC} 16-pin WQFN	 +43°C/W +9°C/W
ESD Rating (HBM)	8kV
ESD Rating (MM)	250V

(1) "Absolute Maximum Ratings" are those parameter values beyond which the life and operation of the device cannot be ensured. The stating herein of these maximums shall not be construed to imply that the device can or should be operated at or beyond these values. The table of "Electrical Characteristics" specifies acceptable device operating conditions.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage (V_{CC} – V_{EE})	3.3V ±5%
Input Coupling Capacitance	1.0 µF
AEC Capacitor (Connected between AEC+ and AEC-)	1.0 µF
Operating Free Air Temperature (T_A)	−40°C to +85°C

DC ELECTRICAL CHARACTERISTICS

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified(1)(2).

Parameter		Test Conditions	Reference	Min	Typ	Max	Units
V_{CMIN}	Input Common Mode Voltage		SDI, $\overline{SDI}$		1.9		V
V_{SDI}	Input Voltage Swing	At LMH0074 input(3)(4)		720	800	950	mV_{P-P}
V_{CMOUT}	Output Common Mode Voltage		SDO, $\overline{SDO}$		V_{CC} – V_{SDO}/2		V
V_{SDO}	Output Voltage Swing	50Ω load, differential			750		mV_{P-P}
	$MUTE_{REF}$ DC Voltage (floating)		$MUTE_{REF}$		1.3		V
	$MUTE_{REF}$ Range				0.7		V
	$\overline{CD}$ Output Voltage	Carrier not present	$\overline{CD}$	2.6			V
		Carrier present				0.4	V
	MUTE Input Voltage	Min to mute outputs	MUTE	3.0			V
		Max to force outputs active				0.8	V
I_{CC}	Supply Current	See(5)			63	77	mA

(1) Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to V_{EE} = 0 Volts.
(2) Typical values are stated for V_{CC} = +3.3V and T_A = +25°C.
(3) Specification is ensured by characterization.
(4) The maximum input voltage swing assumes a nonstressing, DC-balance signal; specifically, the SMPTE-recommended color bar test signal. Pathological or other stressing signals may not be used. This specification is for 0m cable only.
(5) Supply current depends on the amount of cable being equalized. The current is highest for short cable and decreases as the cable length is increased. Refer to Figure 2.

AC ELECTRICAL CHARACTERISTICS

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified(1).

Parameter		Test Conditions	Reference	Min	Typ	Max	Units
BR_{MIN}	Minimum Input Data Rate		SDI, $\overline{SDI}$		125		Mbps
BR_{MAX}	Maximum Input Data Rate					540	Mbps
	Jitter for various Cable Lengths (with equalizer pathological)	270 Mbps, Belden 1694A, 400 meters(2)			0.2		UI
		270 Mbps, Belden 8281, 280 meters(2)			0.2		UI
t_r,t_f	Output Rise Time, Fall Time	20% – 80%(2)	SDO, $\overline{SDO}$		100	220	ps
	Mismatch in Rise/Fall Time	See(2)			2	15	ps
t_{OS}	Output Overshoot	See(2)			1	5	%
R_{OUT}	Output Resistance	Single-ended(3)			50		Ω
RL_{IN}	Input Return Loss	See(4)	SDI, $\overline{SDI}$	15	18-20		dB
R_{IN}	Input Resistance	Single-ended			1.3		kΩ
C_{IN}	Input Capacitance	Single-ended(3)			1		pF

(1) Typical values are stated for V_{CC} = +3.3V and T_A = +25°C.
(2) Specification is ensured by characterization.
(3) Specification is ensured by design.
(4) Input return loss is dependent on board design. The LMH0074 meets this specification on the SD074 evaluation board from 5MHz to 1.5GHz.

CONNECTION DIAGRAM

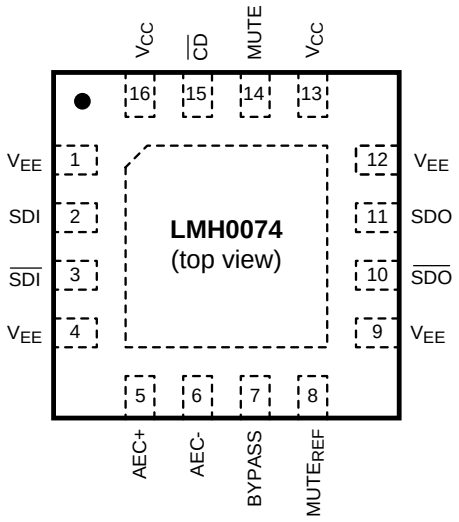
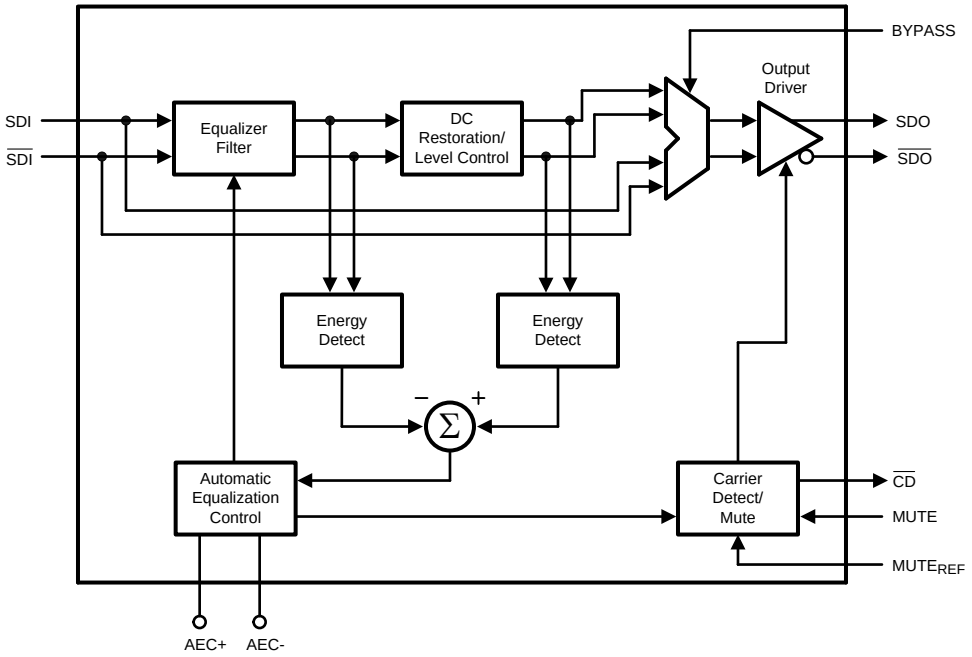


Figure 1. 16-Pin WQFN Package
See Package Number RUM0016A

Pin Descriptions

Pin	Name	Description
1	V_{EE}	Negative power supply (ground).
2	SDI	Serial data true input.
3	$\overline{SDI}$	Serial data complement input.
4	V_{EE}	Negative power supply (ground).
5	AEC+	AEC loop filter external capacitor (1µF) positive connection.
6	AEC-	AEC loop filter external capacitor (1µF) negative connection.
7	BYPASS	Bypasses equalization and DC restoration when high. No equalization occurs in this mode.
8	$MUTE_{REF}$	Mute reference. Sets the threshold for $\overline{CD}$ and (with $\overline{CD}$ tied to MUTE) determines the maximum cable to be equalized before muting. $MUTE_{REF}$ may be unconnected for maximum equalization.
9	V_{EE}	Negative power supply (ground).
10	$\overline{SDO}$	Serial data complement output.
11	SDO	Serial data true output.
12	V_{EE}	Negative power supply (ground).
13	V_{CC}	Positive power supply (+3.3V).
14	MUTE	Output mute. To disable the mute function and enable the output, MUTE must be tied to GND or a low level signal. To force the outputs to a muted state, tie to V_{CC}. $\overline{CD}$ may be tied to this pin to inhibit the output when no input signal is present. MUTE has no function in BYPASS mode.
15	$\overline{CD}$	Carrier detect. $\overline{CD}$ is high when no signal is present. $\overline{CD}$ has no function in BYPASS mode.
16	V_{CC}	Positive power supply (+3.3V).
DAP	V_{EE}	Connect exposed DAP to negative power supply.

Block Diagram



DEVICE OPERATION

BLOCK DESCRIPTION

The **Equalizer Filter** block is a multi-stage adaptive filter. If Bypass is high, the equalizer filter is disabled.

The **DC Restoration / Level Control** block receives the differential signals from the equalizer filter block. This block incorporates a self-biasing DC restoration circuit to fully DC restore the signals. If Bypass is high, this function is disabled.

The signals before and after the DC Restoration / Level Control block are used to generate the **Automatic Equalization Control (AEC)** signal. This control signal sets the gain and bandwidth of the equalizer filter. The loop response in the AEC block is controlled by an external 1µF capacitor placed across the AEC+ and AEC- pins.

The **Carrier Detect / Mute** block generates the carrier detect signal and controls the mute function of the output. This block utilizes the **$\overline{\text{CD}}$** and **MUTE** signals along with **Mute Reference (MUTE_{REF})**.

The **Output Driver** produces SDO and $\overline{\text{SDO}}$.

MUTE REFERENCE (MUTE_{REF})

The mute reference sets the threshold for $\overline{\text{CD}}$ and (with $\overline{\text{CD}}$ tied to MUTE) determines the amount of cable to equalize before automatically muting the outputs. This is set by applying a voltage inversely proportional to the length of cable to equalize. As the applied MUTE_{REF} voltage is increased, the amount of cable that can be equalized before carrier detect is de-asserted and the outputs are muted is decreased. MUTE_{REF} may be left unconnected for maximum equalization before muting.

CARRIER DETECT ($\overline{\text{CD}}$) AND MUTE

Carrier detect $\overline{\text{CD}}$ indicates if a valid signal is present at the LMH0074 input. If MUTE_{REF} is used, the carrier detect threshold will be altered accordingly. $\overline{\text{CD}}$ provides a high voltage when no signal is present at the LMH0074 input. $\overline{\text{CD}}$ is low when a valid input signal is detected.

MUTE can be used to manually mute or enable SDO and $\overline{\text{SDO}}$. Applying a high input to MUTE will mute the LMH0074 outputs. Applying a low input will force the outputs to be active.

$\overline{CD}$ and MUTE may be tied together to automatically mute the output when no input signal is present.

INPUT INTERFACING

The LMH0074 accepts either differential or single-ended input. The input must be AC coupled. Transformer coupling is not supported.

The LMH0074 correctly handles equalizer pathological signals for standard definition serial digital video, as described in SMPTE RP 178.

OUTPUT INTERFACING

The SDO and $\overline{SDO}$ outputs are internally loaded with 50Ω. They produce a 750 mV_{P-P} differential output, or a 375 mV_{P-P} single-ended output.

APPLICATION INFORMATION

PCB LAYOUT RECOMMENDATIONS

Refer to the following Application Note on TI's website: AN-1372, "LMH0034 PCB Layout Techniques." The PCB layout techniques in the application note apply to the LMH0074 as well.

SUPPLY CURRENT VS. CABLE LENGTH

The supply current (I_{CC}) depends on the amount of cable being equalized. The current is highest for short cable and decreases as the cable length is increased. Figure 2 shows supply current vs. Belden 1694A cable length for 270 Mbps data.

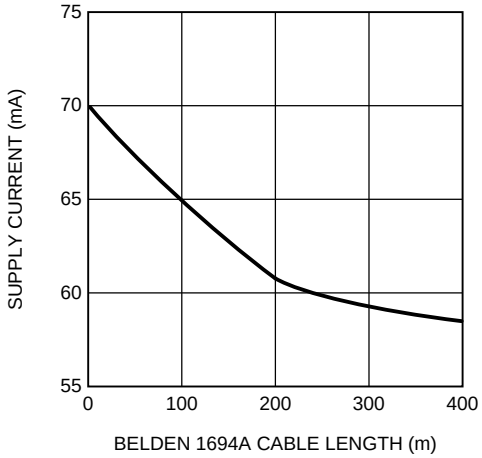


Figure 2. Supply Current vs. Belden 1694A Cable Length, 270 Mbps

REVISION HISTORY

Changes from Revision C (April 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH0074SQ/NOPB	ACTIVE	WQFN	RUM	16	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	L074	Samples
LMH0074SQE/NOPB	ACTIVE	WQFN	RUM	16	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	L074	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

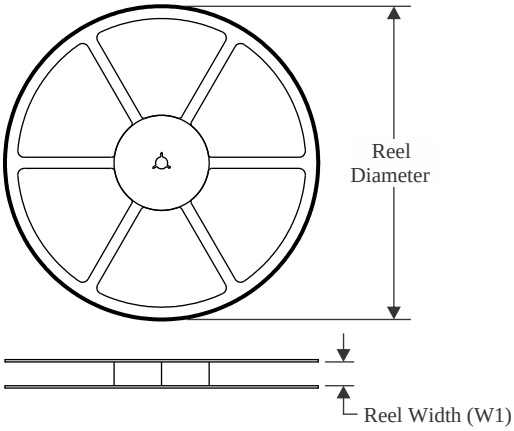
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

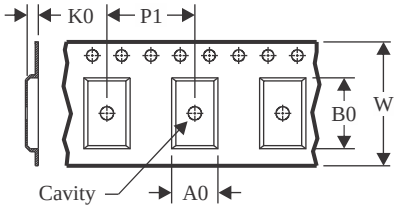
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

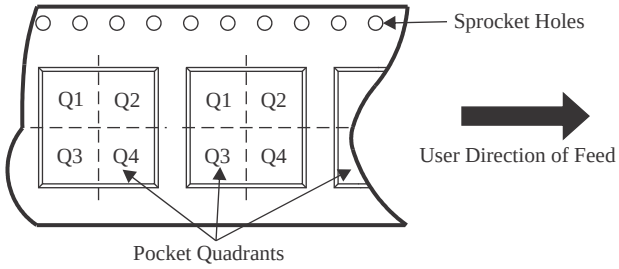


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

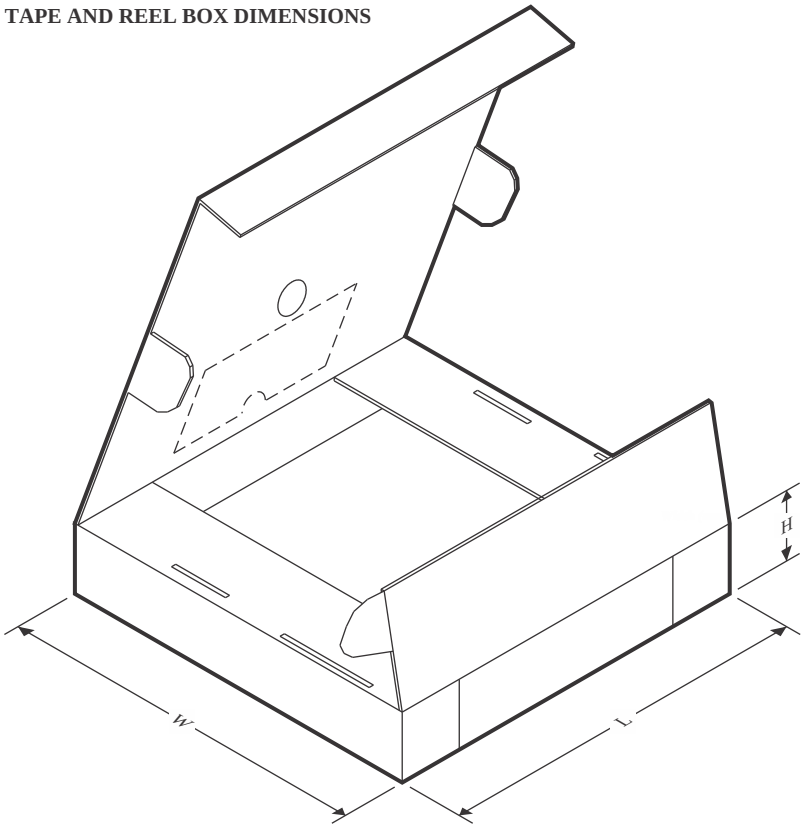
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH0074SQE/NOPB	WQFN	RUM	16	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

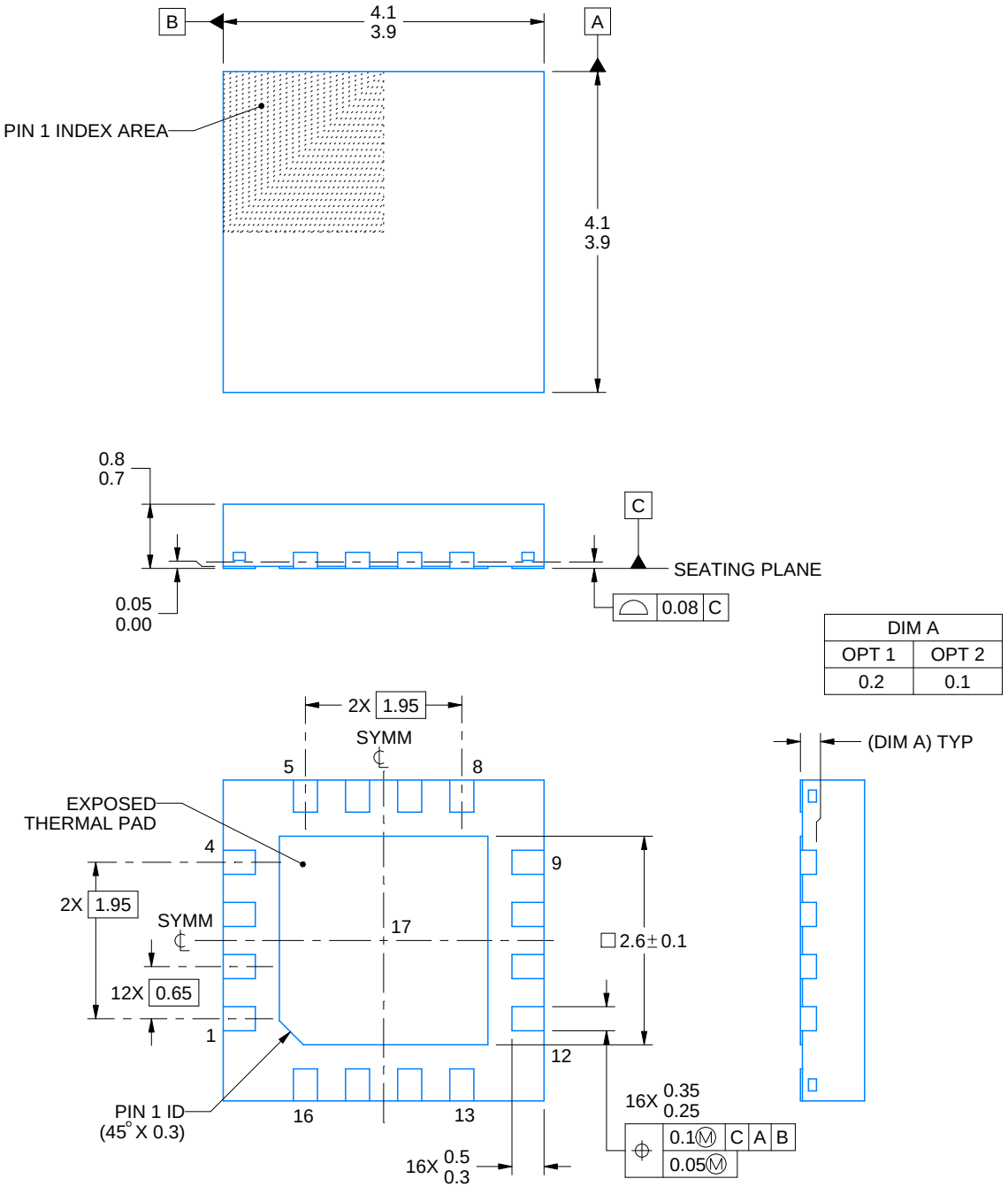
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH0074SQE/NOPB	WQFN	RUM	16	250	208.0	191.0	35.0

RUM0016A

PACKAGE OUTLINE

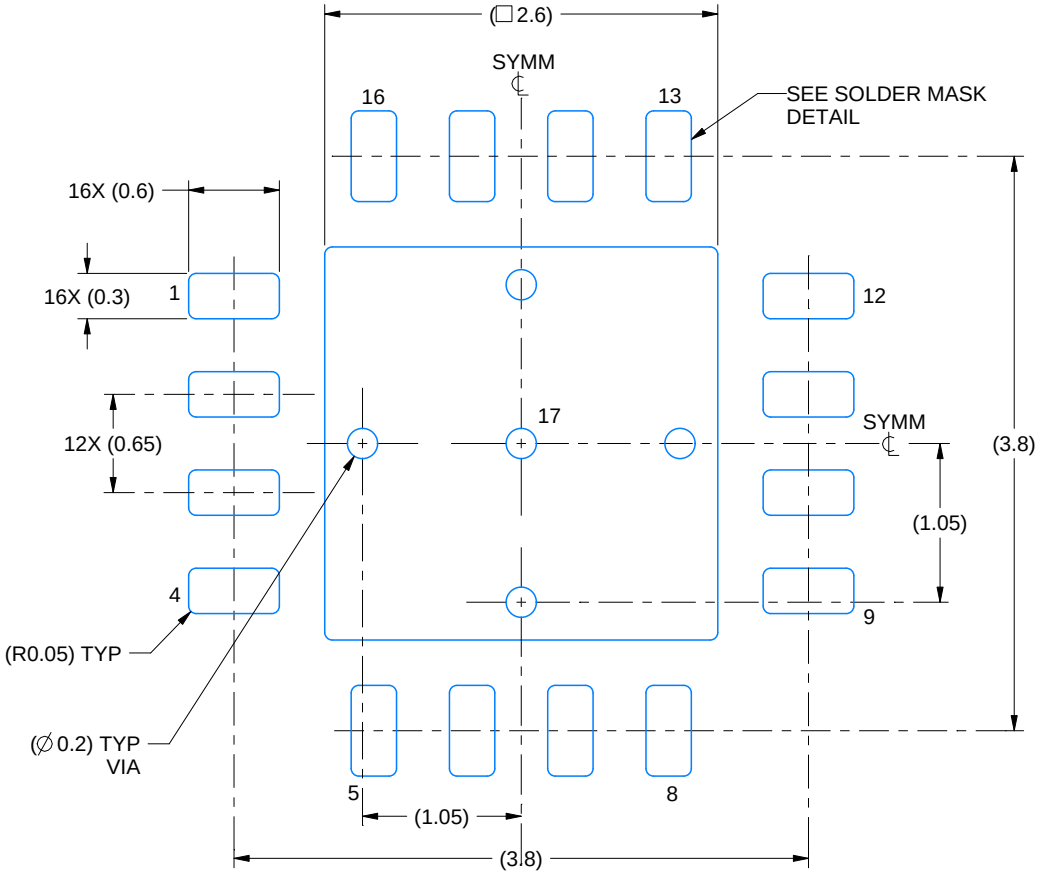
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

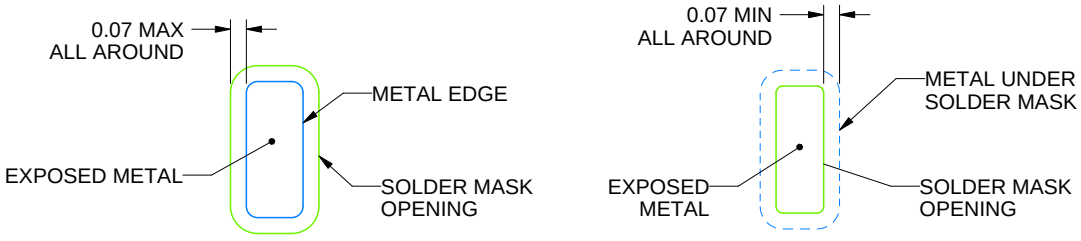


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

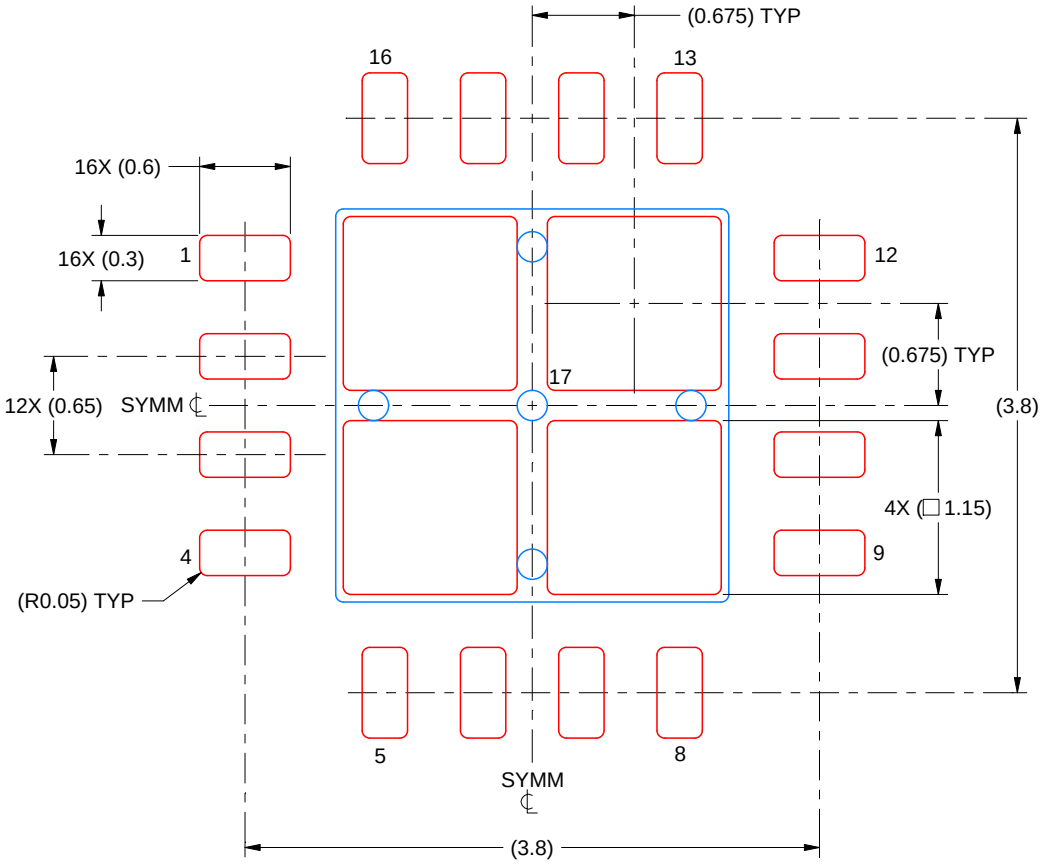
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RUM0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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