Application Report
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# 12G-SDI Printed Circuit Board (PCB) Layout Guidelines

*Nasser Mohammadi*

**ABSTRACT**

This application note enables system designers to implement best practices for PCB layouts in SDI or other high-speed applications.

**Contents**



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## 1 Background

Designers today are faced with major challenges when upgrading from 3G to next-generation 12G-SDI video capture and playback cards. Challenges include achieving maximum cable reach, ensuring SMPTE standards compatibility, and meeting system or regulatory requirements such as power consumption and electromagnetic radiation. To ensure a long product life cycle, it is important not only to meet SMPTE requirements but also to provide performance margin in addition to these requirements.

At 12G-SDI, various phenomena on the PCB layout can jeopardize signal integrity margin. At these speeds, components pads and anti-pads are active elements and contribute to impedance discontinuity. Trace or BNC signal pin stubs can lead to detrimental reflections in the signal path. Moreover, cross-talk effects in applications such as distribution amplifiers (DAs) and video converters, where multiple 12G-SDI drivers and equalizers reside on the same board, may significantly reduce overall cable reach without proper signal isolation. In short, a poorly designed PCB undermines a product's potential for SMPTE compatibility while also needlessly sacrificing performance.

This application note highlights key PCB layout guidelines in conjunction with TI's SDI portfolio that ensures a robust and high-performance signal integrity design.

## 2 PCB Material

If possible, use a very low loss PCB board material. This reduces insertion loss and parasitics, thus optimizing slew rate, cable reach, and return loss.

## 3 Controlled Impedance Signals

The following guidelines should be followed for proper characteristic impedance control and continuity for the high-speed signals.

- Choose a suitable board stack-up that supports 75 Ω single-ended trace and 100 Ω coupled differential characteristic impedance trace routing.
- Ground planes must not be broken in the GND reference layer immediately beneath he transmission line.
- When using an impedance calculator, the outer layers of the PCB contain less glass than the inner layers. This introduces a lower dielectric constant. Therefore, it is recommended to contact the PCB vendor to obtain dielectric constants for outer and inner layers.
- If a transmission line must transition to a different board layer with a signal via, TI recommends using the largest diameter via compatible with the transmission line trace width. This is done to minimize trace width mismatch. If this is not possible, at least two vias must be used to minimize via inductance.
- The current return path should be considered when assigning signal ground and supply layers. The high-speed signal layers must not be between the supply plane and the ground layer. Supply plane and ground plane must be next to one another. Otherwise, the current return path may create noise on the signal layer if it is sandwiched in between.
- Bending transmission lines during routing must be done gradually. The bend radius must be at least 5 to 6 times the trace width. A 90-degrees or lower bend angle may cause trace width mismatches, ultimately leading to unwanted changes in trace impedance characteristics.

## 4 Passive Component Anti-Pad

Place the anti-pad (ground relief) on all PCB layers directly under passive components and IC landing pads to minimize parasitic capacitance effects. The size of the anti-pad depends on the board stack-up and can be optimized by a 3D electromagnetic (EM) simulation tool.

## 5 BNC Anti-Pad

Consult the BNC vendor to provide the recommended BNC footprint and anti-pad based on the board stackup used for your design.



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## 6 Trace Length From BNC Connector to Device

The trace between the device SDI interface and the BNC connector pin should be as short as possible. A short trace and low insertion loss PCB material enhances rise/fall times, reduces parasitics, improves return loss, and minimizes insertion loss on the PCB, thereby improving overall cable reach. Figure 1 shows how minimizing the FR4 trace length between SDI interface and BNC connector pins reduces insertion loss across frequency on the PCB.

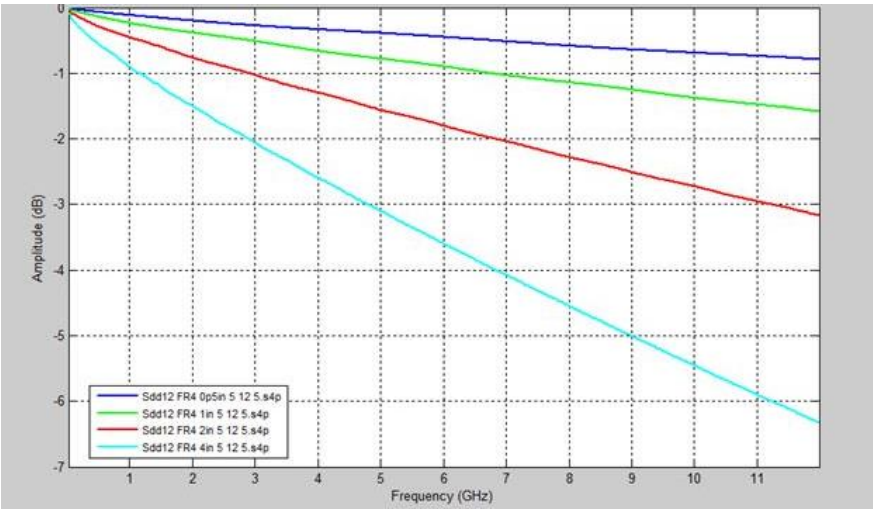


**Figure 1. FR4 SDD21 Insertion Loss vs Frequency for Various Trace Lengths**

Using the same PCB board stackup, simulations also show a correlation between trace length and slew rate. In the analysis shown in Figure 2, every 1000 mils (1 in.) of FR4 PCB trace (dielectric constant Er = 4.3) slows down the slew rate by about 2 ps. For 12G-SDI cable driver applications where the output rise/fall times must be less than 45 ps, this means that each inch of FR4 trace can decrease margin from the limit by about 5%! Additionally, a longer trace length on a 12G-SDI cable EQ input causes additional insertion loss in the system and reduces high frequency signal content, ultimately resulting in lower cable reach.

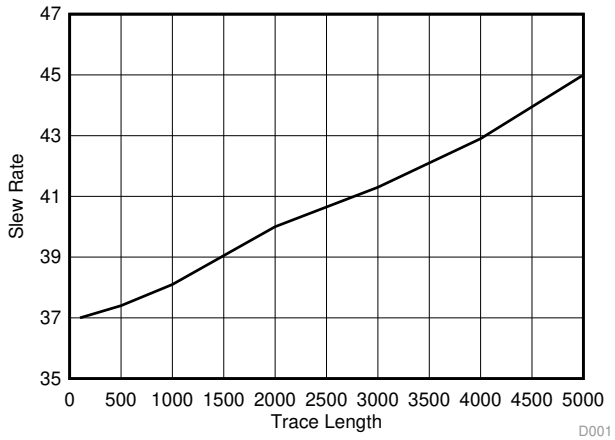


**Figure 2. FR4 Slew Rate (ps) vs Trace Lengths (mils)**


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## 7 Return Loss Optimization

A critical SDI performance parameter is return loss. At 12G-SDI, passive component pads, trace length, board material, and BNC selection and layout all play a major role in signal performance. Both time domain and frequency domain analyses must be used to optimize the impedance to achieve the required return loss with additional margin. A short trace from device pin to the BNC signal pin optimizes both the rise/fall time and return loss while minimizing insertion loss.

In previous generation 3G-SDI cable drivers and EQs, a carefully chosen external resistor and inductor network was required to meet the stringent return loss requirements. Starting with the 12G-SDI products, Texas Instruments has integrated these passive components into the IC, thereby simplifying this iterative design process. Figure 3 shows the return loss performance of the LMH1297 12G-SDI bidirectional I/O taken on an LMH1297EVM, where return loss requirements are easily met without the need for external resistor or inductor.

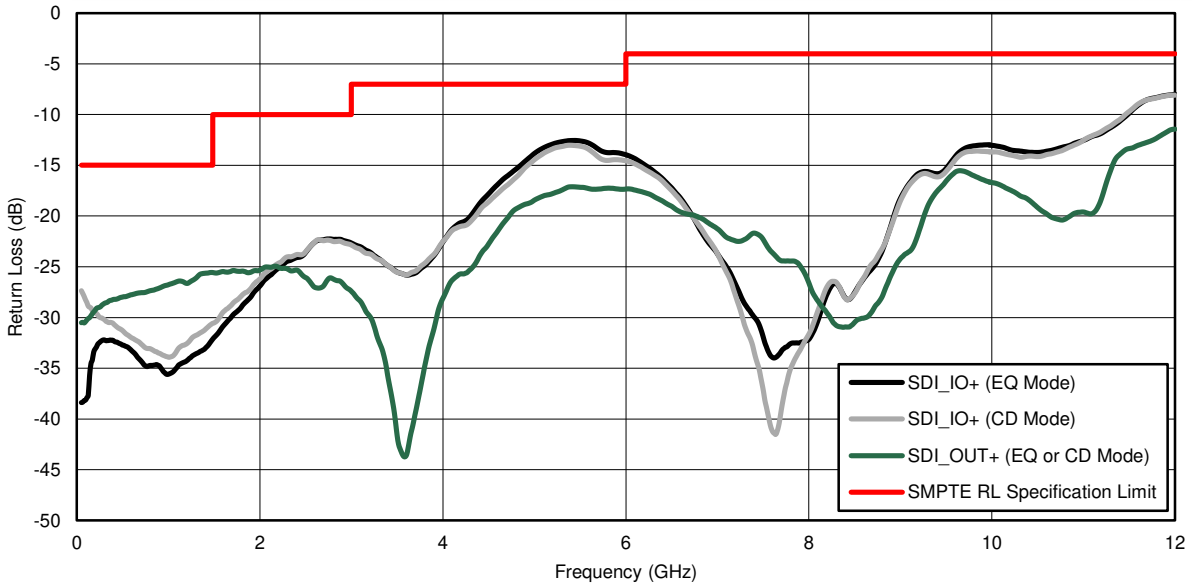


**Figure 3. LMH1297 Return Loss without External Components**

## 8 High Frequency Signal Isolation

In certain applications where cable driver and or equalizers reside on the same board, it is important to provide as much isolation as possible to minimize crosstalk. There are several recommended options to implement this isolation:

1. Use a stripline trace to bury, or sandwich, the signal between two ground planes.
2. Use a grounded coplanar waveguide to provide better isolation. In a coplanar waveguide, a center conductor with ground stitches on both sides of the signal is used. Using coplanar trace, the return current generated by the high frequency signal is shorted to the ground plane. Figure 4 shows an example coplanar PCB layout using the LMH1297 bidirectional I/O. To isolate or reduce cross talk, this coplanar PCB layout isolates SDI input pins number 1 and 2 from SDI output pins 7 and 8. Note that the 50-mil spacing between the ground stitched vias provide a ground return path for up to the 3rd harmonics of cable driver slew rate.



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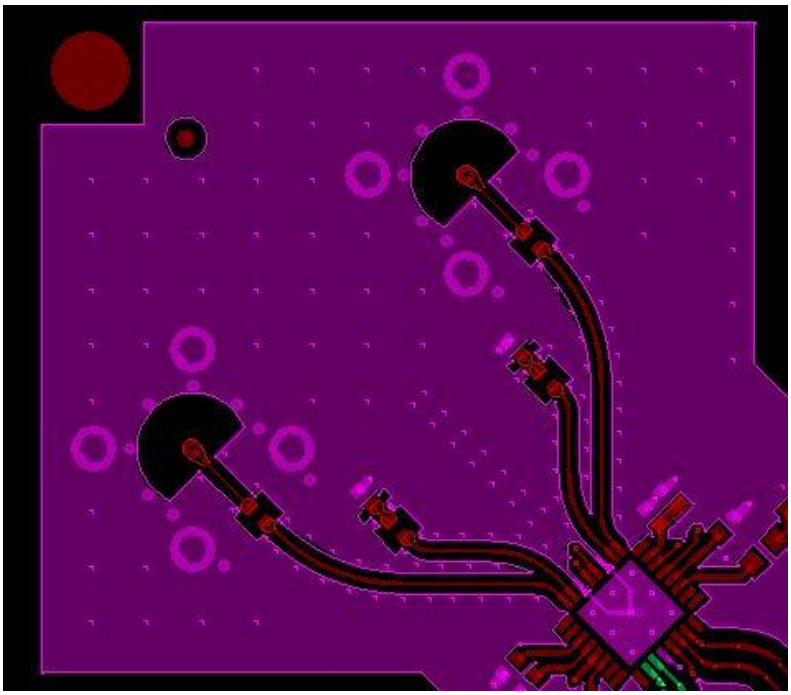

**Figure 4. LMH1297 Through-Hole Coplanar Example**

3. Use a micro-strip PCB layout with ground stitching and ground flooding to isolate the driver and equalizer from one another. Figure 5 shows an example of a micro-strip PCB layout with ground stitching and GND flooding to isolate LMH1297 input pins 1 and 2 from output pins 7-8.

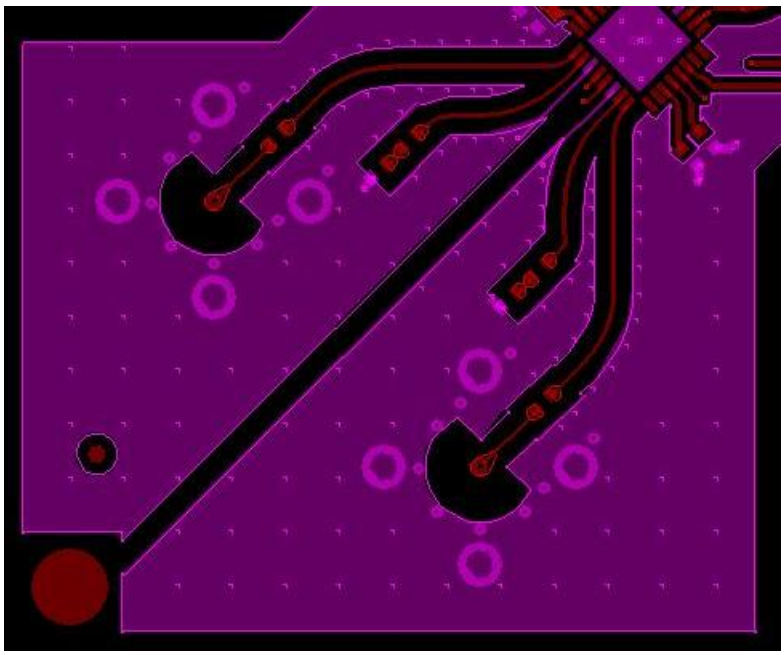

**Figure 5. LMH1297 Through-Hole Microstrip Example**


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The following signal isolation guidelines should be followed, regardless of the isolation technique implemented from the previously mentioned options:

- Digital signal lines must be routed on a separate plane from the RF signals and must be separated by ground planes in between. Although digital signals may operate at low clock rates, the resulting rise/fall times and harmonics may interfere with RF signals.
- High-speed signals that overlap one another on the PCB must have a ground plane in between.
- Cable driver output signals must be kept as far from equalizer input signals as possible.
- Different power supply rails must be routed on dedicated PCB planes. Also, cable driver signals must be isolated from power planes.

## 9 Ground Plane Reference

The following guidelines should be followed for implementing a proper ground plane reference.

- A common practice is to use a solid ground plane on Layer 2 and Layer 3, assuming Layer 1 is used for routing coupled differential 100-Ω and single-ended 75-Ω traces. In this case, the PCB stackup should be designed such that Layer 1 high-speed signals references Layer 2 for differential 100-Ω and Layer 3 for single-ended 75-Ω traces.
- The ground plane reference must not be used to route traces.
- Solid ground plane must exist below the RF signals and must not be broken or split beneath the high-speed trace.
- Ground stitching is highly recommended for the RF portion of the PCB. This helps to reduce ground inductance due to the ground-current return path.
  - One approach is rule of thumb. To determine the spacing between ground stitched vias, the following rough estimate can be used:
    1. Determine the slew rate bandwidth. As a rule of thumb, the minimum bandwidth (in GHz) can be determined by the following equation:

       Min. BW = 0.35 ÷ [slew_rate (in ns)]

    2. Based on the resulting bandwidth, calculate the quarter wavelength to determine the maximum ground stitching via spacing.

    For example, a 30 ps rise/fall time results in 0.35 ÷ 0.03 = 11.6 GHz bandwidth. Rounding up to 12 GHz bandwidth, assume 3e11mm/sec speed of light through vacuum and a 4.3 FR4 dielectric constant.

    Quarter wavelength = [1/4 X (3e11/SQRT(4.3)] / (12e9) = 3 mm or 118 mils
  - Another approach is to use spectrum analyzer to determine the signal bandwidth. For example, Figure 6 and Figure 7 show color bar spectrum content for 3G and 12G-SDI data rates, respectively. FOr 3G, at every 2.97 GHz, there is a pole where maximum energy is transferred.



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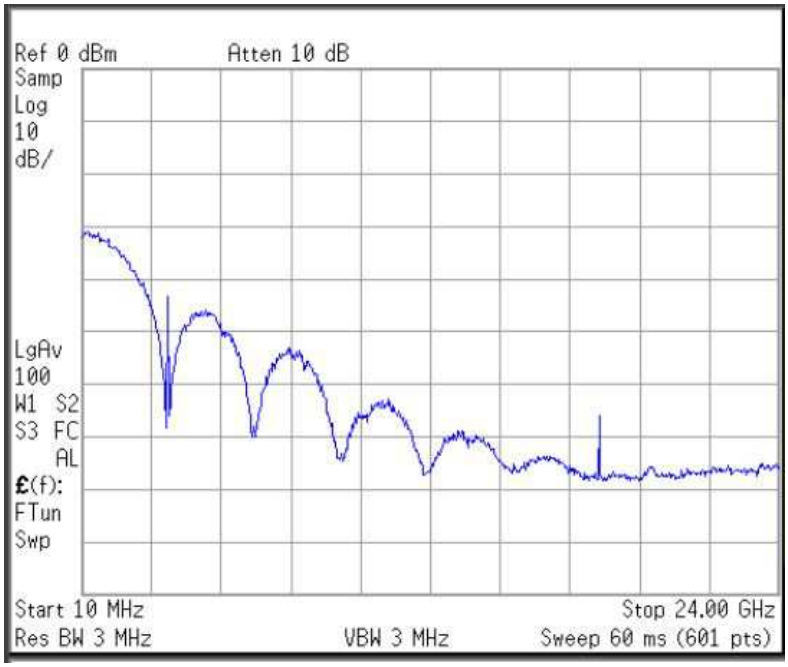


**Figure 6. 3G Video Pattern Spectrum (2.4 GHz/div.)**

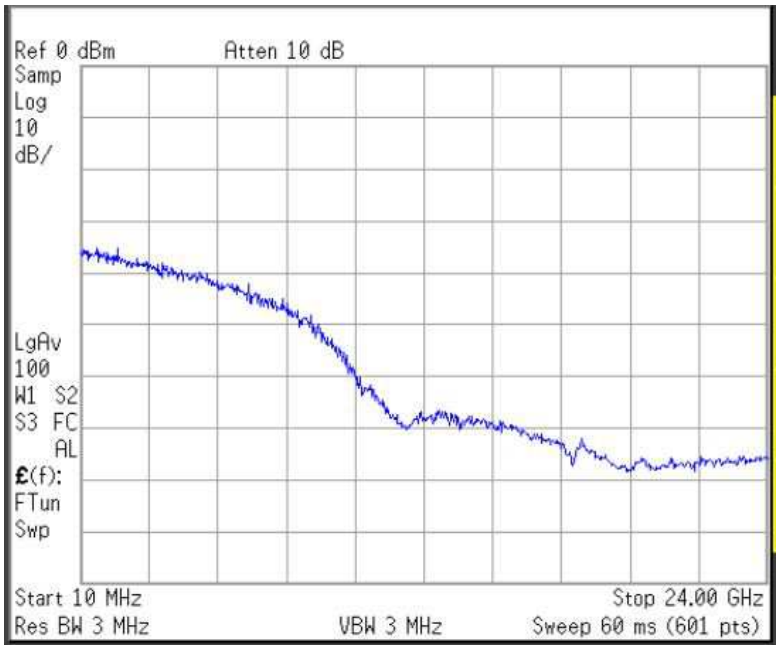


**Figure 7. 12G Video Pattern Spectrum (2.4 GHz/div.)**

Given the harmonics of the data patterns, it important to ensure that at least the 2nd or 3rd harmonics for the video pattern are transferred. For example, at 3G-SDI, we must allow at least a 9 GHz signal bandwidth. For 9 GHz, the quarter wavelength is about [0.25 × (3 × 10e11)] ÷ SQRT(4.3) ÷ 9e9 = 4 mm or about 158 mils. By the same token, for 12G-SDI, we must allow up to at least 24 or 36 GHz bandwidth, resulting in 1.5 mm (60 mils) or 1 mm (40 mils) spacing for ground stitched vias.


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## 10 Decoupling or Bypass Capacitors

Decoupling, or bypass, capacitors eliminate power supply noise and thus improve the overall signal-to-noise (SNR) ratio. The following guidelines should be followed for optimizing power supply deoupling capacitors.

- When selecting capacitors for supply decoupling, verify that the targeted noise frequency is well below the Self-Resonance Frequency (SRF) of the chosen capacitor. When operating beyond the SRF range, the capacitor no longer blocks the noise frequency and becomes inductive, thereby increasing transmission impedance and thus defeating its intended purpose.
- For power supply filtering, it is recommended to use several capacitors with different values to attenuate noise across different frequency bands.
- To minimize via inductance for connecting IC pins to supply or ground planes, it is recommended to use at least two vias connecting VCC pad to decoupling capacitors and ground. Coupling capacitors must be placed as close and adjacent to the device as possible. Vias are usually placed tangent to the supply pins' landing pads with the shortest trace possible.

## 11 Exposed Pad (EP) or Direct-Attach Pad (DAP)

Underneath the IC, there is normally an exposed, or direct-attach, pad (DAP) that must be grounded.

The purpose of this exposed pad is two-fold:

1. Provide thermal relief.
2. Provide a return current or ground signal path. The DAP provides a DC current return path for high speed signals to the ground plane. To minimize return current inductance, refer to the device landing pad drawings in the datasheet for recommendations regarding the minimum number of vias.

## 12 Summary

A well-designed high-speed PCB layout is not only essential, but also critically important in creating systems that meet SMPTE requirements at 12G-SDI. Passive components pads, BNC landing pads, PCB board material, IC anti-pads, and high-speed routing techniques all have a direct impact on surpassing SMPTE limit requirements. By following the PCB design layout recommendations described in this application note and designing with products from TI's SDI portfolio, designers are enabled to develop robust, high-performance systems with confidence.



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