Application Report
SNLA110A–October 2008–Revised April 2013

AN-1893 Demonstrating SMPTE-Compliant SDI Output Jitter Using the LMH1982 and Virtex-5 GTP Transmitter

ABSTRACT

As 3-Gbps serial digital interface (SDI) gains adoption in professional and broadcast video equipment to enable fast-frame 1080p HD video over a single link, the need for flexible and high-performance video clock generation becomes critical to reliably transmit and receive triple-rate (3G/HD/SD) SDI video. This is especially true for multi-channel video equipment using SDI serializers and deserializers based on the serial transceivers in high-end FPGAs, such as Xilinx's Virtex-5 LXT. Because FPGA-based serializers virtually transfer any jitter on its reference clock input to its serial data output, they require very low-jitter reference clocks to meet the SMPTE-specified SDI output jitter requirements.

Contents

List of Figures

List of Tables

1 Introduction

This application report demonstrates SMPTE-compliant SDI output jitter with a Virtex-5 reference design using low-jitter reference clocks from Texas Intruments LMH1982 video clock generator. The reference design included a SD/HD video pattern generator and a multi-rate SDI serializer using the Virtex-5 RocketIO GTP transceiver. The demo was implemented on Xilinx's ML571 Virtex-5 serial digital video (SDV) demo board. TI's LMH1982SQEEVAL evaluation board, which includes the LMH1981 sync separator and LMH1982, was used to generate an external genlock clock for the demo. To interface this external clock to the ML571 board, a CTCMSMA plug-in clock module with SMA connectors (from Cook Technologies) was also required.

2 Demo Overview

Figure 1 shows a block diagram of the entire demo setup with the test and measurement equipment. A Tektronix TG700 test signal generator was used to generate an analog reference input signal, such as SD composite black-burst or HD tri-level sync. This was fed to the LMH1981, which extracted the sync signals required by the LMH1982. A host PC with the LMH1982 evaluation software graphical user interface (GUI) was used to program the genlock configuration and reference clock rate according to the selected reference input and SDI output format. After the SDI output was frequency-locked to the reference input, the SDI output jitter was measured on a Tektronix WFM7100 set for both "Timing Jitter" and "Alignment Jitter" high pass filters (HPF).

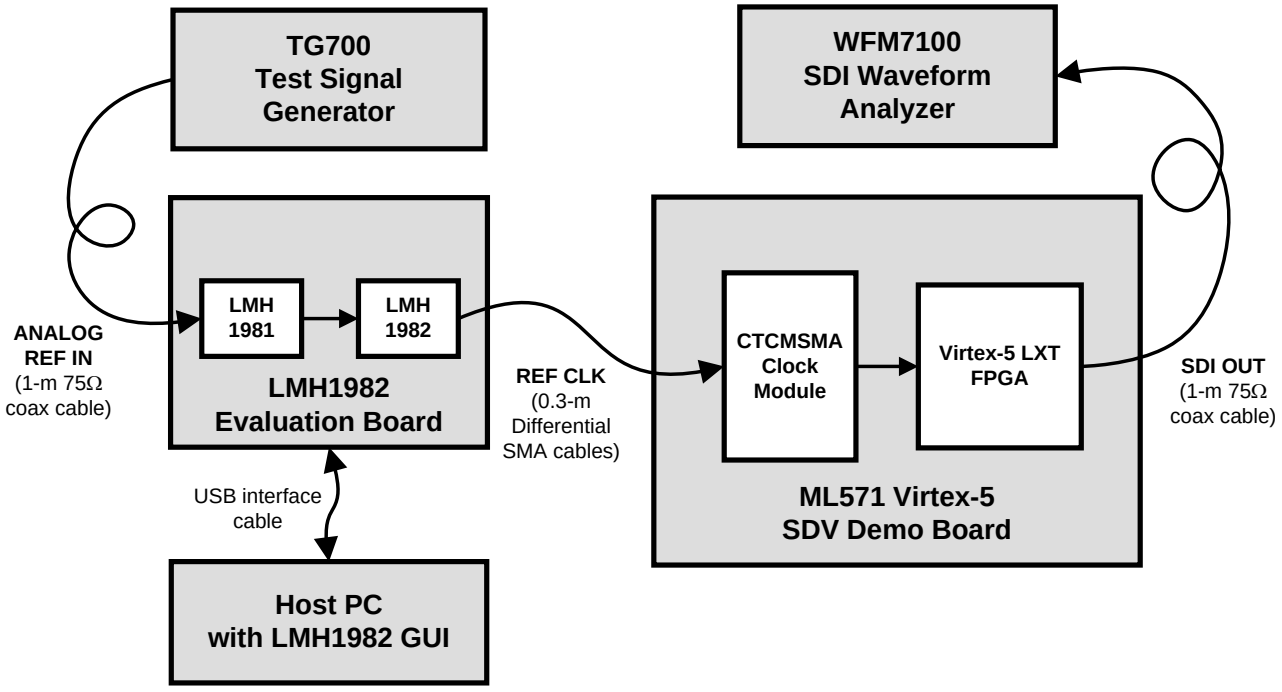

Figure 1. Overview of Demo Setup

3 FPGA Reference Design

In the multi-rate SDI transmitter reference design, a reference clock is required for clocking the GTP transmitter (Tx) to generate and transmit a color bars or SDI checkfield test pattern signal. Two different clock rates, 148.5 MHz and 148.5/1.001 MHz, are used to support the various SDI output formats supported by this demo. The 148.5 MHz clock rate is needed to transmit HD-SDI at 1.485 Gbps and also SD-SDI. The SD-SDI transmitter uses 11x over-sampling (11 x 270 Mbps) to realize an effective bit rate of 2.97 Gbps, which also corresponds to the clock rate x 20. The 148.5/1.001 MHz clock rate is needed to transmit HD-SDI at 1.485/1.001 Gbps, where the 1.001 factor denotes rate compatibility with the NTSC system.

The LMH1982 provided the external reference clock to the GTP transmitter via the SMA clock module, which plugged into the ML571 board. Figure 2 shows a simplified block diagram of the reference design and reference clock routing implemented on the ML571.

The reference design was loaded to the FPGA via the SystemACE controller included on the ML571. Once loaded, the FPGA demo was controlled using on-board switches to select the output SDI standard, bit rate, video format, and video pattern. The reference input format and clock rate were selected and programmed to the LMH1982 according to the SDI output format evaluated.

For more complete descriptions of the multi-rate SDI transmitter reference design example used in this demo, see the *Xilinx's XAPP514 SDI Reference Design Manual* or contact their application support.

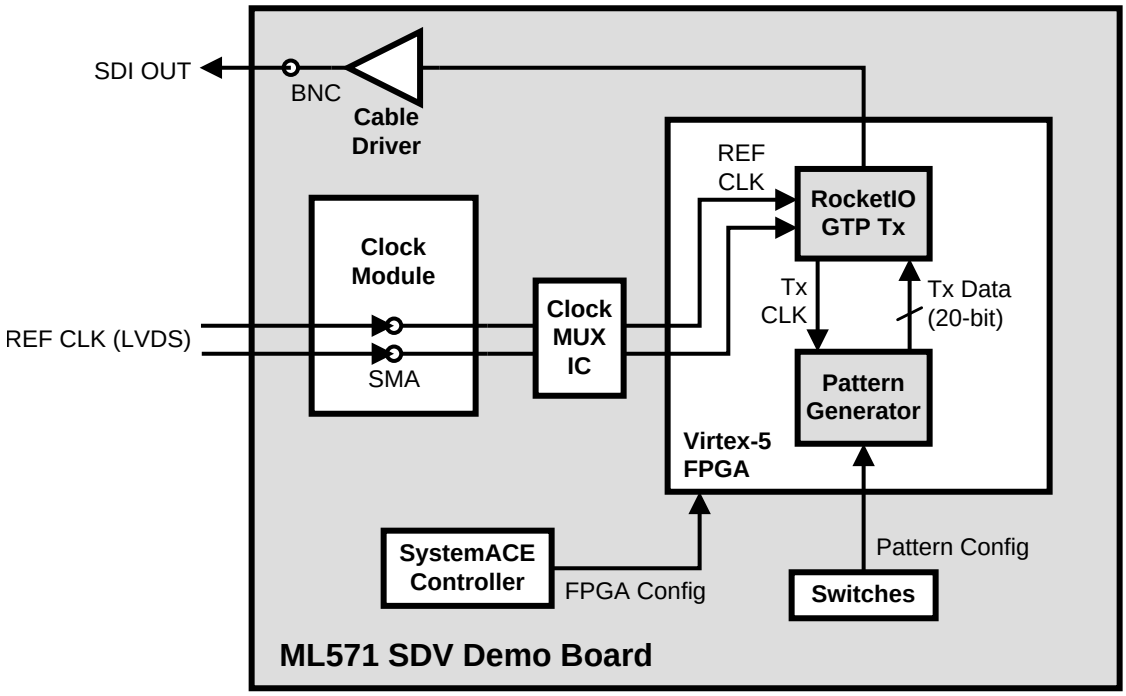

Figure 2. ML571 Board with Reference Design and Clock Routing

4 HD-SDI Output Jitter Hypothesis

Based on the inference of reference clock jitter on the transmitter's output performance, it is possible estimate the HD-SDI output alignment jitter from the typical clock jitter specs of the LMH1982. The "Alignment Jitter" spec defined by SMPTE standards for HD-SDI output signals specifies high-frequency spectral components above 100 kHz. The LMH1982 datasheet specifies clock jitter components above 10 kHz using the time interval error (TIE) method. The LMH1982's typical clock output jitter is 45 ps p-p for the 148.5 MHz clock and 60 ps p-p for the 148.5/1.001 MHz clock.

Therefore, it would be a reasonable hypothesis to expect HD-SDI output alignment jitter as low as 0.07 UI, or 45 ps p-p, for formats based on the 148.5 MHz clock and as low as 0.09 UI, or 60 ps p-p, for formats based on the 148.5/1.001 MHz clock.

4.1 Notes on Clock Jitter

- The LMH1982 jitter specs quoted earlier assume that the external 27 MHz VCXO clock jitter is ≤20 ps p-p and the SD clock output is disabled.
- Refer to Appendix A for information regarding loop response design requirements to meet the SDI output "Timing Jitter" spec, which defines low-frequency spectral components above 10 Hz.

5 SDI Jitter Measurement Results

Using ordinary ML571 and LMH1982 boards, the output jitter was measured for the two major SD-SDI formats and two popular 1080i HD-SDI formats. 3G-SDI was not evaluated in this demonstration because the SDI reference design and the WFM7100 did not support 3G formats. For screen captures of the SDI output eye and jitter plots from the WFM7100, see Appendix B.

Table 1 shows a summary of the measured SDI output jitter as well as the SMPTE jitter specs, and the corresponding reference clock and reference input conditions. In every case, the measured jitter was less than half of the spec limit for both standards. HD-SDI jitter performance was evaluated using both SD and HD reference inputs; however, the eye/jitter plots were only captured for the HD reference inputs.

Table 1. Summary of SDI Jitter Measurements

SDI Output	SD-SDI 270 Mbps		HD-SDI 1.485/1.001 Gbps		HD-SDI 1.485 Gbps	
Output Format / Pattern	525i 59.94 RP 178[1]	625i 50 RP 178[1]	1080i 59.94 75% Color Bars		1080i 50 75% Color Bars	
SDI Eye and Jitter Plot	Figure 4	Figure 5	n/a[2]	Figure 6	n/a[2]	Figure 7
Timing Jitter Data (p-p)	0.06 UI	0.07 UI	0.13 UI	0.13 UI	0.12 UI	0.13 UI
Alignment Jitter Data (p-p)	0.06 UI	0.06 UI	0.09 UI (61 ps)	0.09 UI (61 ps)	0.07 UI (47 ps)	0.07 UI (47 ps)
SDI Standard	SMPTE 259M-2006		SMPTE 292M-1998			
Timing Jitter Spec (p-p)	< 0.2 UI		< 1.0 UI			
Alignment Jitter Spec (p-p)	< 0.2 UI		< 0.2 UI			
Reference Clock	148.5 MHz		148.5/1.001 MHz		148.5 MHz	
Datasheet Typ. Clock Jitter (p-p)	45 ps[3]		60 ps[3]		45 ps[3]	
Reference Input Format	NTSC	PAL	NTSC	1080i 59.94	PAL	1080i 50

(1) Refers to the “SDI Checkfield” test pattern specified in SMPTE RP 178-1996. 75% Color Bars was not a selectable SD test pattern option.

(2) HD-SDI eye/jitter plots were not captured for the SD reference input conditions.

(3) ICP2 and ICP3 register settings (register 14h) were both programmed to a value of 2 to reduce the charge pump current of PLL 2 and PLL 3, respectively, and thus lower their respective loop bandwidths. This effectively reduced the high-frequency jitter on the 148.5 MHz and 148.5/1.001 MHz clocks to improve HD-SDI output jitter in the alignment jitter frequency band.

6 Conclusions

These results demonstrate SMPTE-compliant jitter performance for SD-SDI and HD-SDI using the Virtex-5 RocketIO GTP transmitter with the LMH1981 and LMH1982 genlock clocking solution. There appears to be negligible jitter contribution from the GTP transmitter since there is only small difference between HD-SDI alignment jitter (converted to ps p-p) and the typical reference clock jitter spec. For example, the HD-SDI alignment jitter for 1080i 50 is 0.07 UI p-p, or 47 ps, and the typical LMH1982 clock jitter for 148.5 MHz is 45 ps, which gives an estimated jitter contribution of +2 ps from the GTP transmitter. Therefore, the HD-SDI output alignment jitter data corroborates the earlier stated hypothesis.

Moreover, a reasonable approximation can now be made for 3G-SDI output jitter based on the measured HD-SDI jitter results. Two of the 3G-SDI formats, 1080p 59.94 and 1080p 50, operate at exactly twice the bit rate of the two HD-SDI formats measured. Using the same LMH1982 clocks and a similar GTP transmitter reference design with a 1080p pattern generator, the 3G-SDI output jitter could be extrapolated by doubling the measured HD-SDI jitter for both bit rates.

Table 2 shows the 3G-SDI jitter approximated from the HD-SDI jitter measurements. Additionally, the 3G-SDI output alignment jitter could have been estimated directly from the LMH1982's clock jitter specs, as previously shown in Section 4.

Table 2. 3G-SDI Jitter Estimates

SDI Output	HD-SDI 1.485/1.001 Gbps	HD-SDI 1.485 Gbps	3G-SDI 2.97/1.001 Gbps	3G-SDI 2.97 Gbps
Output Format	1080i 59.94	1080i 50	1080p 59.94	1080p 50
Timing Jitter (p-p)	0.13 UI (measured)	0.13 UI (measured)	0.26 UI (estimate)	0.26 UI (estimate)
Alignment Jitter (p-p)	0.09 UI (measured)	0.07 UI (measured)	0.18 UI (estimate)	0.14 UI (estimate)
SDI Standard	SMPTE 292M-1998		SMPTE 424M-2006	
Timing Jitter Spec (p-p)	< 1.0 UI		< 2.0 UI	
Alignment Jitter Spec (p-p)	< 0.2 UI		< 0.3 UI (< 0.2 UI recommended)	
Reference Clock	148.5/1.001 MHz	148.5 MHz	148.5/1.001 MHz	148.5 MHz
Reference Input Format	1080i 59.94	1080i 50	1080i 59.94	1080i 50

7 Summary

This application report demonstrated the capability of the LMH1981 and LMH1982 to implement low-jitter genlock reference clocks for the Virtex-5 GTP transmitter in a multi-rate video pattern generator demo on the ML571 platform. The HD-SDI output alignment jitter was estimated from the LMH1982's clock jitter specs and ultimately verified from the HD-SDI jitter measurement results. Lastly, the HD-SDI jitter measurements were used to approximate 3G-SDI output jitter performance.

8 Resources

- *AN-1841 LMH1982 Evaluation Board User's Guide* (SNOA527)
- LMH1982 Product Page: http://www.ti.com/product/LMH1982
- LMH1981 Product Page: http://www.ti.com/product/LMH1981
- ML571-1982CLK Video Clock Module Product Page: http://sva.ti.com/en/interface/sdi/timing.html
- Xilinx ML571 SDV Demo Board Page: http://www.cook-tech.com/ctxil406.html
- *Improving Video Clock Generation in Modern Broadcast Video Systems* (SNLA176)
- XAPP514 v4.0 Xilinx Virtex Audio/Video Connectivity Solutions Application Report: http://www.xilinx.com/support/documentation/application_notes/xapp514.pdf
- *LMH1982 Multi-Rate Video Clock Generator With Genlock Data Sheet* (SNLS289)
- SMPTE 259M-2006 SD-SDI Standard
- SMPTE 292M-1998 HD-SDI Standard
- SMPTE 424M-2006 3G-SDI Standard

Appendix A Loop Respnse Design

The LMH1982 relies on its VCXO PLL (PLL 1) to phase-lock the external 27 MHz VCXO clock to the analog reference input in genlock mode. The VCXO clock also provides a stable 27 MHz source for its internal VCO PLLs to generate the 148.5 and 148.5/M MHz output clock rates. Jitter on the VCXO clock could easily transfer to the output clock with little or no attenuation. Therefore, proper design of PLL 1's loop response is necessary to minimize VCXO clock and output clock jitter. The loop response, characterized by the nominal −3 dB loop bandwidth (BW) and damping factor (DF), was designed using the external loop filter and other PLL parameters programmed with the LMH1982 GUI.

Figure 3 shows a simplified block diagram of the LMH1982 board with the LMH1981, external VCXO, and loop filter. The loop filter component values were derived using the loop response analysis described below.

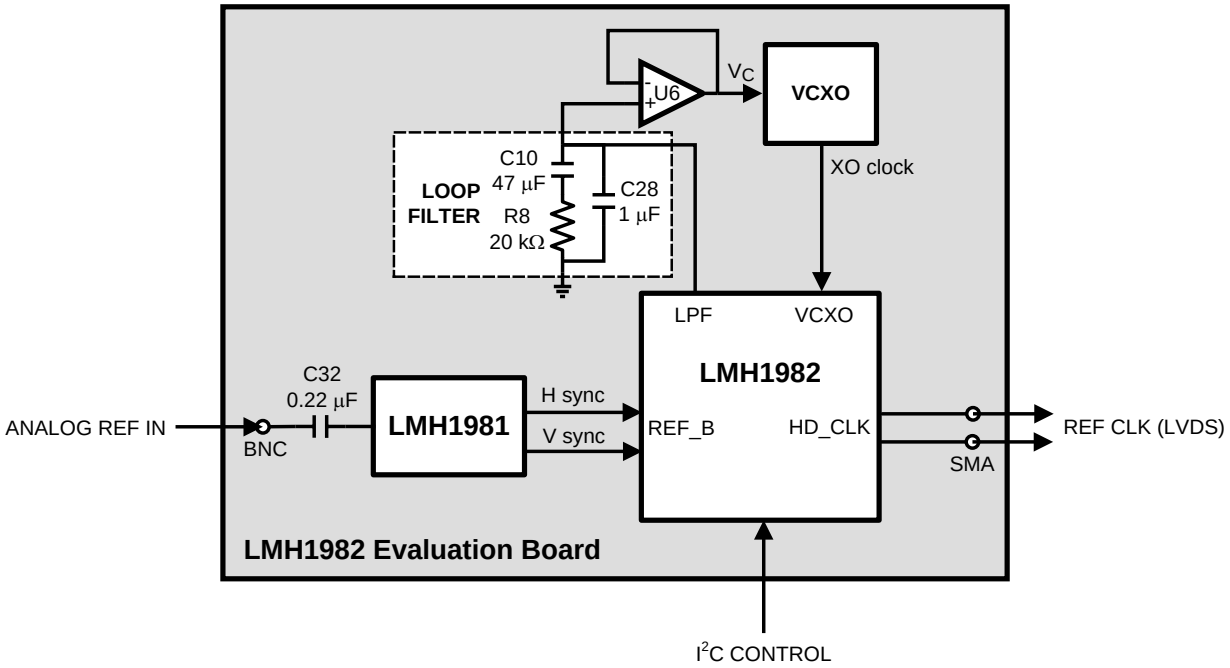

Figure 3. LMH1982 Evaluation Board With Loop Filter Implementation

To design the loop response, it was critical to initially identify and analyze the fundamental jitter characteristics related to PLL 1: 1) VCXO clock jitter requirement, 2) input H sync jitter amplitude and frequencies, and 3) jitter transfer function characteristics.

- The VCXO clock jitter was targeted for no greater than 20 ps p-p to minimize jitter degradation on the output clock. This was denoted in the clock jitter spec test conditions in the *LMH1982 Multi-Rate Video Clock Generator With Genlock Data Sheet* (SNLS289).
- The input H sync jitter was expected to occur predominantly at the reference input line and frame rates, and have jitter amplitude no greater than 2 ns p-p. To realize this level of input jitter, the LMH1981's input coupling capacitor (C32) value was modified to 0.22 µF, as indicated in the *LMH1982 Multi-Rate Video Clock Generator With Genlock Data Sheet* (SNLS289).
- The jitter transfer function for PLL 1 exhibits a roll-off rate of −40 dB/decade at frequencies much higher than the −3 dB BW (above 1 decade). At frequencies near the BW, peaking in the transfer function can be minimized by maintaining a DF value between 0.707 and 1.0.

Based on the above analysis, it was determined to set the BW to 3 Hz to provide at least 40 dB of jitter attenuation at frequencies at 25-30 Hz (reference input frame rate) and above. The DF was set to at least 0.80 to ensure good loop stability and minimal jitter peaking. Using the loop response design methodology and design equations (below) (from the *LMH1982 Multi-Rate Video Clock Generator With Genlock Data Sheet* (SNLS289)), the loop filter component values were derived (see R8, C10, and C28 in Figure 3).

$$BW = I_{CP1} * R_S * K_{VCO} / FB\_DIV \quad (1)$$

$$DF = R_S / 2 * \text{sqrt} (I_{CP1} * C_S * K_{VCO} / FB\_DIV) \quad (2)$$

where:

I_{CP1} — Nominal PLL 1 charge pump current (programmable)

R_S — Nominal resistor value of R8

K_{VCO} — 1000 Hz/V VCXO gain for CTS VCXO p/n 357LBC27M0000

FB_DIV— Feedback divider value

C_S — Nominal capacitor value of C10

The estimated loop response characteristics for PLL 1 are shown in Table 3. In order to maintain consistent BW and DF values across all reference input formats, the charge pump current for PLL 1 needed to be programmed accordingly for each format using the LMH1982 GUI.

Table 3. Estimated PLL 1 Loop Response Characteristics

Reference Input Format	NTSC	PAL	1080i 59.94	1080i 50
Reference Divider	1	1	5	1
Feedback Divider	1716	1728	4004	800
ICP1 Control Register Setting (decimal)	8	8	19	4
ICP1 Current	250 µA	250 µA	594 µA	125 µA
Est. Loop Bandwidth	3 Hz	3 Hz	3 Hz	3 Hz
Est. Damping Factor	0.83	0.82	0.83	0.86

A.1 Loop Filter Capacitors

It is suggested to use tantalum capacitors for C10 and C28 instead of ceramic capacitors in the PLL loop filter, which is a sensitive analog circuit. Ferroelectric ceramics, such as X7R, X5R, Y5V, Y5U, and so forth exhibit piezoelectric effects that generate electrical noise in response to mechanical vibration and shock. This electrical noise can modulate the VCXO control voltage and consequently induce clock jitter at high amplitudes when the board and ceramic components are subjected to vibration or shock. Tantalum capacitors can be used to mitigate this effect.

Appendix B SDI Eye and Jitter Plots

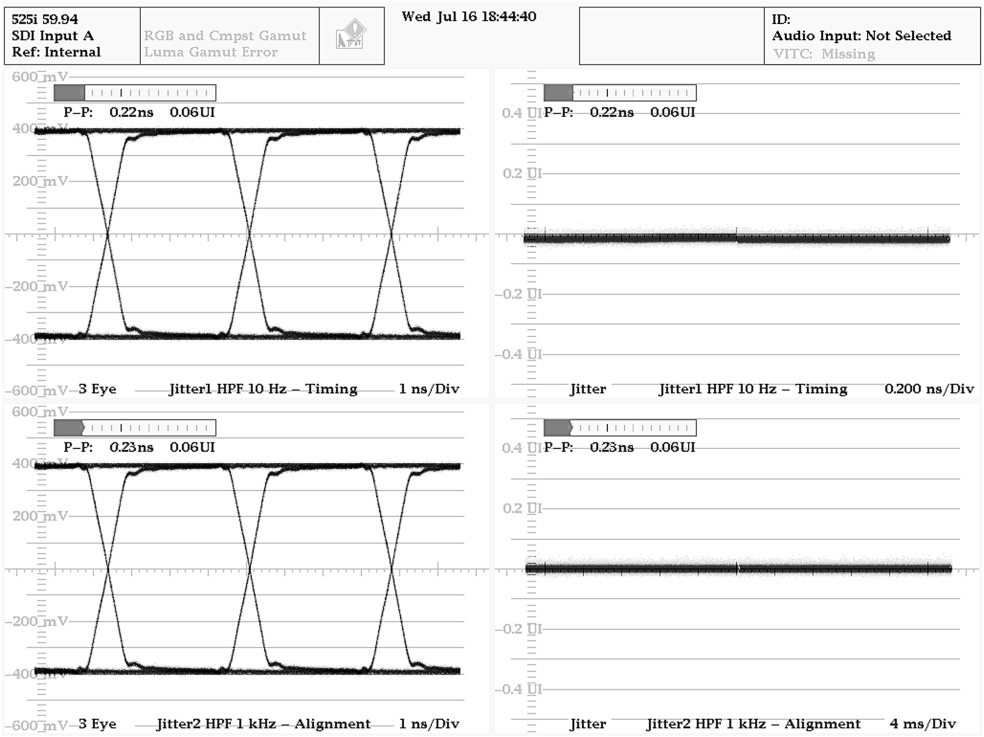

Figure 4. 525i 59.94 SDI Output Upper Plots: Timing Jitter HPF Lower Plots: Alignment Jitter HPF

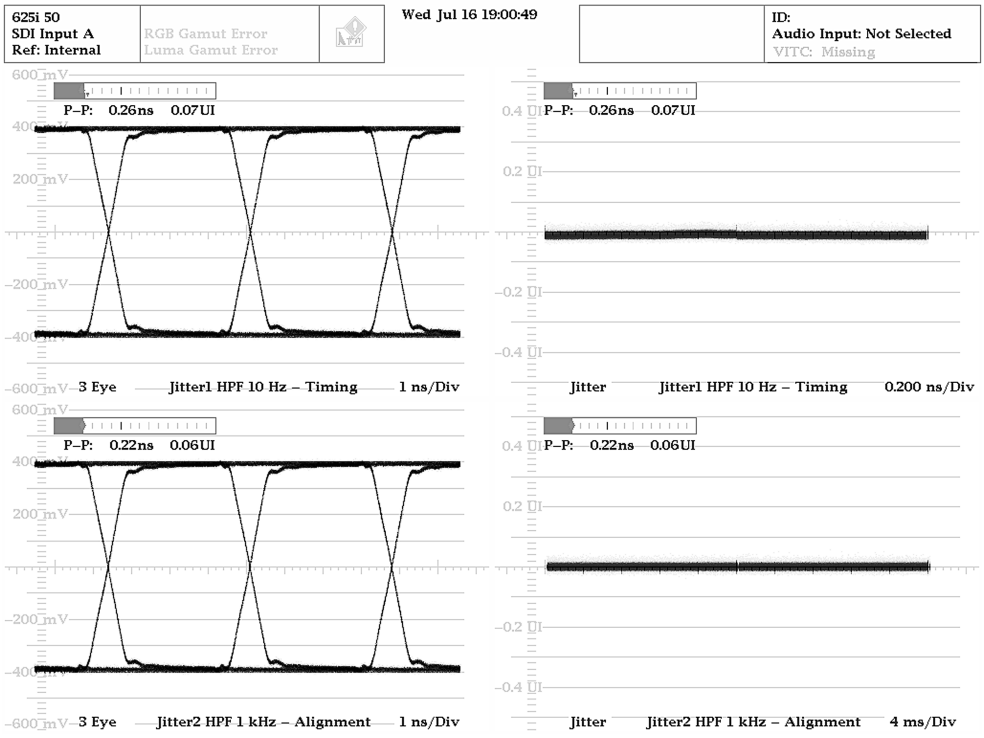

Figure 5. 625i 50 SDI Output Upper Plots: Timing Jitter HPF Lower Plots: Alignment Jitter HPF

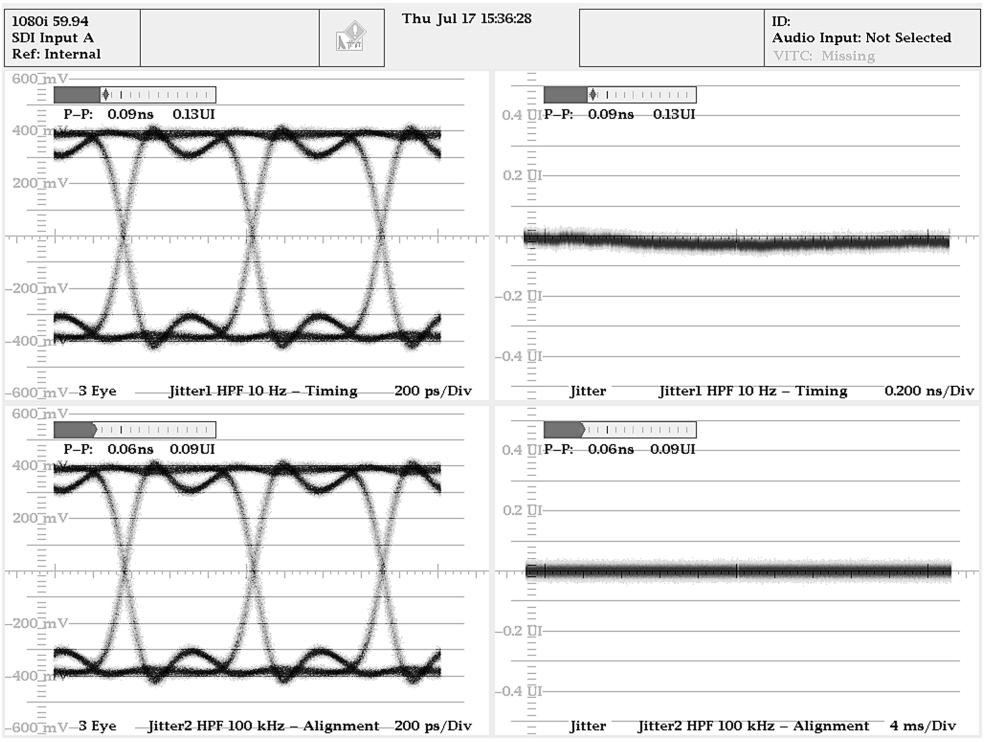

Figure 6. 1080i 59.94 HD-SDI Output Upper Plots: Timing Jitter HPF Lower Plots: Alignment Jitter HPF

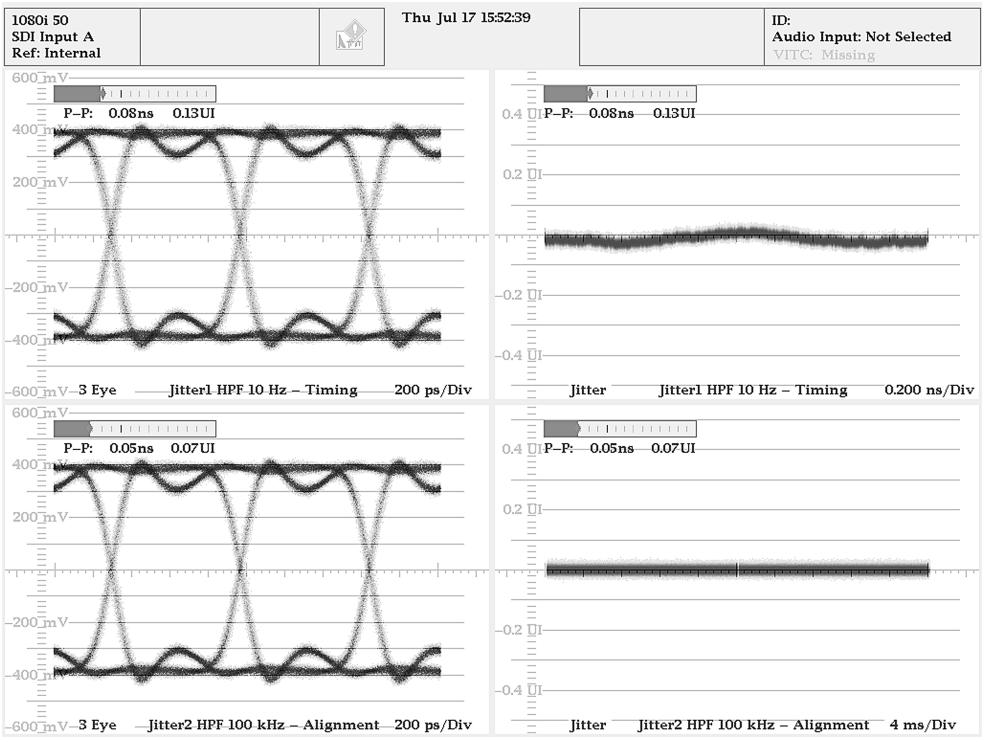

Figure 7. 1080i 50 HD-SDI Output Upper Plots: Timing Jitter HPF Lower Plots: Alignment Jitter HPF

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265