Application Report
SNAA061C–June 2008–Revised April 2013

AN-1865 Frequency Synthesis and Planning for PLL Architectures

ABSTRACT

This application report demonstrates the importance of understanding the least common multiple (LCM) and greatest common divisor (GCD).

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1 Introduction

In many applications, it is desired to generate a set of frequencies from a single source frequency. This source could be a temperature controlled crystal oscillator (TCXO), a clock recovered from data, a recovered signal from GPS, or anything else that generates a fixed frequency. The set of frequencies generated could be several simultaneous fixed frequencies or a single frequency that is tunable. There may also be intermediate frequencies that need to be chosen, such as for the VCO (Voltage Controlled Oscillator) or the phase detector (PD). Frequency planning is the selection of these frequencies in an optimal way.

One common situation in frequency planning is when there is a need to create many fixed frequencies from a single VCO frequency. In this situation, all frequencies must divide into the VCO frequency. For example, one could create 12.288 MHz and 30.72 MHz outputs from a single VCO frequency of 61.44 MHz as shown in Figure 1, by dividing the 61.44 MHz VCO frequency by 5 and 2 respectively.

A second situation that often arises is when there are two fixed frequencies that both must be divided down to the same frequency, such as the phase detector frequency of a PLL. Consider a PLL with an input frequency of 12.288 MHz and a desired output frequency of 30.72 MHz. For optimal performance, it is desirable to find the highest possible phase detector frequency, which can divide into both fixed frequencies. In this case, the phase detector would be 6.144 MHz - also shown in Figure 1.

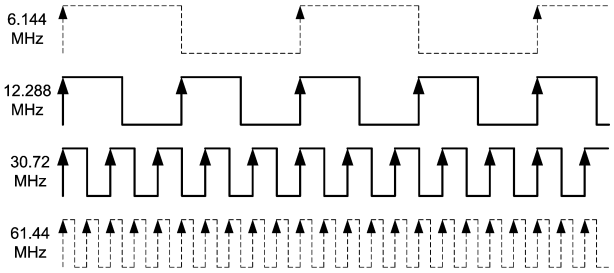

Figure 1. Illustration of GCD and LCM

These examples demonstrate the importance of understanding the least common multiple (LCM) and greatest common divisor (GCD). These concepts are traditionally taught using just whole numbers, but it becomes very useful to expand these concepts to positive rational numbers, like 12.288 and 30.72, to make them more applicable to frequency planning.

2 Least Common Multiple (LCM) and Greatest Common Divisor (GCD)

The least common multiple (LCM) of two or more numbers is the least positive number that is a multiple of each number. For instance, the least common multiple of 12 and 20 is 60. To simplify the LCM calculation, any argument can be disregarded if it divides evenly into any of the other arguments. Following are some examples that show how this principle can be applied.

$$\text{LCM}(5, 10) = \text{LCM}(10) = 10 \quad (1)$$

$$\text{LCM}(19.68, 30.72, 61.44) = \text{LCM}(19.68, 61.44) = 2519.04 \quad (2)$$

See Table 1.

The greatest common divisor (GCD) of two or more numbers is the greatest number that will divide all of them. For example, the GCD (63,18) = 9. To simplify the GCD operator, any argument can be disregarded if it is a multiple of one of the other arguments. Following are some examples that show the application of this concept.

$$\text{GCD}(5, 10) = \text{GCD}(5) = 5 \quad (3)$$

$$\text{GCD}(19.68, 61.44, 122.88) = \text{GCD}(19.68, 61.44) = 0.48 \quad (4)$$

See Table 1.

Once the LCM and GCD are simplified using the previous principles, there is a simple method that can be used to simultaneously calculate them. This method involves listing out all the common factors in a factor table as shown in Table 1. The GCD is the product of these common factors, and the LCM is the product of the common factors times the remaining factors.

Table 1. Calculation of GCD and LCM

Common Factor	Remaining Factor	Remaining Factor
	19.68	61.44
0.01 = 1/100	1968	6144
4	492	1536
4	123	384
3	41	128
Final Remaining Factor	41	128
GCD	0.01 × 4 x 4 × 3 = 0.48	
LCM	0.48 × 41 × 128 = 2519.04	

The factor table method is good for most cases in frequency planning, since crystal and output frequencies are often expressed in terms of non-repeating decimals. In this case, the first common factor (0.01 in this case) is obvious. For other cases where the fractions are non-terminating decimals the first common factor would be a fraction. For example, to calculate LCM(10/3, 236/7), the first common factor would be 1/21. Although the factor table could be used in this case, there is a more elegant method that could also be used. The first step of this method is to find two integer constants, p and q, such that:

$$\text{LCM}(10/3, 236/7) = p \times 10/3 \quad (5)$$

$$\text{LCM}(10/3, 236/7) = q \times 236/7 \quad (6)$$

Dividing the first equation by the second one and reducing to a lowest terms fraction:

$$p/q = (236/7) / (10/3) = (236 \times 3) / (7 \times 10) = 354/35 \quad (7)$$

Now that it is known that p = 354, it can be substituted back in to calculate:

$$\text{LCM}(10/3, 236/7) = 354 \times 10/3 = 3540/3 = 1180 \quad (8)$$

The GCD can also be calculated using similar reasoning:

$$(10/3) / \text{GCD}(10/3, 236/7) = p \quad (9)$$

$$(236/7) / \text{GCD}(10/3, 236/7) = q \quad (10)$$

$$p/q = (10/3) / (236/7) = 35/354 \quad (11)$$

$$\text{GCD}(10/3, 236/7) = (10/3) / p = (10/3) / 35 = 2/21 \quad (12)$$

If there are more than two numbers involved, this method can be applied multiple times to get the result. Provided the ratio of the numbers is rational, the LCM and GCD can be calculated using one of the methods presented in this section. For pathological cases where the ratio of the numbers is not rational, LCM and GCD are undefined. From here on, it will be assumed the reader is comfortable dealing with LCM and GCD. If no units are stated and frequencies are being dealt with, it will be assumed the units are in MHz.

3 Frequency Planning for Various Architectures

This section goes over many of the different possible architectures that can be used to generate a set of frequencies. Although there are many different architectures, they are often combinations of a source frequency (f_{OSC}), phase detector frequencies (f_{PD}), VCO frequencies (f_{VCO}), and divider frequencies (f_{OUT}). The source frequency is always present in any architecture, but the other building blocks may or not be there.

3.1 Single PLL

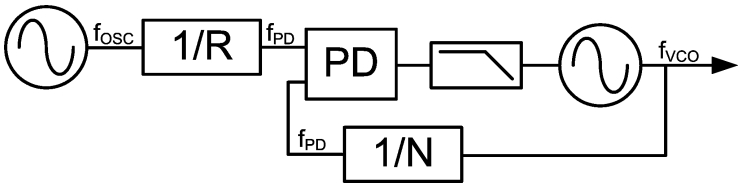

Figure 2. Basic PLL Architecture

In the Single PLL architecture (Figure 2), the source frequency, f_{OSC}, is divided down by a fixed value, R, in order to achieve a fixed phase detector frequency of f_{PD}. The VCO frequency, f_{VCO}, is divided down by a fixed value, N, in order to also generate the same phase detector frequency. The phase detector frequency therefore satisfies the following equations:

$$f_{PD} = f_{VCO} / N \quad (13)$$

$$f_{PD} = f_{OSC} / R \quad (14)$$

These relationships can be restated as:

$$f_{VCO} = f_{OSC} \times N/R \quad (15)$$

$$N/R = f_{VCO} / f_{OSC} \quad (16)$$

If desired, the VCO frequency can be tuned by changing the N counter value. This allows the generation of a whole set of frequencies from a single frequency. The frequency accuracy of the VCO is as good as that of the source frequency and there is also a precise phase relationship between the VCO and the source frequency, f_{OSC}.

Because the N divider value multiplies the noise of the phase detector, it is desirable to minimize this N divider value, which is equivalent to maximizing the phase detector frequency. Another benefit of maximizing the phase detector frequency is that it pushes reference spurs out to higher frequencies, which are easier to filter. Reference spurs are spurious tones visible in the frequency domain that occur at an offset from the carrier equal to the phase detector frequency.

Where the VCO frequency, f_{VCO}, is fixed, the values for the N and R counter can be found by reducing the fraction f_{VCO}/ f_{OSC} to a lowest terms fraction. This gives the minimum possible value for N and therefore the highest phase detector frequency. This theoretical maximum possible phase detector frequency is calculated as:

$$f_{PD} = GCD (f_{OSC}, f_{VCO}) \quad (17)$$

In some applications, there may be the option of choosing the source frequency, f_{OSC}. In this case, it is often good to choose one that maximizes the phase detector frequency by choosing it to maximize GCD (f_{OSC}, f_{VCO}). For TCXOs (Temperature Compensated Crystal Oscillators) and crystals, to a point, it is good to have a higher frequency and divide this down, since this also divides down the noise of this source. One also needs to be aware the part being used may have restrictions on the maximum phase detector frequency or minimum values for N and R that could cause one to have to reduce this phase detector frequency. For some parts, the R counter does divide all the way down to one, but others have a larger minimum restriction on this. For the N counter, prescalers are often used to handle the higher frequency

operation. These prescalers put restrictions on the divide values that can be produced by these counters. There will typically be a continuous range of divide values that can be produced. Below this, there could be allowable values, but they will be discontinuous. Consider the example where one wants to generate 245.76 MHz signal. The source frequencies available are 10 MHz, 30.72 MHz, and 61.44 MHz. Assume the PLL to be a LMX2306 with the specifications in Table 2.

Table 2. Single PLL Example

Parameter	Allowable Values
Source Input Frequency	5 – 100 MHz
VCO Input Frequency	25 – 550 MHz
Phase Detector Frequency	≤ 10 MHz
R Divider	3-16383
N Divider	24-27
	32-36
	40-45
	48-54
	56-65535

The first step is to choose the source frequency. From the available values of 10, 30.72, and 61.44 MHz, 61.44 MHz has the largest GCD value with the output frequency of 245.76 MHz and meets the input requirements for the part. From Table 2, it is obvious that the VCO and source are within the operating range of the part. Now that this is satisfied, the theoretical N and R values can be calculated as:

$$N/R = 245.76/61.44 = 4/1 \quad (18)$$

So the theoretical solution would be to set N to 4 and R to 1, but these are both below the minimum values allowed for the N and R counter. Furthermore, the 10 MHz maximum phase detector rate implies the R counter must be at least 7. If we were to multiply both N and R by 7, then the R counter and phase detector rate requirements would be met, but the N counter would be 28, which is not allowable. The solution that does work is to use an N value of 32 and an R value of 8. This implies a phase detector rate of:

$$f_{PD} = 61.44 \text{ MHz}/8 = 7.68 \text{ MHz} \quad (19)$$

The same result could be obtained by first calculating the phase detector frequency as GCD (245.76, 61.44) = 61.44 MHz, and then dividing this value down until the divider and phase detector requirements are met.

One observation is that because the counter values and phase detector frequency specifications are limiting the phase detector frequency, one could also get the same phase detector frequency from a 30.72 MHz source. This would be a perfectly acceptable solution. However, the 61.44 MHz solution might have better noise performance because this frequency is being divided down by a bigger value of R.

Another circumstance of the basic PLL architecture is where the VCO actually tunes across a band of several frequencies with a channel spacing of f_{CH}. The theoretical maximum phase detector frequency can be found as:

$$f_{PD} = \text{GCD}\ (f_{OSC}, f_{CH}) \quad (20)$$

For example, consider an application where it is desired to generate the frequencies of 902 MHz, 903 MHz, … , 928 MHz from a 10 MHz crystal. In this case, the channel spacing and phase detector frequency are GCD (10 MHz, 1 MHz) = 1 MHz. When the N counter is changed by one, the VCO frequency changes by 1 MHz. Now consider what would happen if the crystal was changed to 14.4 MHz. in this case, the phase detector frequency would be:

$$f_{PD} = \text{GCD}\ (14.4 \text{ MHz}, 1 \text{ MHz}) = 0.2 \text{ MHz} \quad (21)$$

In either case, once the phase detector frequency is known, the R and N counter values can also be quickly found. If there is freedom to choose the source, then it is ideal to choose it to maximize this GCD value.

There are also some applications where there might be only 2 or 3 output frequencies required based on the mode of operation for the device. In this case, the phase detector frequency can be optimized for each frequency. If the phase detector frequency changes a lot, then the charge pump gain can also be used to compensate for this. The key is to keep the following expression from changing too much:

$$K_{PD} \times K_{VCO} / N \quad (22)$$

K_{PD} is the charge pump gain in mA/rad, K_{VCO} is the VCO gain in MHz/V, and N is the N Counter value. Another way to say this is to make the charge pump gain inversely proportional to the phase detector frequency.

For example, suppose a part has 16 levels of charge pump gain (that is, 1X, 2X, …, 16X). Assume a 10 MHz crystal and the output frequencies of 902 and 902.5 MHz are desired. One approach would be to choose a phase detector frequency of 0.5 MHz, but this would not give the best performance. Another approach would be to use 2 MHz for the 902 MHz and 2.5 MHz for the 902.5 MHz.

In Table 3, although the phase detector frequency is changing, the charge pump gain is changing such that the product of these two quantities is a constant. In some cases, the programmable charge pump current may not have enough resolution to keep this product perfectly constant, it can keep this product from changing too much.

Table 3. Calculated Phase Detector Frequencies

Output Frequency	K_{PD}	f_{PD}
902 MHz	15 X	2 MHz
902.5 MHz	12 X	2.5 MHz

In summary, the single PLL architecture is fundamental to creating fixed or tunable frequencies. A lot of the frequency planning involves calculating the highest possible phase detector frequency that does not violate the usable conditions of the part. If the VCO has many frequencies to achieve, it is typical to keep the phase detector constant. If there are just a few, sometimes the phase detector frequency can be adjusted for each frequency. In this case, the charge pump current can also be used to keep the PLL well optimized.

3.2 Dual PLL

One common place where the Dual PLL architecture (Figure 3) is used is in superheterodyne receivers, where one VCO produces a frequency that can tuned across some frequency band and the other one produces a fixed frequency. This architecture is very much like two separate single PLL architectures except the source frequency is typically common to both PLLs. If there is freedom to choose the source frequency, then there are choices in maximizing the phase detector frequency. In the superheterodyne architecture, the fixed frequency PLL typically has less stringent requirements, so it makes sense to optimize the tunable frequency PLL. If both are equally important, then one might want to try to maximize GCD (f_{OSC},f_{VCO1},f_{VCO2}).

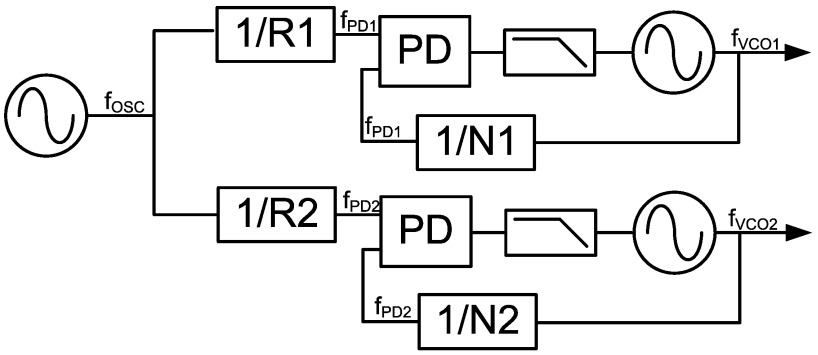

Figure 3. Dual PLL Architecture

3.3 Fractional N PLL

So far it has been assumed that all the counters can only assume integer values. If the N counter value is allowed to assume a fractional value, then this allows a higher phase detector frequency and therefore better performance. For purposes of frequency planning, the fractional word, Fnum/Fden, is the fractional part of the N divider value and is assumed to be a lowest terms fraction. In order to achieve the highest possible phase detector frequency, Fden should be chosen as large as possible.

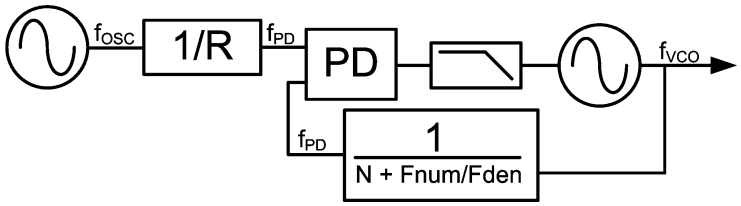

Figure 4. Fractional PLL Architecture

The output frequency for the Fractional N architecture can be calculated as:

$$f_{VCO} = f_{OSC} \times (N + Fnum/Fden)/R \quad (23)$$

The fractional denominator, Fden, is typically very flexible. The basic method to find this is to divide the source frequency by the phase detector frequency that would be achievable with an integer PLL:

$$Fden_{MAX} = f_{OSC} / f_{PD} = f_{OSC} / GCD (f_{OSC}, f_{CH}) \quad (24)$$

If this theoretical value is not supported by the part, then one should choose the largest available value the part supports that divides $Fden_{MAX}$. Once the value for Fden is chosen, the frequencies can be solved by treating the part as a basic PLL with the channel spacing multiplied by Fden.

$$f_{PD} = GCD (f_{OSC}, Fden \times f_{CH}) \quad (25)$$

For example, consider the case that a 14.4 MHz crystal used with the LMX2354 PLL to generate the frequencies of 902 MHz to 928 MHz with a 1 MHz channel spacing. Assume the PLL to have the specifications in Table 4.

Table 4. Fractional PLL Example

Parameter	Allowable Values
f_{OSC}	2-50 MHz
f_{VCO}	500-2500 MHz
f_{PD}	≤ 10 MHz
Fden	15 or 16
R Divider	1 - 32767
N Divider	40 - 32767

In this case, the ideal fractional denominator would be 14.4/GCD (14.4,1) = 14.4/0.2 = 72. This part does not support a fractional modulus of 72, so therefore you need to choose a the highest fractional modulus that divides into 72. In this case, a fractional modulus of 8 could be realized by using the modulus 16 mode and stepping the fractional numerator in steps of 2. So for this part, a fractional modulus of 8 could be chosen. The phase detector frequency would be 1.6 MHz. A quick check of the requirements of this part shows this does not violate minimum continuous divide or maximum phase detector requirements.

More modern fractional PLLs tend to be of the delta-sigma architecture, that support much more fractional denominators. One example of this would be the LMX2485 PLL. In addition to excellent performance and a very flexible fractional denominator, this part also has a frequency doubler that can be software enabled for the source frequency. The specifications for this part are in Table 5.

Table 5. Delta Sigma Fractional PLL Example

Parameter	Allowable Values
f_{OSC}	5 – 110 MHz (Doubler Disabled) 5 – 20 (Doubler Enabled)
f_{VCO}	500-3000 MHz
f_{PD}	≤ 50 MHz
Fden	1-4194303
R Divider	1-4095
N Divider	31-2039

If you consider the same example, the 14.4 MHz source frequency could be doubled to 28.8 MHz. From this, GCD (28.8 MHz, 1 MHz) = 0.4 MHz and 28.8/0.4 = 72. The ideal fractional denominator is therefore 72, which implies the ideal phase detector frequency is 28.8 MHz. A quick check shows there are no violations with this part. In general, when the fractional denominator is very flexible, the phase detector frequency often ends up being the source frequency (or doubled source frequency in this case).

In summary, fractional parts allow a higher phase detector frequency by allowing the N Counter value to be a fraction. This advantage is greatest when the channel spacing is very small, or when the source frequency is something that would otherwise force a low phase detector rate.

3.4 PLL with VCO Divider

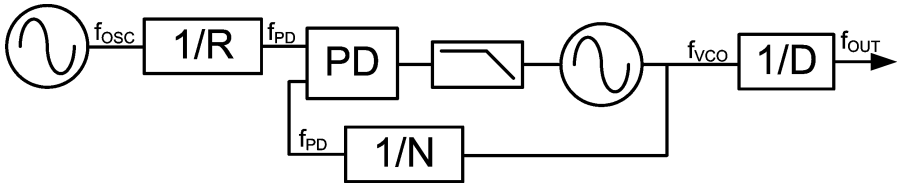

Figure 5. PLL with VCO Divider

One common addition to the PLL architecture is to add a divider after the VCO (see Figure 5) in order to make the product more flexible and able to reach lower frequencies. It is also true that lower frequency VCOs frequencies require larger inductors, which are difficult for VCOs that are integrated on silicon. The output frequency can be found as:

$$f_{OUT} = f_{VCO} / D = f_{OSC} \times N/(R \times D) \quad (26)$$

Typically, the VCO tuning range will restrict the value of D that can be used to get a set of output frequencies to a single value. If there is any degree of freedom, the best performance typically comes when the divide value D is maximized and the R Counter value is minimized. However, this typically also consumes more current because the VCO and counters are working at higher frequency. In addition to dividing the VCO frequency by a factor of D, the channel spacing is also divided down by this factor. For instance, if D = 2, then the VCO channel spacing could be twice the channel spacing needed in the actual application. This allows the advantage of a higher phase detector frequency which translates into better noise and spur performance, provided the source frequency does not prevent this. Mathematically, this is similar to the case of a fractional PLL with the differences being that the fractional denominator is typically not flexible but has no added noise or spurs.

$$f_{PD} = GCD (f_{OSC}, D \times f_{CH}) \quad (27)$$

It is also possible to put a divider after a fractional PLL (see Figure 6). In this case, this allows even more flexibility and also can eliminate and reduce fractional spurs. The LMX2531 family is a good example of this. It includes an integrated VCO which can be divided by 1 or 2. When the divide by 2 is enabled, there are performance advantages for the fractional spurs. In addition to this, issues with frequency pulling can also be reduced since the true VCO frequency and output frequency of the device are different.

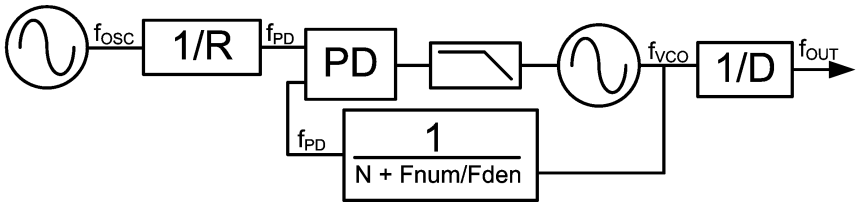

Figure 6. Fractional PLL with VCO Divider

3.5 Basic Timing Device

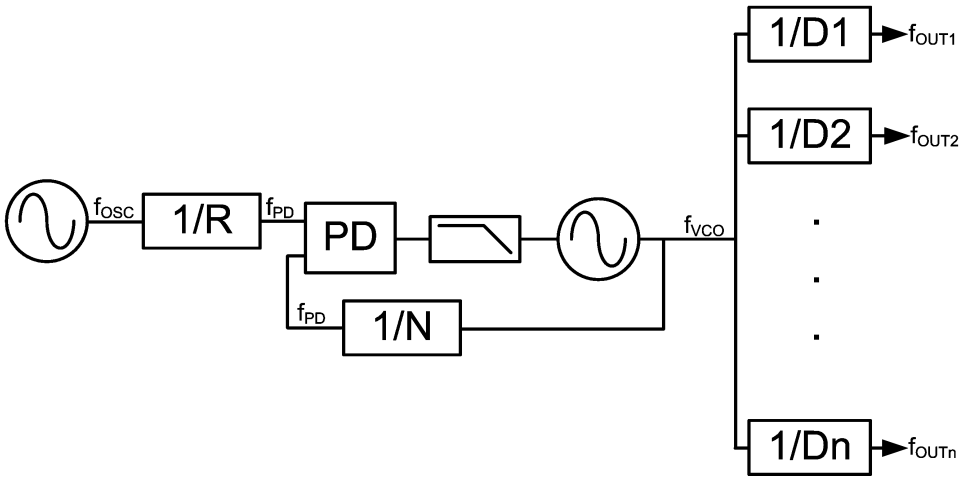

Figure 7. Basic Timing Device

In this architecture, the VCO is divided by multiple dividers in order to create several simultaneous and different frequencies. These parts are typically used to produce a set of fixed frequencies from a fixed VCO frequency. Since all of the output frequencies are derived from the same VCO frequency:

$$f_{VCO} = k \times LCM\ (f_{OUT1}, f_{OUT2}, \ldots, f_{OUTn}),\ \text{where } k = 1,2, \ldots \quad (28)$$

This relationship is typically enough to figure out if a VCO can hit the frequency range. For instance, suppose frequencies of 14.4, 30.72, 61.44, and 122.88 MHz are desired. LCM (14.4, 30.72, 61.44, 122.88) = LCM (14.4, 122.88) = 1843.2 MHz. So the VCO frequency needs to be 1843.2 MHz, or some higher multiple. Knowing the LCM frequency can quickly guide one to determine what part can be usable in an application. If this number turns out to be something that is too high frequency for a VCO to produce, one might consider using a different architecture, perhaps one with two different VCOs. The LMK02000 family of parts requires an external VCO and is a good example of a timing device.

One variation of the clock conditioner architecture is when an additional divider is between the VCO and the output dividers (see Figure 8). The reason why this is done is that only the divider directly after the VCO needs to be able to handle the high VCO frequencies, the other divider can be lower frequency dividers. Also, it also can be used to make more controlled phase relationship between the input and the output, since the delay and random phase state of this divider is tracked out by the PLL loop.

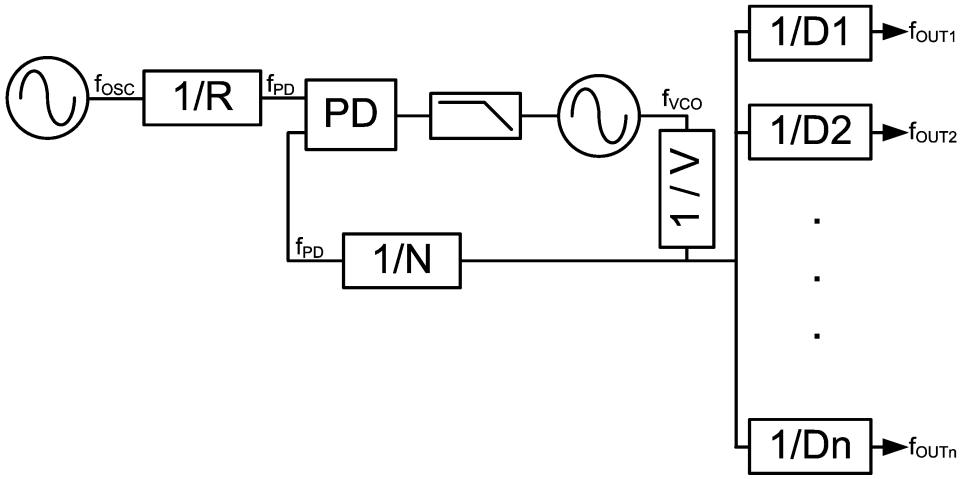

Figure 8. Basic Timing Device with VCO Divider

The frequency planning for this architecture is very similar to the case where there is no divider directly after the VCO with the exception that it does force a common factor. In the previous example where the VCO frequency was 1843.2 MHz, the total divide can be calculated as shown in Table 6.

Table 6. Calculating Total VCO Divide

VCO Frequency	Output Frequency	Total VCO Divide
1843.2 MHz	14.4 MHz	128
	30.72 MHz	60
	61.44 MHz	30
	122.88 MHz	15

The VCO divider value, V, must divide all the total divide values. In other words, V must divide GCM (128,60,30,15) = GCM (128,15) = 1. So the VCO divider would have to divide one, which means it would have to be one. So unless the VCO divider could be bypassed, this architecture could not be usable. If the 14.4 MHz output was not needed, then this would resolve this issue.

Consider another example where the frequencies of 12.288, 61.44, and 76.8 MHz are to be generated from a 10 MHz source. LCM (12.288, 61.44, 76.8) = LCM (61.44 , 76.8) = 307.2 MHz. For the three parts shown in Table 7, 307.2 MHz is outside the VCO frequency range, so therefore a multiple needs to be used. Since the VCO frequency needs to be a multiple of 307.2 MHz, this rules out the LMK03002.

Table 7. LMK03000 Series Parameters

Part	VCO Range	Allowable VCO Divider Range	Allowable Channel Divider Range
LMK03000	1185 – 1296 MHz	2,3,4,5,6,7,8	1,2,4, … 510
LMK03001	1470 – 1570 MHz	2,3,4,5,6,7,8	1,2,4, … 510
LMK03002	1566 – 1720 MHz	2,3,4,5,6,7,8	1,2,4, … 510

Once the VCO is chosen, the total divide between the VCO and the output can be calculated, see Table 8. This is necessary to ensure there are no issues violating divider values.

Table 8. LMK03000 Series Example

Part	VCO Frequency	Output Frequency	Total Divide	VCO Divide	Channel Divide
LMK03000	1228.8 MHz	61.44 MHz	20	2	10
				4	None (5 not allowed)
		76.8 MHz	16	2	8
				4	4
LMK03001	1536 MHz	61.44 MHz	25	5	None (5 not allowed)
		76.8 MHz	20		4
LMK03002	Not Possible	n/a			

For the LMK03000, GCD (20,16) = 4, so the VCO divide must divide 4, which leaves the possibilities of 2 and 4. For the LMK03001, the only possible VCO divide is 5. After the VCO divider is chosen, then the channel divide also needs to be verified. For the VCO divide of 4 for the LMK03000, this leads to a channel divide of 5, which is not allowed, leaving only the choice of a VCO divide of 2. For the LMK03001, the only possible VCO divide is 5, but this leads to a channel divide by 5, which is not supported. This rules out the LMK03001.

So among these three parts, there is only one possible part and one possible configuration, which is the LMK03000 with a VCO divide of 2. Given the source frequency is 10 MHz, now the maximum phase detector frequency needs to be calculated as f_{PD} = GCD (10, 1228.8) = 0.4 MHz. Since the VCO divider is 2, the total N divider must also have a factor of 2. In this case, the total N divider value is 1228.8/0.4 = 3072, which would mean the VCO divide = 2 and the N divide = 1536.

3.6 Dual Loop

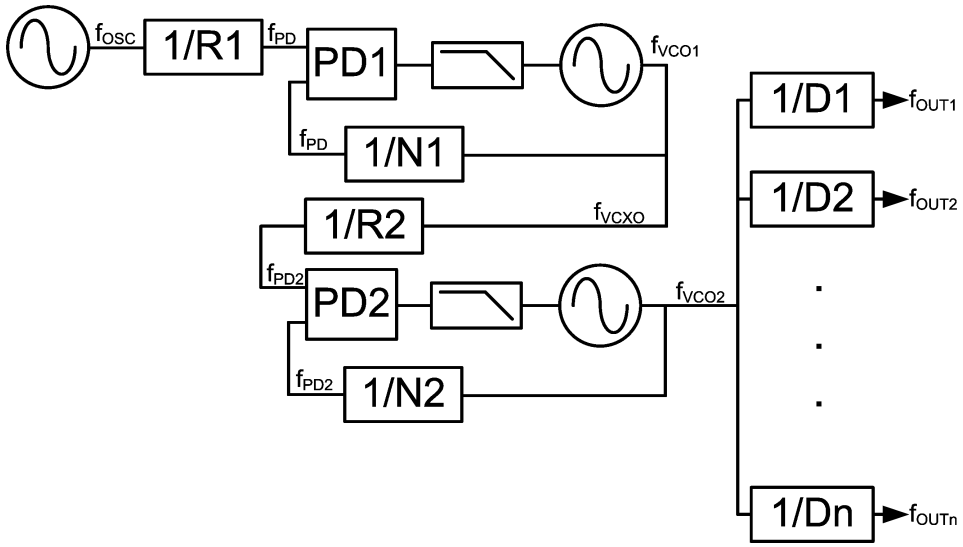

Figure 9. Dual Loop Architecture

The dual loop architecture (Figure 9) is typically used when the source frequency is not clean and offers excellent noise performance and good frequency flexibility at the same time. In this architecture, there are actually two tunable oscillators. The first one (VCO1) is typically a VCXO (Voltage Controlled Crystal Oscillator) with a fixed frequency and good phase noise that is used to clean up a dirty source signal. The second one (VCO2) is a standard VCO that is typically higher frequency with less stringent phase noise requirements. The phase detector frequency is not important for the PD1, since the noise of the source and VCO1 typically dominate over the noise produced by PD1. Because this phase detector frequency is not important, the source frequency is typically not considered in the equations. The output frequency relates to the first VCO frequency as:

$$f_{VCO1} \times N2/R2 = f_{VCO2} = k \times LCM(f_{OUT1}, \ldots f_{OUTn}), \text{ where } k = 1,2, \ldots \quad (29)$$

Choosing the frequency for f_{VCO1} is an art. It is good to maximize the phase detector frequency of PD2. However, since this is typically a VCXO (Voltage Controlled Crystal Oscillator), there may be certain frequencies cheaper and easier to obtain than others. In order to compare several different frequencies for f_{VCO1}, the frequency relationship needs to be analyzed. The best f_{VCO1} frequency choice would be one that had the largest common factor with f_{VCO2} which is equivalent to maximizing GCD (f_{VCO1}, f_{VCO2}).

Suppose the desired frequencies were 12.288 and 30.72 MHz. Also assume f_{VCO1} is free to choose and f_{VCO2} has a tuning range of 1430 – 1570 MHz. f_{VCO2} is therefore a multiple of LCM (12.288, 30.72) = 61.44 MHz. This means f_{VCO2} can be 1474.56 MHz or 1536 MHz. Once the f_{VCO2} and f_{VCO1} frequencies are known, the maximum phase detector frequency can be calculated as GCD (f_{VCO1}, f_{VCO2}) as shown in Table 9.

Table 9. Dual Loop Example

f_{VCO1}	Maximum Possible f_{PD2} with	
	f_{VCO2} = 1474.56 MHz	f_{VCO2} = 1536 MHz
10 MHz	0.08 MHz	2 MHz
14.4 MHz	2.88 MHz	0.96 MHz
30.72 MHz	30.72 MHz	30.72 MHz
100 MHz	0.16 MHz	4 MHz
122.88 MHz	122.88 MHz	61.44 MHz

4 Conclusion

Frequency planning involves choosing frequencies to make a part usable with optimal performance. If there are many possible configurations, it is often a good idea to maximize the phase detector frequency of the PLL to achieve the best phase noise performance. The concepts of least common multiple (LCM) and greatest common divisor (GCD) are fundamental concepts to help calculate frequencies. Many different architectures have been presented, but this list is in no way exhaustive as there are many possible permutations.

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