Application Report
SNAA065A–March 2009–Revised April 2013

AN-1939 Crystal Based Oscillator Design with the LMK04000 Family

ABSTRACT

This application report for the LMK04000 family of clock conditioners covers the design of an external oscillator circuit using a crystal resonator.

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1 Introduction

The LMK04000 family supports either an external, self-contained VCXO module or a discretely implemented voltage controlled crystal oscillator based upon a crystal resonator. The LMK04000 family features an internal loop amplifier that enables the implementation of the crystal oscillator. In many applications, the crystal resonator option will offer a cost effective method for cleaning the jitter of the incoming reference clock. In this application note, we will first review basic oscillator circuit fundamentals, and along the way highlight certain specifications for crystals which are critical to the design of the oscillator circuit. It also examines some important aspects of circuit operation. A reference design is presented along with examples of measured performance. A suggested design procedure is presented along with specific LMK040xx programming required for crystal oscillator implementations.

1.1 LMK04000 Clock Conditioner Family

The LMK04000 family of precision clock cleaners employs a cascaded phase locked loop (PLL) architecture to achieve its highly effective jitter cleaning and frequency synthesis. Figure 1 illustrates the dual PLL architecture of the LMK04000.

In other application reports we have discussed in detail how jitter cleaning is accomplished using a cascaded loop architecture. The key to building a jitter cleaning clock solution with a LMK040xx clock conditioner is to substitute the phase noise of the external oscillator paired with PLL1 for the phase noise of the incoming reference clock. The performance of this external oscillator is critical to the overall performance of the clocks at the output of the LMK040xx device.

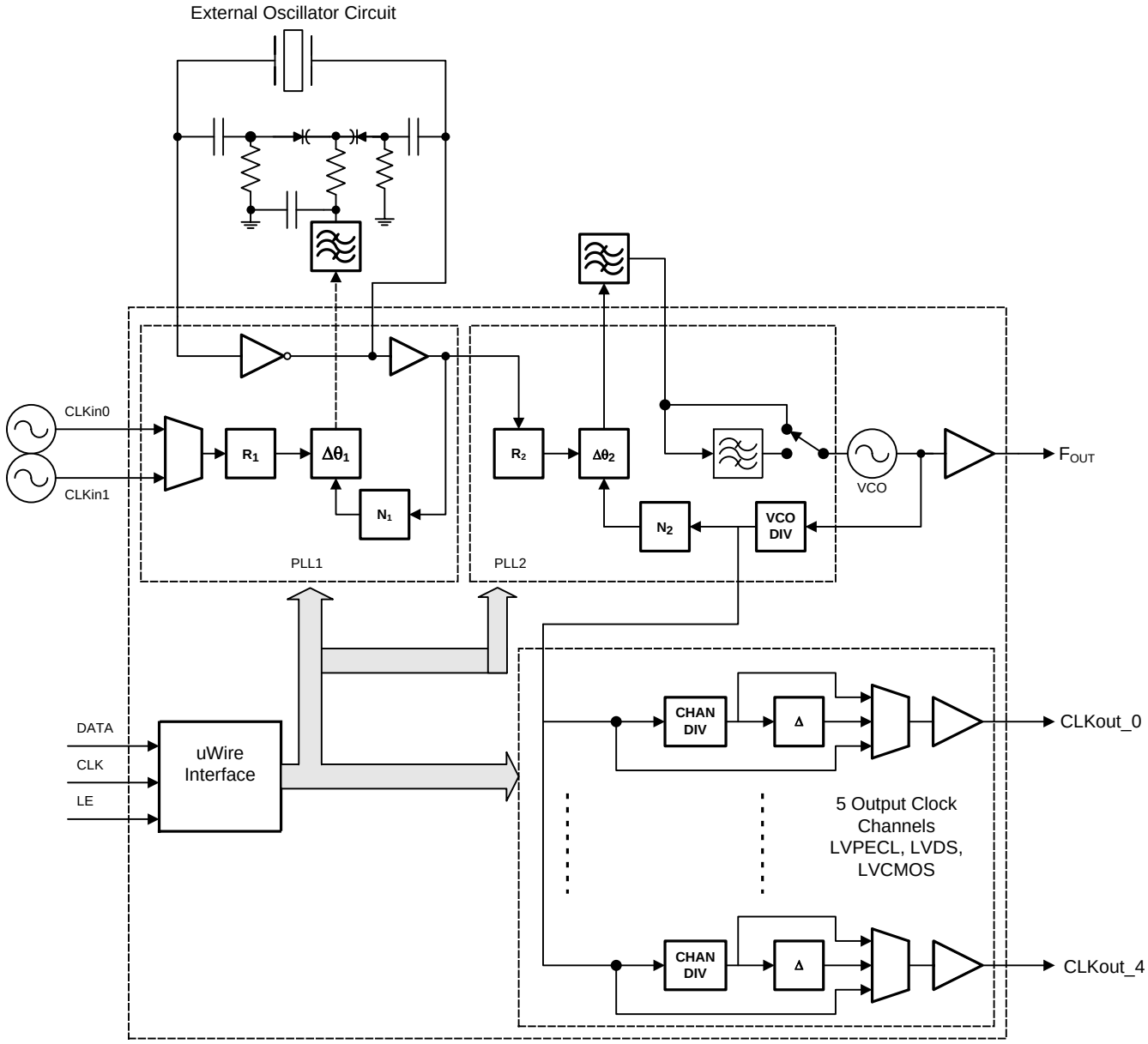

Figure 1. LMK04000 Family Dual PLL Architecture with Crystal Oscillator Circuit

2 Review of Oscillator Fundamentals

An oscillator is constructed from a tuned circuit and an amplifier arranged in a feedback loop, as shown in Figure 2.

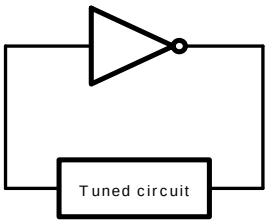

Figure 2. Functional Representation of an Oscillator Circuit

The criteria for oscillation are:

1. Closed loop gain >= 1 at the frequency of oscillation
2. The total phase shift around the loop is n*2π radians, n = 1,2,3...

The inverter-amplifier provides a nominal phase shift of π radians, leaving the remainder of the phase shift to the tuned circuit. The tuned circuit, which is effectively a bandpass filter, may be constructed from a simple L-C series resonant circuit or other frequency selective circuit, such as a crystal.

The oscillator configuration shown in Figure 3 is known as the parallel resonant mode. This is the oscillator mode supported by the LMK040xx family. A load capacitor, C_L, is placed in parallel with the crystal. The equivalent circuit of a crystal is shown on the right half of Figure 3. It can be shown that a good approximation for the oscillation frequency of the parallel resonant mode is given by [1]:

$$f_L = f_S \cdot \left(\frac{C_1}{2 \cdot (C_0 + C_L)} + 1 \right) \quad (1)$$

Where:

$$f_S = \frac{1}{2\pi\sqrt{L_1 C_1}} \quad (2)$$

is the series resonant frequency of the crystal.

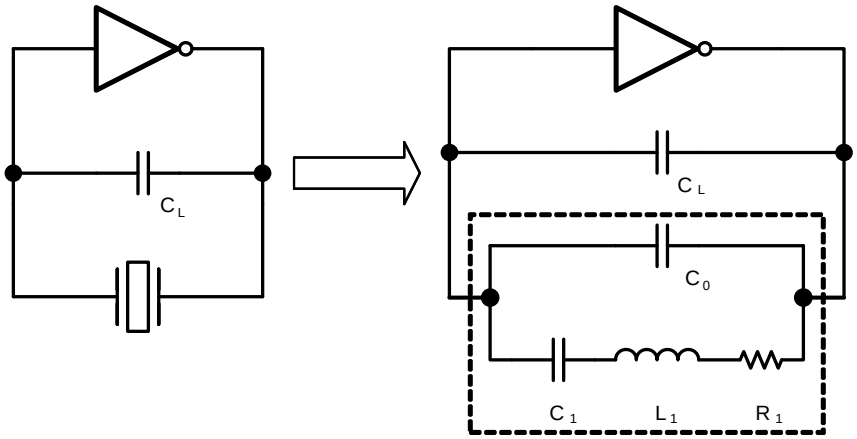

Figure 3. Parallel Resonant Crystal Oscillator Circuit

C_1, L_1 and R_1 represent the *motional capacitance*, *motional inductance* and *motional resistance* of the crystal. C_0 represents the *shunt capacitance* of the crystal, primarily due to the capacitance of the electrodes attached to the crystal plus any other stray capacitance associated with the crystal packaging. C_0 will be specified in a crystal data sheet, and usually has a specified maximum value of 5 to 7 picoFarads (pF). Because most data sheet specifications that are listed as maximums represent the tail of some underlying probability distribution, the typical value is often much less, for example, 3 pF. C_1 may be directly specified, or may be inferred from the ratio of C_0/C_1, which may instead be listed on the data sheet. Typical values of C_1 will fall in the low femtoFarad (fF) range, for example, 10 fF. Typically, the motional resistance and inductance are not listed on a crystal data sheet. Instead of motional resistance (R_1), another resistance specification, *equivalent series resistance* (ESR), will be listed. Some data sheets mistakenly list this as motional resistance, though it is not. A more complete explanation of ESR will be given in a subsequent paragraph.

Load capacitance (C_L) is another important parameter listed by the crystal manufacturer on the data sheet. For crystals intended to be used in parallel resonant mode designs, C_L is the value that causes the crystal to oscillate at the nominal resonant (center) frequency. The remainder of this note will focus on the parallel resonant crystal oscillator design.

In Figure 4, the oscillator loop circuit has been partitioned into two blocks, as shown in the left half of the diagram. One part is the active amplifier block and the second part is the frequency selective block, which includes not only the crystal but also the load capacitor, C_L. The right half of the diagram shows the impedance represented by each of the partitions can be resolved into real and reactive parts. It can be shown that the real part of the impedance represented by the frequency selective block is given by [1]:

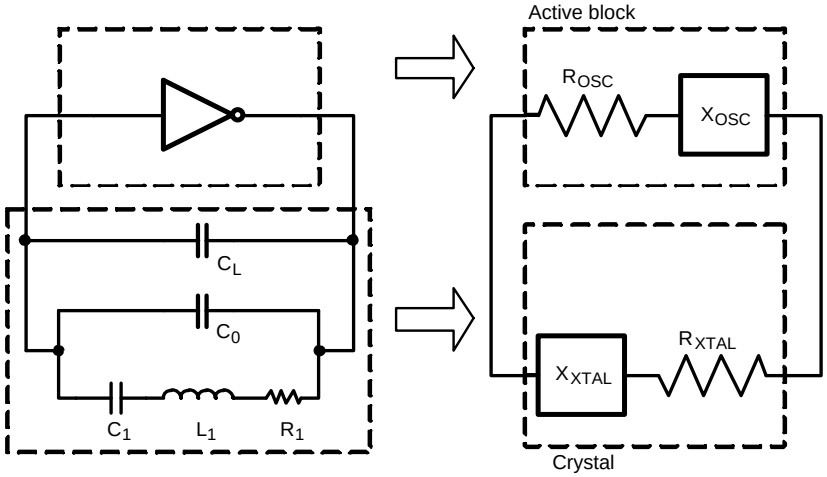

Figure 4. Negative Resistance Model and the Equivalent Oscillator Circuit

$$R_{XTAL} = R_{ESR} = R_1 \cdot \left(\frac{C_0 + C_L}{C_L}\right)^2 \quad (3)$$

ESR is the real part of the complex impedance represented by the crystal and the parallel load capacitor. It is proportional to the motional resistance scaled by a factor including the shunt capacitance and the load capacitance. ESR is a data sheet parameter. Typical values will depend on the crystal frequency, but usually fall in the range of 20 ohms to >100 ohms. The significance of ESR to the oscillator design engineer is that the gain required by the oscillator amplifier is directly proportional to the ESR of the crystal at the oscillation frequency. Consequently, a higher relative ESR requires a higher gain in order for the oscillator to achieve startup. The maximum ESR supported by the LMK04000 family is 100 ohms.

Note that the parallel resonant frequency is a function of C_L. If C_L is varied over some range, then the frequency of parallel resonance can be tuned over some range. Assuming some lower limit for C_L as C_{L1}, and upper limit as C_{L2}, the *normalized tuning range* of the parallel resonance mode is given by:

$$\frac{\Delta F}{F} = \frac{F_{CL1} - F_{CL2}}{F_{CL1}} = \frac{C_1}{2} \cdot \left(\frac{1}{(C_0 + C_{L1})} - \frac{1}{(C_0 + C_{L2})} \right) \bullet \text{ppm}$$
$$= \frac{C_1}{2} \cdot \left(\frac{C_{L2} - C_{L1}}{(C_0 + C_{L1})(C_0 + C_{L2})} \right) \quad (4)$$

In the oscillator circuit of Figure 3, we can replace C_L by a variable capacitor, called C_{TUNE}, in parallel with the crystal, as shown below in Figure 5. In practice, this variable capacitor is a varactor diode whose capacitance value is controlled by the tuning voltage produced by the phase detector/charge pump and loop filter of the PLL.

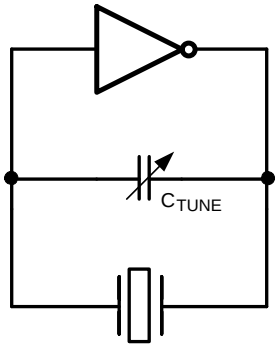

Figure 5. Oscillator Circuit with Tunable Capacitance (C_{TUNE}) for C_{LOAD}

The tuning range of the oscillator is strongly related to the adjustable range of C_{TUNE}. On a practical printed circuit board (PCB) layout using real-world devices, there will always be some stray capacitance that will contribute to the effective C_L. For example, this stray capacitance can be due to PCB characteristics (trace width and trace lengths) and to the input capacitance of the amplifier device in the loop. A more realistic model of the oscillator circuit is represented in Figure 6:

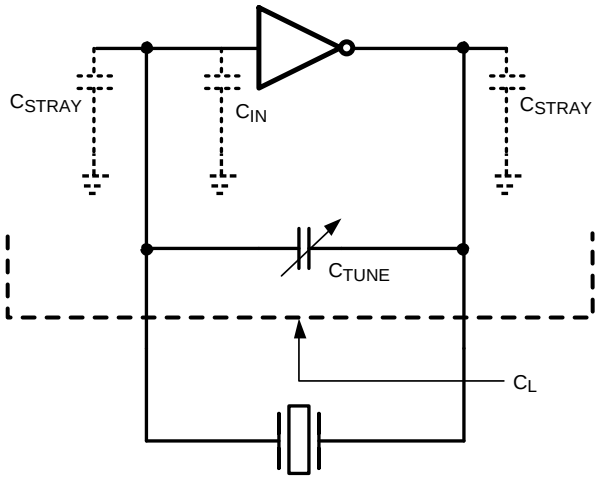

Figure 6. Oscillator Circuit Showing Contributions to C_{LOAD}

C_L is now given by:

$$C_L = C_{IN} + C_{TUNE} + \frac{C_{STRAY}}{2} \quad (5)$$

Assuming that C_{TUNE} can be forced to zero, this equation indicates that the minimum load capacitance is set by stray capacitance of the PCB and any other capacitive loading associated with the amplifier block in the oscillator circuit. Under ideal conditions, it is preferable to choose C_{TUNE} so its range is centered on the value of C_L given in the crystal data sheet. However, if C_{IN} and C_{STRAY} are large enough, they in effect reduce the tuning range of the circuit. For this reason, it is important to minimize the stray capacitance associated with the PCB.

3 Factors that Influence Crystal Selection and Oscillator Design

3.1 Tuning

The capability to tune, or pull, the crystal frequency is critical in frequency synthesis applications. The following paragraphs address why.

3.1.1 Crystal Errors

A crystal is a manufactured device, and like all manufactured products, the fundamental behavior of a crystal is dependent on the design, material and processes used to produce it, as well as the environment in which it operates. While the design of the crystal cut and packaging may take into account these factors, it is usually not cost effective (nor possible) to eliminate all variability, however large or small. Consequently, crystal data sheets will include specifications for tolerances in the crystal frequency due to basic construction, operating stability, and aging. On a datasheet, these might be called out as *frequency tolerance*, *frequency stability* and *aging* tolerance, respectively. *Frequency tolerance* refers to accuracy and repeatability of the nominal crystal frequency across multiple devices for a fixed set of conditions (temperature, load, etc.). This specification may often be chosen when ordering a crystal, subject to a finite set of tolerance ranges from which to select. Typical values may range from ±10 ppm to ±50 ppm. *Frequency stability* refers to the variation of the instantaneous operating frequency over temperature. Again, many manufacturers offer multiple grades of stability, so this may also be specified by the customer when ordering. Typical values may range from ±30ppm to ±100 ppm, and may also be customized by operating temperature range. Finally, an *aging* tolerance addresses the effects of change in the crystal lattice over time which lead to a change in the nominal crystal operating frequency. Typically, this specification is split between first year aging and then either a second aging parameter that addresses aging per year after the first year, or total aging variation for a longer block of time, such as 10 years. For example, an aging tolerance might be: ±5 ppm in year 1, and ±2 ppm/year thereafter. An example of the second form would be: ±5 ppm in year 1, and ±15 ppm per 10 years thereafter.

So, how do these tolerances (errors) relate to tuning requirements and the designer's selection of a crystal? First, crystals are often used in frequency synthesizer applications where they are frequency locked to a reference clock or oscillator, under the control of a phase locked loop (PLL). Assuming that the frequency accuracy of the reference clock is exact, and assuming that the capacitive loading presented to the crystal by the circuit is exactly as stated on the data sheet, the tolerances discussed above tell us that there is no guarantee that the crystal will actually operate at its specified nominal frequency. Assume that a particular crystal has the following specifications: *frequency tolerance* = ±20 ppm, *frequency stability* = ±50 ppm, and *aging* = 5 ppm/year. Hence, it is possible that the loaded operating frequency of the crystal could differ from nominal by ±75 ppm after one year and ±120 ppm after ten years. As such, the operation of the PLL would act to *pull* the crystal's frequency to the correct value. This is done, of course, when the PLL generates a control voltage which is applied to a varactor diode that acts as a voltage variable capacitor. The capacitance of the diode is changed, which changes the loading seen by the crystal, which in turn changes its frequency, according to Equation 4.

3.1.2 Reference Clock Errors

In the LMK04000 family, the crystal resonator is locked to an external, incoming reference clock. A second consideration acknowledges that in reality, the reference clock frequency is not always exact, so even if the frequency tolerances (errors) of the crystal are zero (that is, it is perfect) under the specified load, the crystal frequency must be adjusted to the actual frequency of the reference clock. For example, if the frequency tolerance of the reference clock is ±20 ppm, the tuning capability of the oscillator circuit must support this range.

3.1.3 Pulling Range and How it is Influenced by Circuit Parameters

Taking into consideration all error sources identified in the preceeding sections, the pulling range design target for the oscillator is usually chosen to be the sum of crystal errors plus reference clock error. Using the numbers from the previous discussion, the total minimum pulling range requirement of the oscillator circuit is: ±75 ppm ±20 ppm = ±95 ppm (for the moment, the aging tolerance is being excluded). Note that this is the design *requirement*, but not necessarily the achievable performance. Recalling Equation 4, you see that the achievable pulling (tuning) range is determined by:

1. The range of the load capacitance, $C_{L2} – C_{L1}$
2. The motional capacitance, C_1, and
3. The shunt capacitance, C_0

Shunt capacitance (C_0) is specified on the data sheet and a common value is 7 pF. The motional capacitance may either be directly read from the data sheet or calculated from the ratio C_0/C_1 if it is given on the data sheet. This leaves the load capacitance range as the remaining parameter that determines the pulling range of the oscillator. For convenience, assume that the specified load of a candidate crystal is 14 pF, and that the tuning range of the varactor diode to be used in the circuit is 2 pF to 19 pF, corresponding to a tuning voltage range of 3 VDC to 0 VDC. Using these values and Equation 4 and Equation 5, we can plot pulling range versus C_0/C_1 for various values of $C_{IN} + C_{STRAY}/2$, the fixed capacitance. This is illustrated in Figure 7.

Each trace plotted in the graph reflects the assumption that C_{LOAD} is given by Equation 5, and the minimum C_{LOAD}, C_{L1}, is the sum of the minimum value of the varactor diode (2 pF) plus the corresponding fixed capacitance value of ($C_{IN} + C_{STRAY}/2$). The maximum value (C_{L2}) is bounded by the maximum tuned value of the diode (19 pF) plus the fixed value ($C_{IN} + C_{STRAY}/2$).

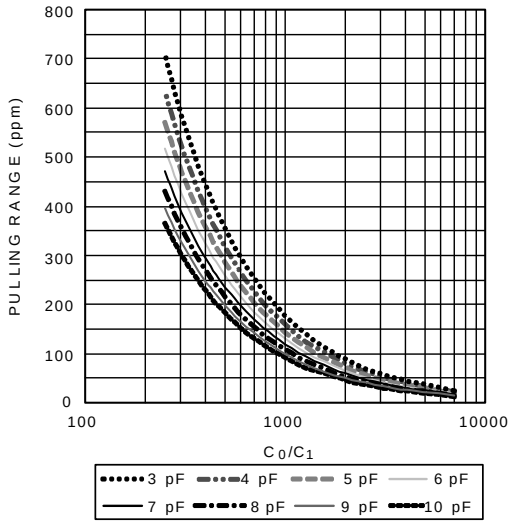

Figure 7. Pulling Range vs. C_0/C_1 for Selected Values of $C_{IN} + C_{STRAY}/2$

In examining Figure 7, you can observe two important points:

- First, for a fixed C_0/C_1, larger values of ($C_{IN}+C_{STRAY}/2$) decrease the pulling range of the circuit.
- Second, for a fixed value of ($C_{IN}+C_{STRAY}/2$), increasing C_0/C_1 decreases the pulling range.

Our example pulling range was ±95 ppm, or a total range of 190 ppm. Selecting a value with margin, for example, to accommodate crystal aging, we choose a pulling range of 240 ppm, or ±120 ppm. For a C_0/C_1 value of 700, we see that we can only achieve this range when (C_{IN} + C_{STRAY}/2) <= 3 pF. For a C_0/C_1 value of 350, a pulling range of 240 ppm is achievable for (C_{IN} + C_{STRAY}/2) <= 10 pF, a much more relaxed constraint on the PCB layout and capacitive load presented by the amplifier circuit. However the frequency stability of the crystal is improved with higher C_0/C_1 ratios, so the tradeoff for higher input capacitance and/or stray capacitance is lower crystal frequency stability.

While we may correctly conclude that specifying a lower C_0/C_1 ratio extends the pulling range of the oscillator, keep in mind that we are forced into this choice by a larger value attributed to (C_{IN} + C_{STRAY}/2). Also note this says nothing about the symmetry of the pulling range around the nominal center frequency. The plots shown in Figure 8 illustrate the pulling range for two cases:

- **Case 1**: (C_{IN} + C_{STRAY}/2) = 10 pF
- **Case 2**: (C_{IN} + C_{STRAY}/2) = 5 pF

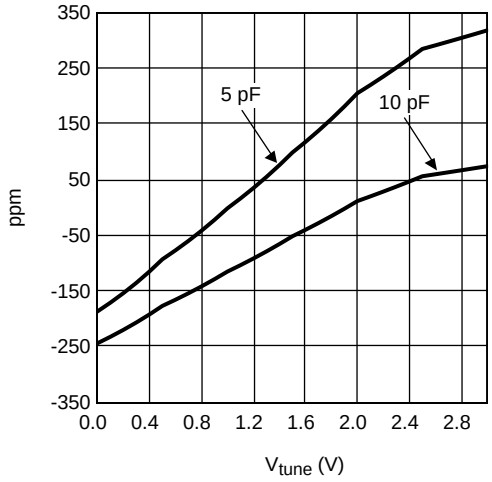

Figure 8. Pulling Range Symmetry

The curves in Figure 8 were generated from Equation 4 for a crystal having F_{NOM} = 12.288 MHz, C_0 = 7pF maximum, C_1 = 25 fF, and a nominal C_{LOAD} = 14 pF. The tuning curve for the varactor diode used in this example in shown in Figure 9. First, note that for Case 1 (10 pF), the pulling range extends from about +70 ppm to -250 ppm. Though the total pulling range is 320 ppm and meets the 240 ppm requirement, it is highly asymmetric and would not meet the requirements of ±120 ppm given above. For Case 2 (5 pF), we see that we have achieved slightly better symmetry and a wider pulling range, extending from approximately -200 ppm to over +300 ppm. For this case, the absolute pulling range is ~500 ppm and covers the design target of ±120 ppm. If the nominal frequency F_{NOM} corresponds to 0 ppm, for Case 2 it is achieved when V_{tune} = 1 V. We would prefer that F_{NOM} be achieved as close as possible to the midpoint of the V_{tune} range, or at about 1.5 VDC. Though we have noted that larger values of C_{IN} + C_{STRAY}/2 place constraints on the design and operation of the oscillator circuit, there are certain instances where adding some capacitance can be beneficial in improving the tuning symmetry of the circuit. This capacitance is represented in Figure 6 by the capacitors labeled as "C_{STRAY}". In Figure 6, the capacitors labeled as C_{STRAY} are intended to represent uncontrolled parasitics but could in fact be components deliberately included in the circuit.

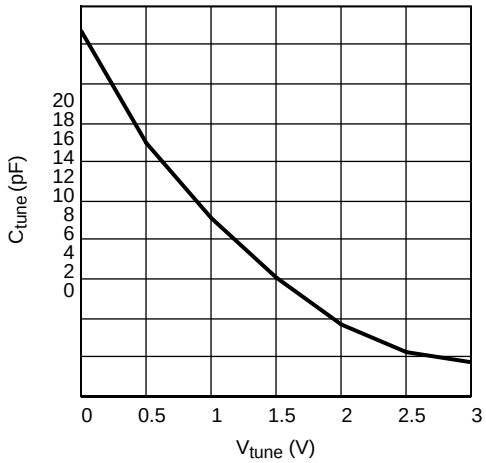

Figure 9. Example Diode Tuning Curve

Figure 10 illustrates the oscillator tuning curve when $C_{IN} + C_{STRAY}/2 = 6.8$ pF, in effect, Case 2 with 1.8 pF of added capacitance. Relative to Case 2, also re-plotted in the graph, it is much more symmetric, covering approximately ±210 ppm, and though still not centered, the 0 ppm point has shifted to 1.3 VDC, an improvement relative to Case 2. Note, however, that the total pulling range decreased from about 500 ppm to 420 ppm, though still adequate to meet a design target of 240 ppm.

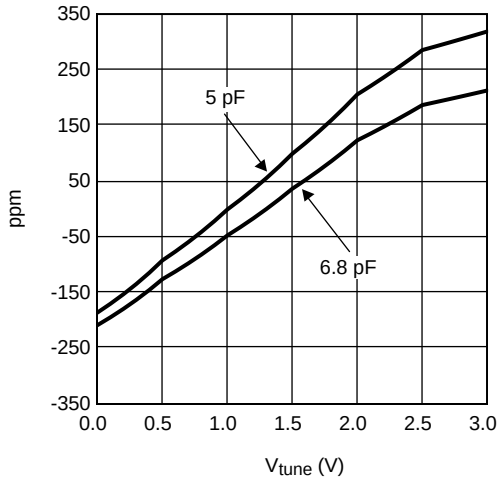

Figure 10. Tuning Curve for $C_{IN} + C_{STRAY}/2 = 6.8$ pF and 5 pF

In summary, many factors lead to deviations from the nominal frequency. To fully compensate for this, the tuning range of the crystal oscillator should be as large as possible. To maximize the tuning range, the influence of C_{TUNE} should be as large as possible. This is done by:

- Minimizing the PCB parasitic capacitance, C_{STRAY}
- Selecting a tuning diode with a wide tuning range (Cmax/Cmin)
- Specifying the load capacitance of the crystal to maximize the tuning range. Ideally, the tuning range should be centered on the nominal crystal frequency. This can be achieved by specifying the crystal load capacitance using:

$$C_L \text{ (specified)} = C_{IN} + C_{TUNE} \left(\frac{V_{CC}}{@\ 2} \right) + \frac{C_{STRAY}}{2} \quad (6)$$

The calculated value should be rounded up to the nearest integer number. This approach will result in the widest tuning range. However, the range may not be centered perfectly around the nominal crystal frequency. Centering of the tuning range may be accomplished by adding small capacitors to C_{STRAY} at the expense of a slightly narrower tuning range.

Example:

C_{IN} = 6 pF (measured or estimated)

C_{STRAY} = 5 pF (measured, estimated or added)

C_{TUNE}(@1.5 V) = 4.56 pF (from diode data sheet)

Specified load capacitance:

C_L(spec) = 6 + 4.56 + 5/2 = 13.06 pF

If a crystal with C_L(spec) = 14 pF is used, the tuning range can be centered by adding 2.0 pF to C_{STRAY}, resulting in a load capacitance of 14 pF at V_{TUNE} = 1.5 V. Based on this example, an oscillator was constructed using a Vectron VBX1 crystal, and the measured tuning range was +138/-114 ppm (3.3 V, 25 °C).

When designing the tuning circuit, it should be noted that the tuning range will vary as function of the power supply voltage. However, as the tuning diode is ground referenced, only the upper end of the tuning range will vary. Thus, if good centering is important, the tuning circuit should be designed to provide good centering at the lowest possible power supply voltage.

3.2 Crystal Power Dissipation

The last critical data sheet parameter to be discussed is maximum drive level, or power dissipation capability of the crystal. Power dissipation in a crystal is: $P_{XTAL} = I^2_{RMS} \times R_{ESR}$.

I_{RMS} is the current through the crystal, and R_{ESR} is the ESR of the crystal. As piezoelectric devices, crystals have limited power dissipation capability. Overdriving a crystal will either damage the crystal or cause premature aging. The drive level requirement for any crystal used with an LMK04000 family device will depend on several factors:

- Capactive load and R_{ESR}
- V_{CC}
- Loaded resonant frequency
- Expected operating temperature

Equation 7 can be used to calculate the required crystal drive level (in microwatts) for a crystal used with the LMK04000 family. It takes into account the crystal's ESR, expected operating temperature, and loaded frequency:

$$P_{XTAL} = ((-0.00869 \cdot R_{ESR} + 1.876) \cdot (0.1322 - (\Delta T \cdot 0.0003)) \cdot f_L)^2 \cdot R_{ESR}, (\mu W) \quad (7)$$

Where: $\Delta T = T_{OP} - 25\ °C$, T_{OP} = expected operating temperature in degrees C.

f_L = nominal, loaded operating frequency of the crystal, in MHz

R_{ESR} = Crystal ESR (measured or from data sheet), in Ohms

This equation does not include adjustment factors for capacitive load or V_{CC}. This is because the coefficients used in the equation take into account a worst case scenario of 3.45 V and CL = 28 pF. Consequently, the calculated drive level will provide sufficient operating margin under the following constraints: V_{CC} <= 3.45 VDC and C_L <= 28 pF.

As an example, assume a crystal with a nominal frequency of 12.288 MHz has a specified ESR of 40 Ohms and will operate at 50 °C. Inserting these values into Equation 7 yields a required drive level of 219.4 µW. Some common crystal drive levels are 50 µW, 100 µW, 500 µW and 1 mW, so a 500 µW crystal would easily meet the drive level requirement.

Figure 11, Figure 12, and Figure 13 illustrate maximum required power dissipation vs. operating temperature and R_{ESR} for three different crystal frequencies: 12.288 MHz, 15.36 MHz and 19.44 MHz. The traces in each figure represent 20 °C intervals, starting at -45 °C and ending at +75 °C. These figures graphically illustrate that power dissipation is directly proportional to the crystal frequency and inversely proportional to operating temperature, which can also be inferred from Equation 7. Consequently, if the crystal will be operating over a range of temperatures, *the required drive level should be calculated using the lowest expected operating temperature*.

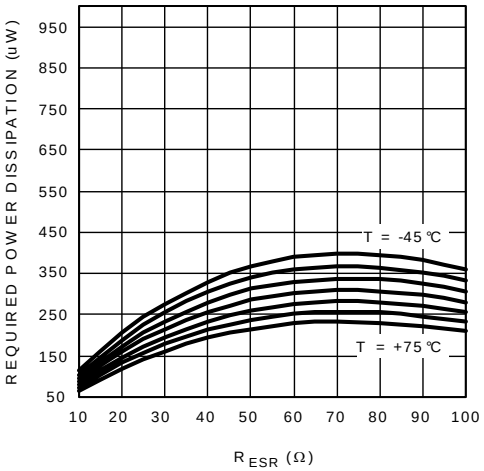

Figure 11. Maximum Required Power Dissipation by Operating Temperature and R_{ESR}, 12.288 MHz Crystal

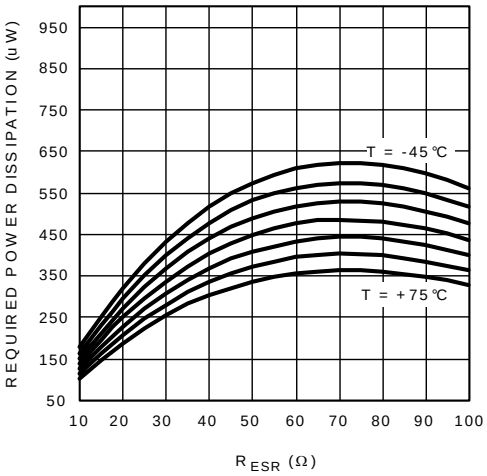

Figure 12. Maximum Required Power Dissipation by Operating Temperature and R_{ESR}, 15.36 MHz Crystal

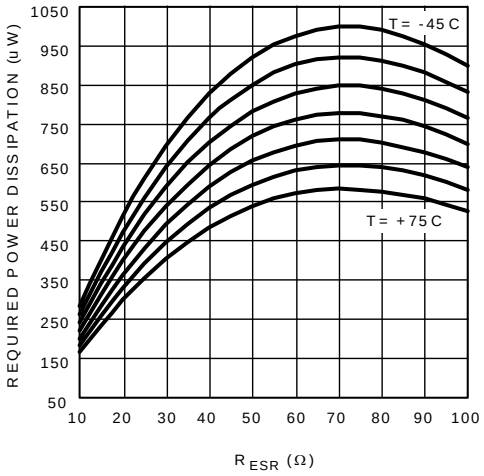

Figure 13. Maximum Required Power Dissipation by Operating Temperature and R_{ESR}, 19.44 MHz Crystal

4 Crystal Oscillator Reference Design and Performance Examples

Figure 14 illustrates a reference design for a crystal oscillator using the LMK04000 family. This oscillator circuit is implemented on the LMK04000 family evaluation board. It has been tested with the crystals itemized in Table 1. The tuning diode is a Skyworks model SMV1249-074LF. It is a dual diode package in a common cathode arrangement. This diode configuration has the advantage of blocking reverse leakage current. The loop filter components are chosen to achieve a narrow loop bandwidth, in the range of 10 Hz to 20 Hz. The actual component values will depend on the parameters chosen for PLL1 (R divider and N divider values) and the slope of the crystal tuning curve. An initial estimate of the slope of the tuning curve can be developed using Equation 4 and the appropriate parameters from the crystal data sheet. Also note that Equation 5 should be substituted for C_L in Equation 4. A nominal value of 6 pF can be used for C_{IN}. A reasonable range of values that can be used for C_{STRAY} is 2 pF to 4 pF. After the actual oscillator circuit has been implemented on a printed circuit board, the tuning curve should be measured to verify that the original estimate of the tuning slope was correct. Any significant difference may require recalculation of the loop filter components to maintain the desired loop bandwidth.

Each crystal listed in Table 1 was integrated with an LMK04031 and the phase noise and jitter performance at the clock outputs of the LMK04031 was measured using an Agilent E5052A Signal Source Analyzer.

Table 1, Table 2, and Table 3 provide measured phase noise data at selected offsets and RMS jitter for:

1. Each crystal, and
2. Each clock output type for the LMK04031

All measurements were taken at 25 °C.

Table 1. Example Crystals and Specifications

PARAMETER	Vectron VXB1-1127-12M288	Fortiming HC49SM-15M360-1B25B14
F_{NOM} (MHz)	12.288	15.36
Mode	Fundamental	Fundamental
Calibration Tolerance	±20 ppm (25 °C)	±30 ppm (25 °C)
Stability	±30 ppm (-40 °C to +85 °C)	±25 ppm (-40 °C to +85 °C)
Load Capacitance (pF)	14	14
C_0/C_1	280 ±20%	NA
ESR	40	50
Drive Level	500 µW	1000 µW
Aging	±5 ppm/year max., ±20 ppm maximum over 20 years	±5 ppm/year maximum
Packaging	Surface mount	Surface mount

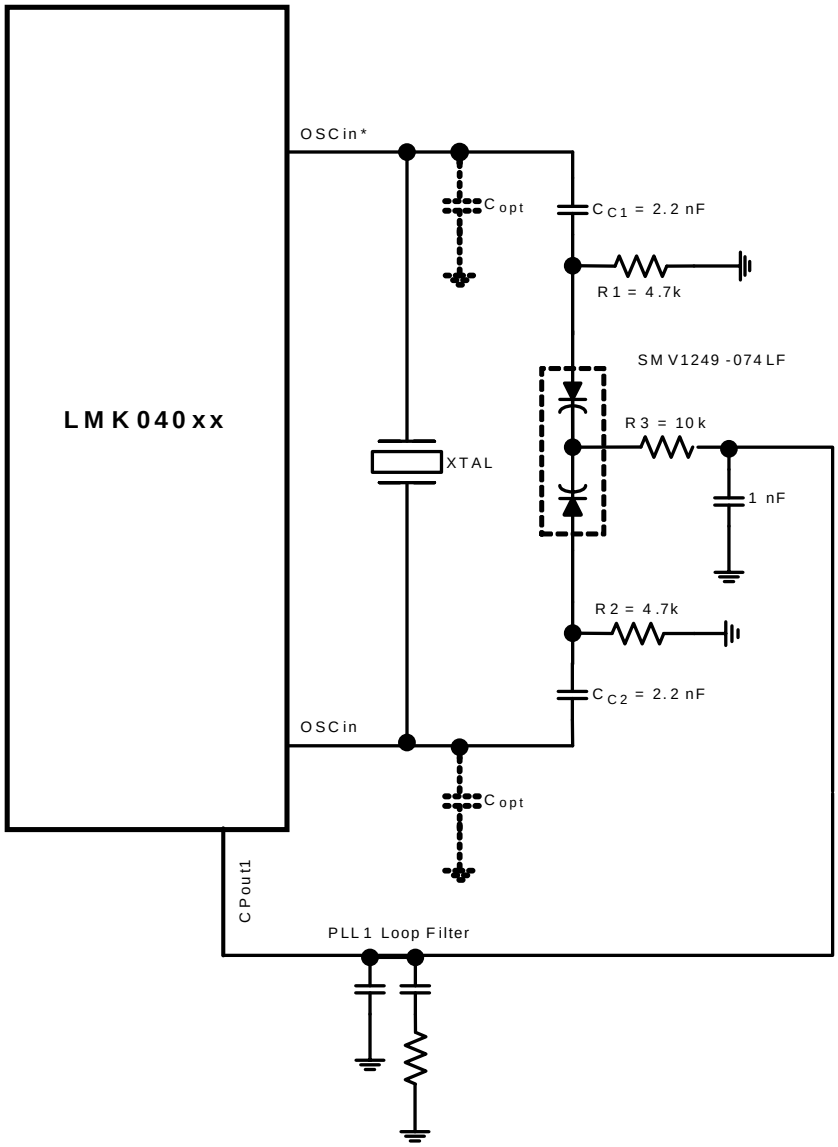

Figure 14. Crystal Oscillator Reference Design Circuit

Table 2. Vectron VXB1, 12.288 MHz, Selected Phase Noise Data and RMS Jitter, 25 °C

F_{CLK} = 122.88 MHz, PLL2 CP Gain = 1600 µA, PLL2 Loop BW = 57 kHz							
CLOCK OUTPUT TYPE	RMS JITTER (fs)	PHASE NOISE (dBc)					
		100 Hz	1 kHz	10 kHz	100 kHz	1 MHz	10 MHz
Crystal Output (closed loop)	244 (100 Hz - 200 kHz)	-111	-143	-151	-152	-152	NA
LVDS	245.8 (100 Hz - 20 MHz)	-102	-126	-128	-134	-152	-158
LVPECL	258 (100 Hz - 20 MHz)	-102	-127	-128	-133	-152	-158
LVCMOS	249 (100 Hz - 20 MHz)	-100	-127	-129	-134	-153	-160

Table 3. Fortiming, HC49SM, 15.36 MHz, Selected Phase Noise Data and RMS Jitter, 25 °C

F_{CLK} = 122.88 MHz, PLL2 CP Gain = 1600 µA, PLL2 Loop BW = 57 kHz							
CLOCK OUTPUT TYPE	RMS JITTER (fs)	PHASE NOISE (dBc)					
		100 Hz	1 kHz	10 kHz	100 kHz	1 MHz	10 MHz
Crystal Output (closed loop)	124.9 (100 Hz - 200 kHz)	-121	-150.1	-157	-157.6	-157.9	NA
LVDS	240.1 (100 Hz - 20 MHz)	-102	-125	-127	-135	-156	-158
LVPECL	250 (100 Hz - 20 MHz)	-100	-127	-127	-134	-156	-158
LVCMOS	228.5 (100 Hz - 20 MHz)	-101	-127	-128	-135	-157	-160

5 Summary Guidelines and Design Procedure

5.1 Summary of Important Points and Guidelines

- The nominal frequency of the crystal occurs at a specified C_{LOAD}.
- For a given tuning range, a higher value of $C_{IN} + C_{STRAY}/2$ requires a smaller C_0/C_1 specification for the crystal, at the cost of lower frequency stability inherent in the crystal, and restricted tuning range. C_{IN} is fixed by the oscillator amplifier characteristics. Minimizing C_{STRAY} (due to PCB parasitics) increases the range of C_0/C_1 that can be specified and allows the designer to adjust C_{STRAY} to better center the tuning curve.
- Crystal power dissipation is directly proportional to R_{ESR}. Higher R_{ESR} also requires higher loop amplifier gain to ensure faster startup.
- Refer to the data sheet for the LMK04000 family for the acceptable range of crystal frequencies and R_{ESR}.

5.2 Crystal Oscillator Design

This section summarizes the steps for designing a crystal oscillator. However, this is a little misleading because as with most design procedures, some iteration is required due to the degrees of freedom in choosing device parameters, or stated another way, there are more unknowns than equations. Hence, it is not possible construct a fixed procedure.

1. The minimum tuning range of the oscillator is set by the frequency stability of the reference clock summed with the crystal stability parameters (calibration, temperature and aging). A good starting point for total tuning range is 200 ppm (±100 ppm), assuming that the reference clock stability is much better than this (for example, ±20 ppm or less). In the final crystal selection, remember to account for aging over the expected operating life of the system.
2. Measure, estimate, or specify maximum C_{STRAY} and C_{IN}. When using the LMK04000 family of devices, use a max value of 6 pF for C_{IN}.
3. If a candidate for the tuning diode has been identified, calculate the required load capacitance of the crystal using Equation 6 and the values of C_{STRAY} and C_{IN} established in the previous step. Otherwise, if a candidate crystal has been selected, use Equation 6 with C_{LOAD}, C_{STRAY} and C_{IN} to calculate the required nominal tuning capacitance of the diode at Vcc/2.
4. Calculate the range of C_{LOAD} (C_{L1}, C_{L2}) that can be achieved given the diode tuning characteristics and Equation 5.
5. Using the min and max C_{LOAD} from the previous step and some initial starting value for tuning range (as suggested in Step 1), use Equation 4 to calculate some possible values for C_0 and C_1. A reasonable range of values for C_0 is single digit picofarads, while C_1 will have values that may range from less than 10 femtofarads to greater than 20 femtofarads. Compare these values to nominal values listed on data sheets for some candidate crystals. Also remember to calculate the ratio of C_0/C_1. In practice, this ratio should be between 200 and 300 for pullable crystals.
6. Refer to the LMK04000 family data sheet for maximum allowable R_{ESR}. However, when selecting a crystal, always try to choose the lowest value possible, as this will reduce the drive level required by the crystal. Calculate the expected drive level using Equation 7. This is the minimum that should be specified for the crystal

At this point, a complete set of starting parameters for the crystal and oscillator design has been generated. These starting values should be analyzed with regard to choice of tuning diode, typical manufacturer crystal specifications, and what can be achieved in the PCB layout of the oscillator circuit. Some iteration may be required to find acceptable components.

5.3 PCB Layout Guidelines

The circuit in Figure 14 can be used as a starting point. The capacitors C_{C1} and C_{C2} are included for DC-blocking, and should be a couple of orders of magnitude greater than the required nominal load capacitance. The capacitors labeled as C_{OPT} are included so that some stray capacitance can be added to help center the tuning curve, if needed. Maintain close spacing of the components for the crystal oscillator, and, locate the components as close as possible to the OSCin/OSCin* pins (pins 28 and 29) of the LMK040xx device. This will minimize stray capacitance. Using 10 mil to 15 mil trace widths will also help minimize stray capacitance.

5.4 Measuring the Tuning Curve

It is important to measure the actual tuning curve of the oscillator once it has been constructed, either on a prototype board or final PCB. If using a prototype of the circuit, it should be as close as possible to the final version, as differences in the actual PCB construction will change the circuit characteristics.

Method 1: This procedure assumes that the crystal oscillator circuit is integrated with a PLL such as the LMK04000 family. The diode tuning voltage must be monitored as well as the crystal output frequency that is associated with the specific tuning voltage. The crystal frequency can be calculated by measuring the frequency at one of the clock outputs of the LMK04000 device, or at the F_{OUT} pin. If using a clock output to measure the frequency, then the following formula gives the crystal frequency:

$$F_{CRYSTAL} = \frac{F_{CLK} \cdot R_2 \cdot CLKout\_DIV}{N_2} \tag{8}$$

Where:

F_{CLK} = CLKout frequency

R_2 = PLL2 R-counter value

N_2 = PLL2 N-counter value

VCO_DIV = VCO output divider value (see Figure 1)

If measured at F_{OUT}, the following formula can be used:

$$F_{CRYSTAL} = \frac{F_{OUT} \bullet R_2}{N_2 \bullet VCO\_DIV} \tag{9}$$

The basic measurement procedure consists of sweeping the frequency of the reference source and measuring and recording the tuning voltage produced by PLL1 at each step in the sweep. The range of the frequency sweep of the reference source should be less than or equal to the expected tuning range of the crystal circuit, in ppm. For example, if the nominal frequency of the reference clock is 122.88 MHz and the expected tuning range of the crystal oscillator is ±100 ppm, the reference source would be swept from approximately 122.892 MHz to 122.868 MHz. The step size between these two endpoints is selectable. For example, a frequency step size that corresponds to 5 ppm to 20 ppm is a reasonable step size. Figure 15 illustrates a suggested measurement setup:

1. Use a tunable signal generator as the reference clock to PLL1 (CLKin0 or CLKin1 of the LMK04000 family). This signal source should be highly stable and accurate.
2. To measure the output frequency of the LMK040xx device, use an accurate (±1 Hz) frequency measurement device such as a frequency counter or spectrum analyzer. This device and the signal generator should be tied to a common reference source.
3. Measure the tuning voltage applied to the oscillator circuit using a high impedance voltmeter or similar device.
4. Though not shown in the figure, the lock state of PLL1 should be monitored using the LD pin (pin 12).

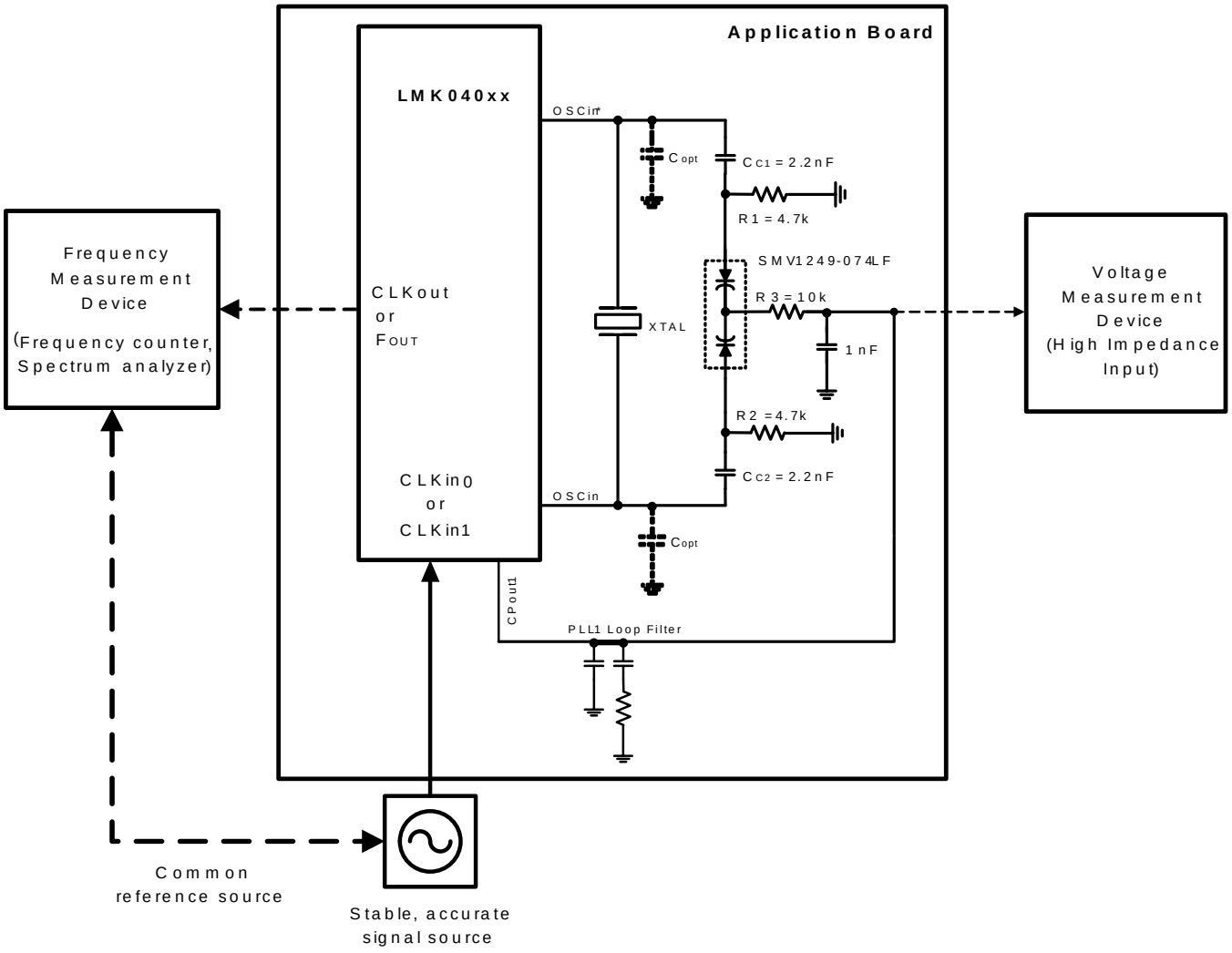

Figure 15. Tuning Curve Measurement Setup

Table 4 contains example data for a tuning curve measurement. In this case, the lock-state of the PLL was monitored, as shown in the last column of Table 4. Only values for which the PLL was locked are used to construct the tuning curve. The resultant tuning curve is plotted in Figure 16.

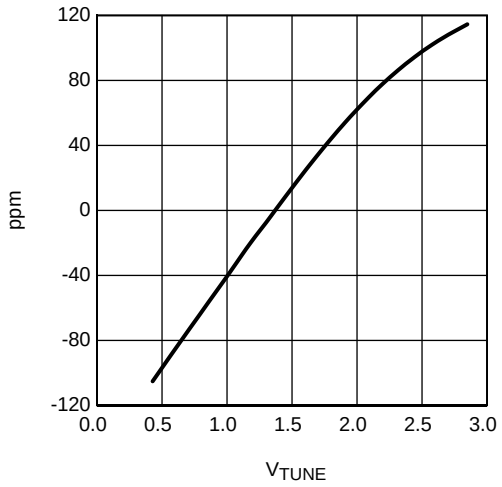

Figure 16. Tuning Curve for Data in Table 4

Table 4. Example Measurement Data for Crystal Oscillator Tuning Curve

Ref Clock Frequency (MHz)	Expected F_{XTAL} (Hz)	Measured F_{XTAL} (Hz)	Measured ΔF (Hz)	Measured ppm	Measured V_{TUNE} (VDC)	PLL1 Lock State
122.9	12290000	12289497	1497	121.8	3.07	unlocked
122.899	12289900	12289497	1497	121.8	3.07	unlocked
122.898	12289800	12289497	1497	121.8	3.07	unlocked
122.897	12289700	12289497	1497	121.8	3.07	unlocked
122.896	12289600	12289497	1497	121.8	3.07	unlocked
122.895	12289500	12289497	1497	121.8	3.07	unlocked
122.894	12289400	12289400	1400	113.9	2.846	LOCKED
122.893	12289300	12289300	1300	105.8	2.659	LOCKED
122.892	12289200	12289200	1200	97.6	2.504	LOCKED
122.891	12289100	12289100	1100	89.5	2.37	LOCKED
122.89	12289000	12289000	1000	81.4	2.25	LOCKED
122.889	12288900	12288900	900	73.2	2.14	LOCKED
122.888	12288800	12288800	800	65.1	2.04	LOCKED
122.887	12288700	12288700	700	57	1.944	LOCKED
122.886	12288600	12288600	600	48.8	1.854	LOCKED
122.885	12288500	12288500	500	40.7	1.768	LOCKED
122.884	12288400	12288400	400	32.5	1.685	LOCKED
122.883	12288300	12288300	300	24.4	1.604	LOCKED
122.882	12288200	12288200	200	16.3	1.526	LOCKED
122.881	12288100	12288100	100	8.1	1.449	LOCKED
122.88	12288000	12288000	0	0	1.373	LOCKED
122.879	12287900	12287900	-100	-8.1	1.298	LOCKED
122.878	12287800	12287800	-200	-16.3	1.218	LOCKED
122.877	12287700	12287700	-300	-24.4	1.143	LOCKED
122.876	12287600	12287600	-400	-32.5	1.073	LOCKED
122.875	12287500	12287500	-500	-40.7	1.002	LOCKED
122.874	12287400	12287400	-600	-48.8	0.929	LOCKED
122.873	12287300	12287300	-700	-57	0.856	LOCKED

Table 4. Example Measurement Data for Crystal Oscillator Tuning Curve (continued)

Ref Clock Frequency (MHz)	Expected F_{XTAL} (Hz)	Measured F_{XTAL} (Hz)	Measured ΔF (Hz)	Measured ppm	Measured V_{TUNE} (VDC)	PLL1 Lock State
122.872	12287200	12287200	-800	-65.1	0.784	LOCKED
122.871	12287100	12287100	-900	-73.2	0.711	LOCKED
122.87	12287000	12287000	-1000	-81.4	0.639	LOCKED
122.869	12286900	12286900	-1100	-89.5	0.567	LOCKED
122.868	12286800	12286800	-1200	-97.6	0.496	LOCKED
122.867	12286700	12286700	-1300	-105.8	0.425	LOCKED
122.866	12286600	12286600	-1400	-113.9	0.351	unlocked
122.865	12286500	12286500	-1500	-122.1	0.258	unlocked
122.864	12286400	12286400	-1600	-130.2	0.141	unlocked
122.863	12286300	12286350	-1650	-134.3	0.08	unlocked

Method 2: A second method for measuring the tuning curve of the oscillator circuit eliminates the tunable signal source and employs a DC voltage source applied directly to the tuning input of the oscillator. The output of the PLL1 loop filter is temporarily disconnected from the oscillator circuit. This measurement setup is shown in Figure 17.

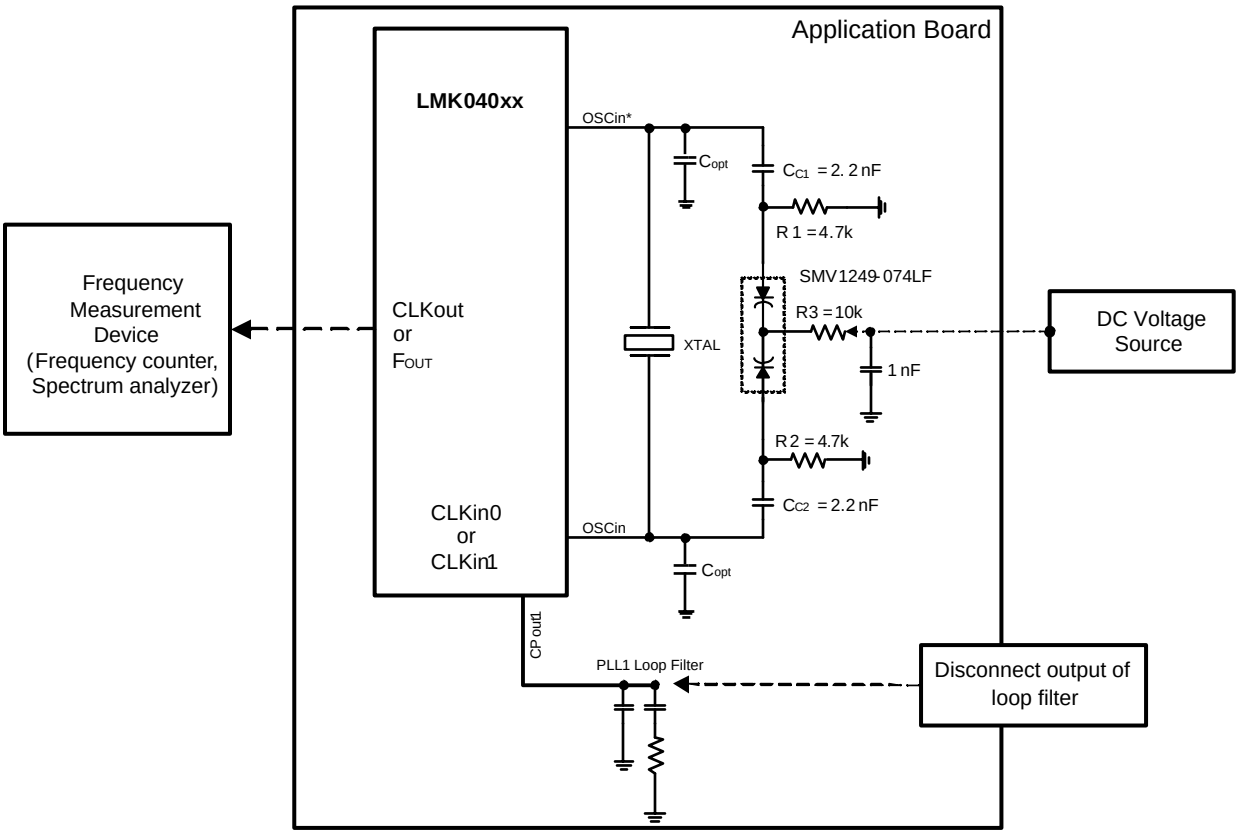

Figure 17. Measurement Setup for Tuning Curve Measurement Using Method 2

The DC voltage source is swept over some voltage range (for example, 0.1 V to 3.0 V) and the resultant crystal frequency is measured at each voltage increment, either directly or as shown in the figure by measuring the frequency at the output of the LMK040xx device and applying either Equation 8 or Equation 9 to calculate the crystal frequency. While this method is a reasonable approach, Method 1 is slightly superior in that it reveals the tuning dynamics of the PLL and the actual operating range that can be expected from the circuit.

5.5 Programming the LMK040xx

When a discrete crystal oscillator circuit is implemented with the LMK040xx, the internal loop amplifier must be enabled by setting the EN_PLL2_XTAL bit to 1 (Register 13, bit 21 = 1). In CodeLoader, this bit field is found on the Bits/Pins tab in the PLL block on the left side of the page, as shown in Figure 18.

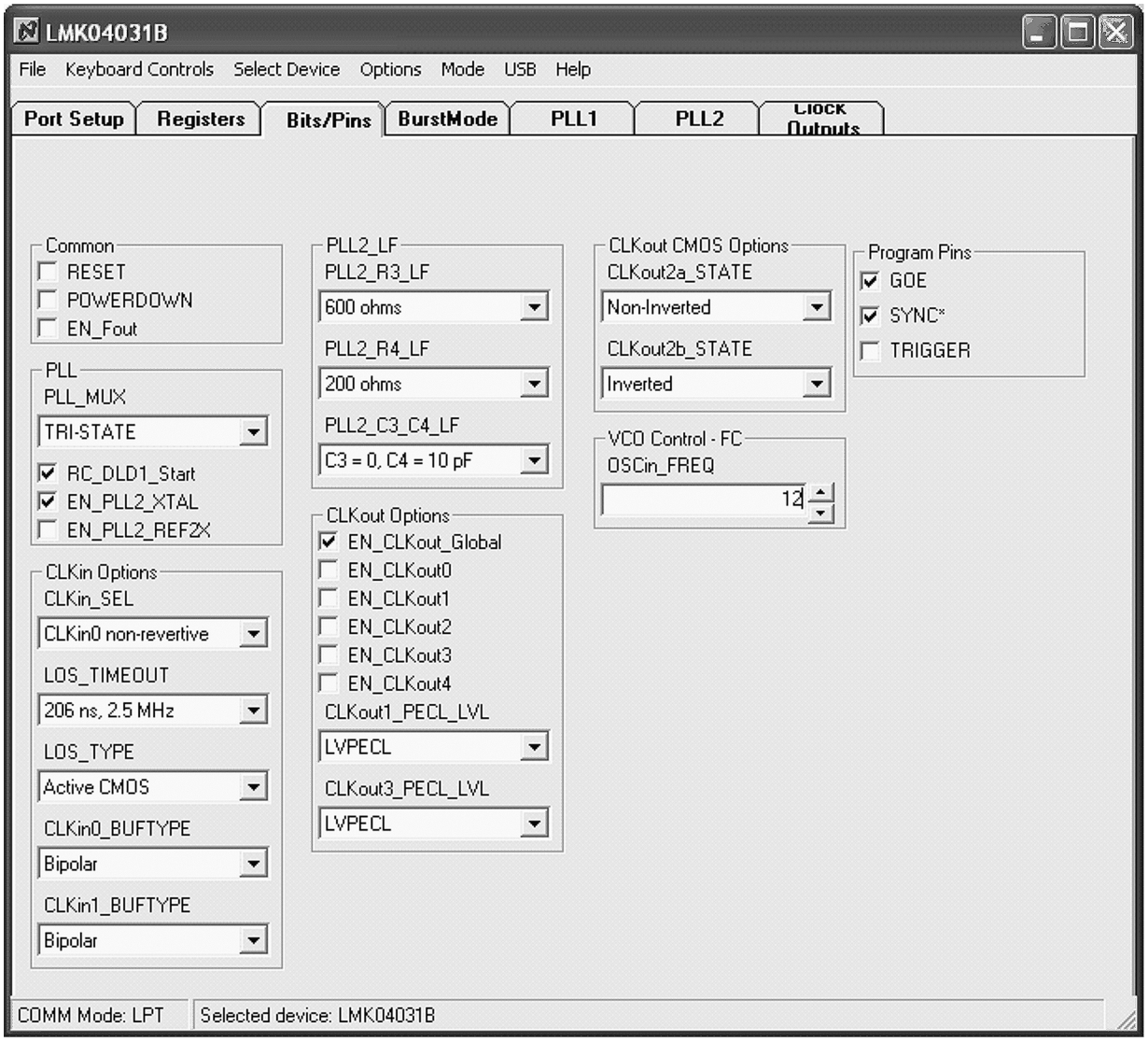

Figure 18. CodeLoader Bits/Pins Tab Showing EN_PLL2_XTAL Bit Field

The crystal frequency must be entered in the OSCin_FREQ field. The remainder of the LMK040xx configuration is as required for the application.

An option that can be used with a crystal oscillator implementation is the PLL2 reference frequency doubler. This option is also available when using a VCXO. The bit field that enables this option, EN_PLL2_REF2X, is also shown in Figure 18, below the EN_PLL2_XTAL field (Register 13, bit 16). When this bit is enabled (checked), the PLL2 R-counter is bypassed and the external oscillator input is routed through a frequency doubler circuit. This allows the PLL2 phase detector frequency to be increased, lowering the in-band PLL2 noise. If this option is enabled, the value entered in the PLL2 Reference Oscillator Frequency field on the PLL2 tab should be equal to 2x the crystal frequency (or 2x the VCXO frequency). Figure 19 shows an example for a 12.288 MHz crystal.

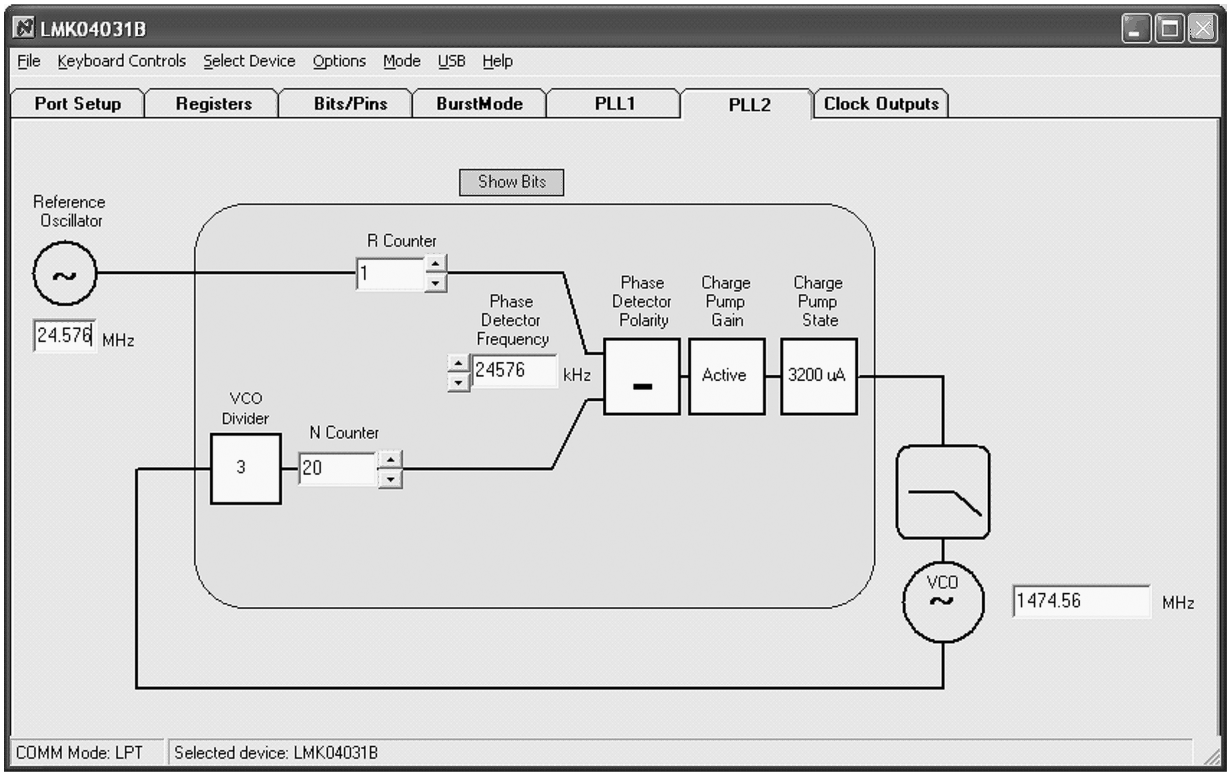

Figure 19. CodeLoader PLL Tab

6 Summary and Conclusions

This application report for the LMK040xx family has covered the design of an external crystal oscillator using the built-in loop amplifier featured in the LMK040xx family of clock conditioners. In many applications, this provides a low cost approach for the design of an oscillator with acceptable performance.

7 References

1. Cerda, Ramone M., “Specifying a quartz Crystal for a VCXO,” *RF Design Magazine*, August 2004.
2. Nguyen, N.M., Meyer, R. G., “Start-up and Frequency Stability in High-Frequency Oscillators,” *IEEE Journal of Solid-State Circuits*, Vol. 27, No. 5, May 1992.
3. *Design of Crystal and Other Harmonic Oscillators*, Benjamin Parzen, John Wiley and Sons, New York, 1983.

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