Application Report
SNAA310–May 2017

SDPLL for LMK046xx Family

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ABSTRACT

PLLs used in the LMK046xx family of devices are based on Semi-digital PLL architecture. LMK04610 and LMK04616 devices have two fully integrated PLLs. The first PLL, called PLL1 here, uses an external VCXO as its voltage-controlled oscillator. It is a very low-bandwidth PLL and the loop bandwidth is <300 Hz. Such a low bandwidth helps the jitter cleaning for a dirty input clock.

The second PLL in the LMK046xx devices, called the PLL2, is a relatively high-bandwidth PLL. PLL2 has an integrated high performance LC oscillator as a VCO. The frequency range of the VCO is 5800 MHz to 6200 MHz. The PLL2 is used to multiply the input clock up and provide very low-noise floor clock outputs. Both PLLs in the LMK046xx family of devices are based on a semi-digital PLL architecture.

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1 Traditional Analog PLL

The traditional analog PLL is shown in Figure 1. Input clock CLKIN and feedback clock FBCLK are applied to the Phase frequency detector. Based on the phase difference, the PFD generates UP/DOWN pulses.

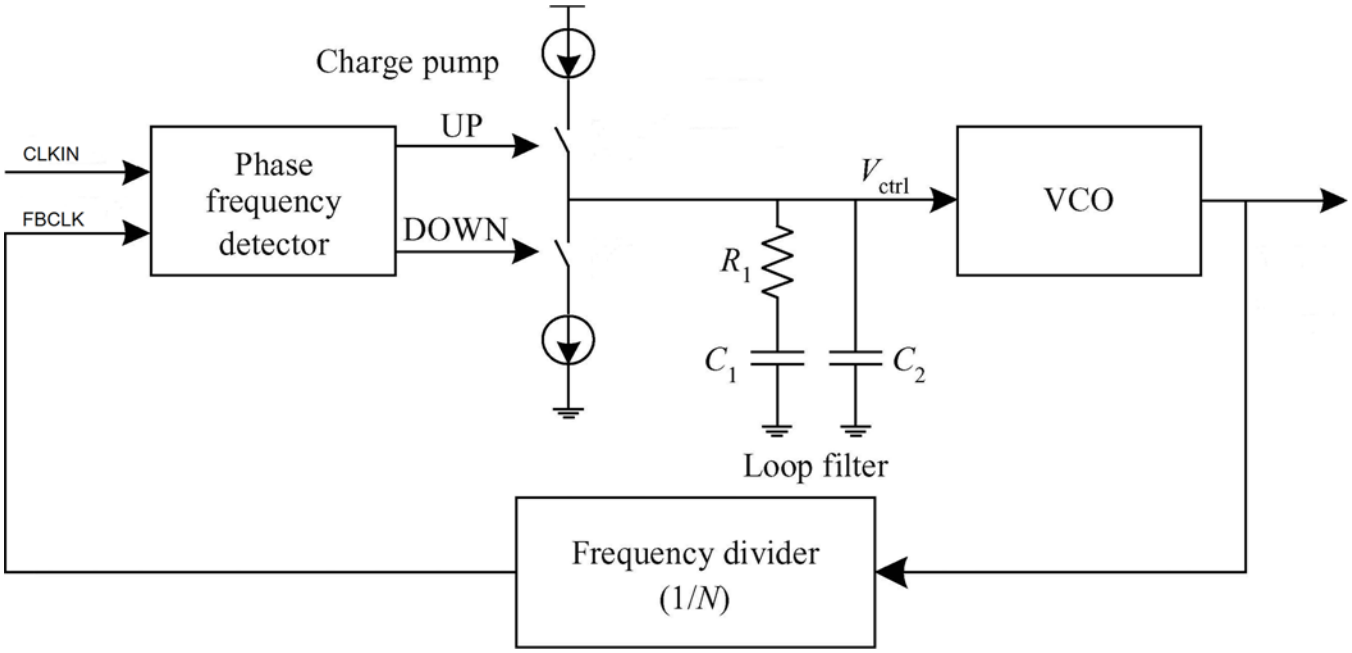

Figure 1. Traditional Analog PLL

The UP/DOWN triggers the current from the charge-pump and is applied to the Loop filter. The Loop filter converts the current into the voltage which controls the frequency of the VCO. To generate higher frequencies, a feedback frequency divider is used. In the steady state, the CLKIN and FBCLK are phase- and frequency-aligned. The output clock frequency is N times the input clock frequency.

Traditional PLL has several disadvantages when designing for low-bandwidth applications, like the need for big resistors and capacitors that are off-chip. Additionally the noise transfer characteristics of the semi-digital PLL are much better compared to the traditional PLL.

2 Semi-Digital PLL (SDPLL)

The block diagram of the semi-digital PLL is shown in Figure 2. The main difference between the traditional PLL and the semi-digital PLL is that the VCO employs a split control instead of a single control voltage used in Figure 1.

The VCO is controlled by the integral path with multiple controls which are mix of analog and digital (semi-digital) and the analog proportional control path. The locking of the PLL is always analog controlled.

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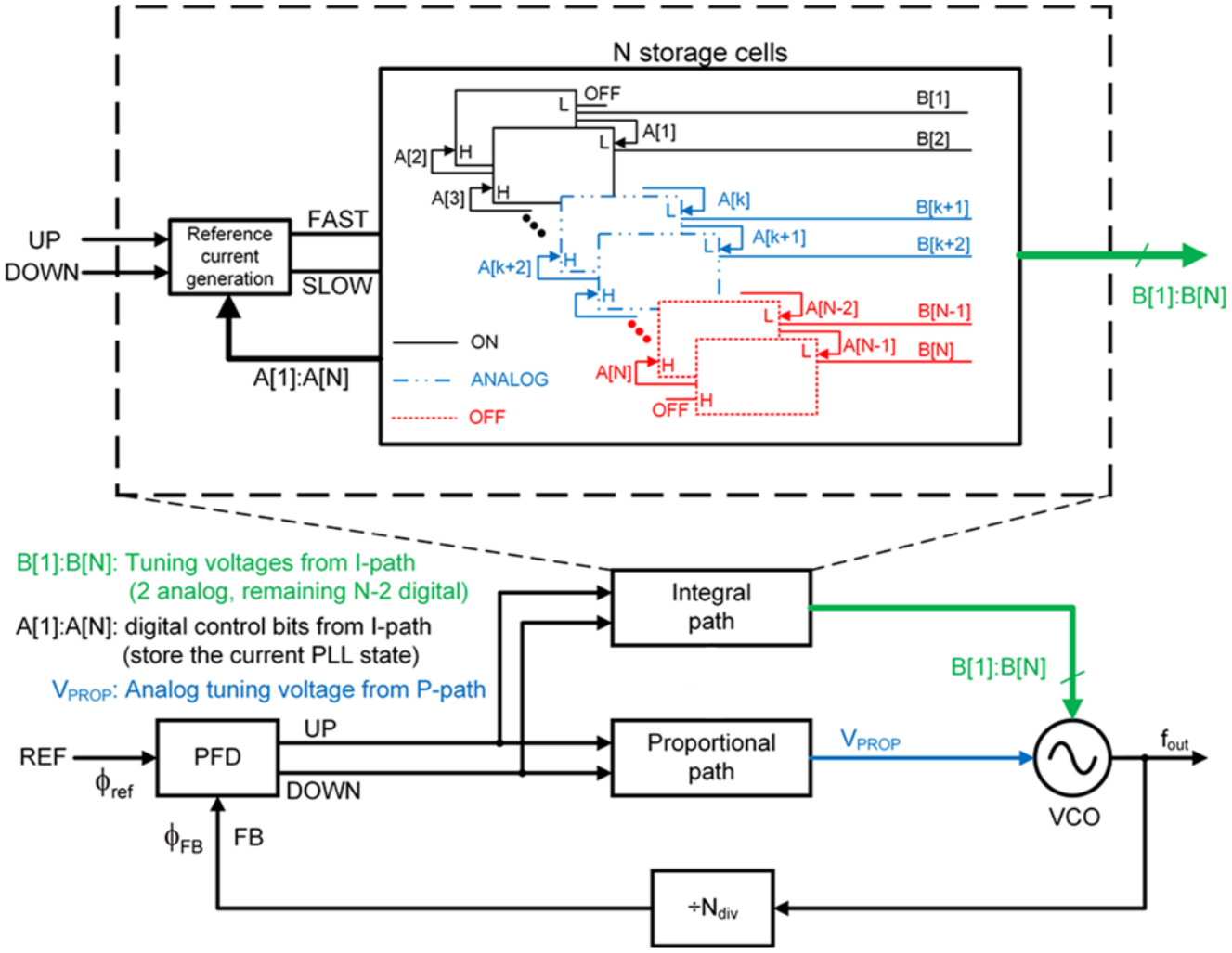

Figure 2. Semi-Digital PLL Block Diagram

2.1 Integral Path - Storage Cells Concept

As shown in Figure 2, the storage path consists of N elements called the storage cells. The control of the VCO for the target frequency is stored here. In the traditional PLL, the big loop filter capacitor C1 is used for the same purpose.

The storage cells are controlled by a Reference current block that is triggered by the PFD. The information in each storage cells can be stored as analog voltage or a digital bit (High/Low level). At every point in time, all SCs (storage cells) up to a certain position *k* are in digital HIGH/LOW state. Those after position *k + 2* are in digital LOW/HIGH state and the two intermediate SCs at *k + 1* and *k + 2* are in analog tuning mode. There is a very smooth handover from the digital to the analog control. Each storage cell enters the digital mode only after reaching the full HIGH or LOW level. Once in digital mode, the Reference current control has no effect to it and it keeps its state. Once in analog tuning mode, the output voltage gets affected by the Reference current block. As soon as the voltage on the active storage cell reached half of the supply voltage, the previous or next storage cell is released to the analog control from digital control. Handover of the controls is always active and depends on the voltage level of the active storage cell, which also means that there are at least two storage cell active in the analog control mode at any point in time.

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2.2 Proportional Path and Active Damping

Figure 3 shows the comparison of the active damping used in the semi-digital PLL and the damping in the traditional PLLs.

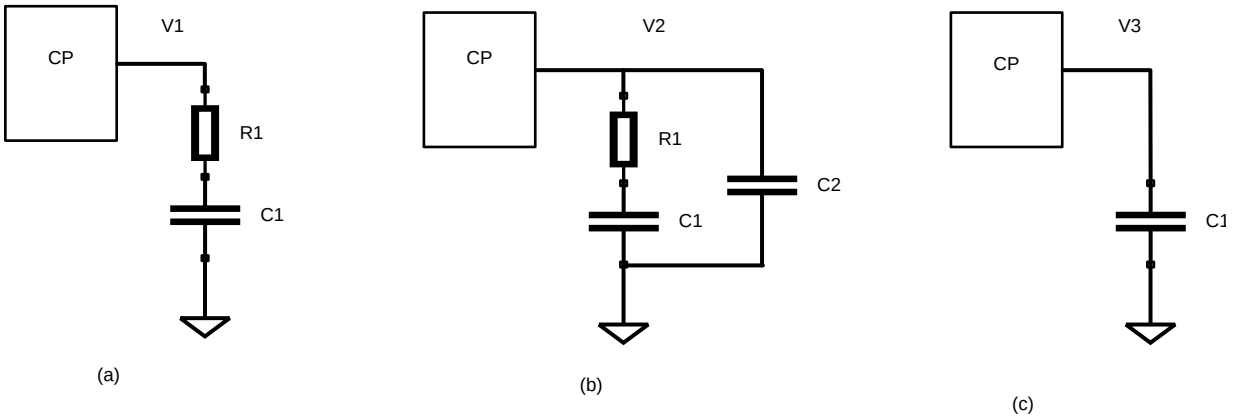

Figure 3. Loop Filter Comparison

As shown in Figure 3, the damping in the traditional PLL is achieved using a resistor in series to the big capacitor C1. Fig 3 (a) shows the CP and LPF of 2nd order conventional analog PLL, Fig 3(b) shows the CP and LPF of 3rd order conventional analog PLL, and Fig 3(c) is the proportional path in SDPLL. The output waveforms of the three configurations are also shown in Figure 4.

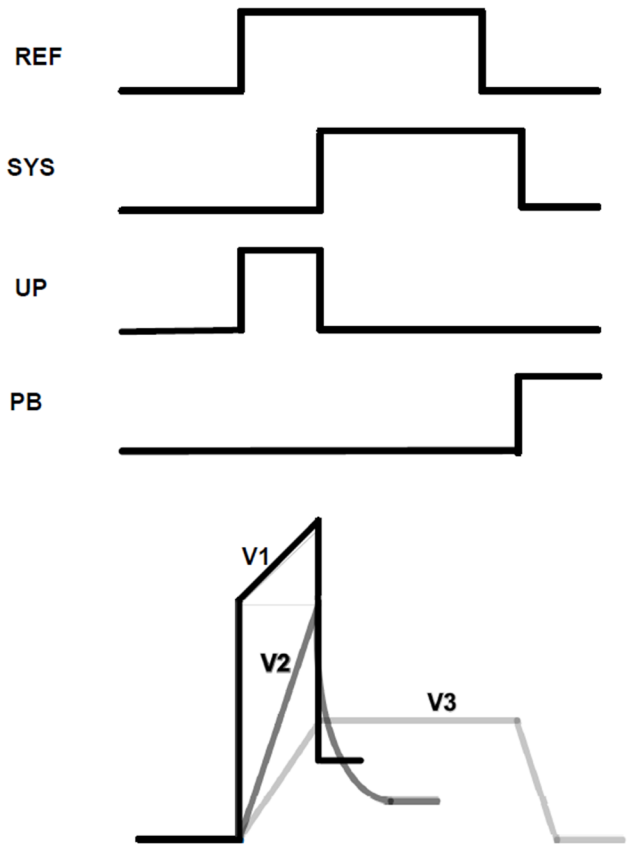

Figure 4. Loop Filter Voltage Comparison

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For configuration (a), Voltage V1 has huge spikes due to the resistor R1 when the rising edge of the UP comes. These spikes causes update jitter at the output of the VCO. To smooth out this effect the ripple capacitor C2 is added (configuration b). This spreads the effect on multiple VCO cycles and smooths out the sudden jumps in control voltage due to resistor R1.

For SDPLL in Fig 3(c), the proportional capacitor C1 is initialized to a nominal voltage by an active pullback circuit. When the PFD triggers the charge-pump with UP/DOWN signals, the voltage V3 on the proportional capacitor is pulled away depending on the width of the UP/DOWN signals. C1 retains its voltage for the rest of the cycle. PB signal pulls the C1 voltage to back to same nominal level before the start of next cycle. This creates a very low disturbance on the VCO control voltage and a more clean VCO output is obtained compared to the previous two cases. In Figure 4 under the same damping, the peak disturbance on the control voltage is lower in the case of SDPLL, and the effect is evenly spread across the VCO cycles.

3 PLL1 in LMK046xx Devices – Low Bandwidth PLL

PLL1 in the LMK046xx is based on SDPLL architecture, which gives the advantage of having very low bandwidths without the need for external Loop filter components. The PLL1 is used for jitter cleaning the input clock. The bandwidth can be programmed from 3 Hz to 300 MHz. The block diagram of the PLL is shown in Figure 5.

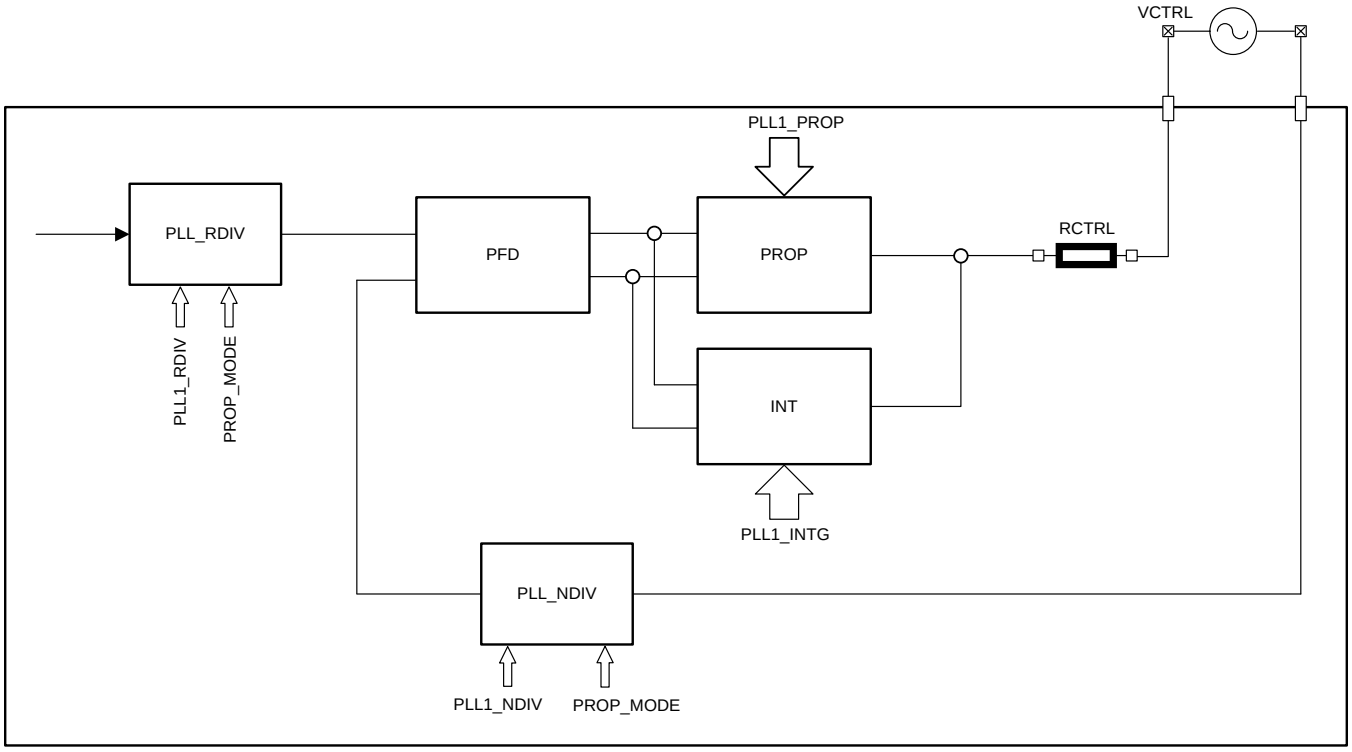

Figure 5. PLL1 Block Diagram

Due to the SDPLL architecture, PLL1 has split proportional (PROP) and integral path (INT) to the VCO control. The gain of the proportional and integral paths can be selected independently using the PLL1_PROP and PLL1_INTG. The PLL1 uses the active damping principal instead of a passive RC damping, which gives the advantage of having less noise transfer from the charge pump to the VCO. The PLL uses an external VCXO as a voltage-controlled oscillator. The PLL1 control voltage goes off-chip through the Vctrl Pin and must be connected to the external VCXO control voltage. The clock output from the external VCXO must be connected to the OSCin pin of LMK046xx devices to close the loop.

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3.1 PLL1 Integral Path

PLL1 integral path consists of Reference current block and a number of storage cells. The storage cells store the information for the VCXO control in semi-digital memory elements. The transition from one storage cell to the next happens in a smooth analog fashion with the help of two consecutive storage cells always active in the analog tuning mode. The remaining storage cells keep the information latched digitally.

The Integral Reference Current block defines the speed at which the storage cells are charged or discharged. In the holdover mode, the information inside the storage cells is frozen to keep the frequency constant while the input clock has lost. There are 16 settings (0 – 15) to control the speed of the storage path using PLL1_INTG, with 0 being the slowest setting and 15 being the fastest.

3.2 PLL1 Proportional Path

PLL1 proportional path uses an active damping concept. The proportional charge pump can be programmed using the PLL1_PROP. Additionally, the proportional path can be configured in three different ways using the PROP_MODE. It has an influences on the proportional gain and thereby the PLL bandwidth. It also provides another option to influence the PLL bandwidth.

3.2.1 Proportional Modes

The proportional gain can be influenced by the duty cycle of the PFD clock. It can be configured through the PLL_RDIV and PLL_NDIV using the PROP_MODE configurations.

There are three options supported by LMK046xx PLL:

- **Low Pulse Mode:** output clock duty cycle is 4 input clock cycles wide
- **High Pulse Mode:** output clock duty cycle is n-4 input clock cycle wide, with n being the divider ratio
- **50% mode:** the PFD clock duty cycle is 50%

When selected, the input clock to the PFD looks like as shown in Figure 6.

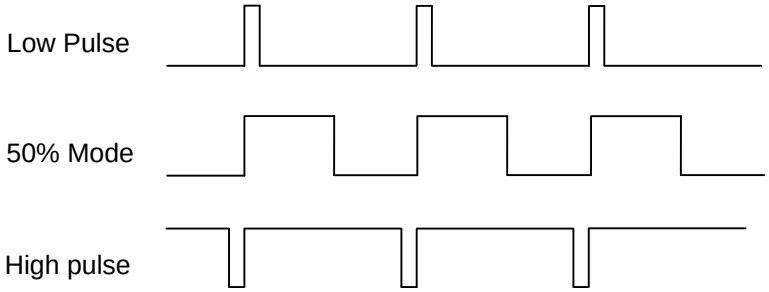

Figure 6. Three Mode Options Supported by the LMK046xx

Recapping the active damping concept explained in Section 2.2, the proportional voltage gets reset (pullback to nominal level) when the PB goes high. The PB is triggered when both input clocks to the PFD are at low level.

While using the 50% Mode, the proportional is effective for 50% of the PFD clock period and then the pullback resets the proportional voltage to its nominal value. In case of Low Pulse mode, the proportional is effective only for 4 VCXO cycles, which is less compared to using the 50% Mode, resulting in lower bandwidth. Similarly using the High Pulse mode, the proportional is effective for N-4 VCXO cycles, which is more than 50% of the PFD clock period and results in a higher loop bandwidth.

3.3 PLL1 Loop Filter Design Using TICSpro

To ease the loop design and choosing the right parameters, TICSpro software provides tools to Loop filter design. Snapshot of the PLL1 Loop filter design tool is shown in Figure 7.

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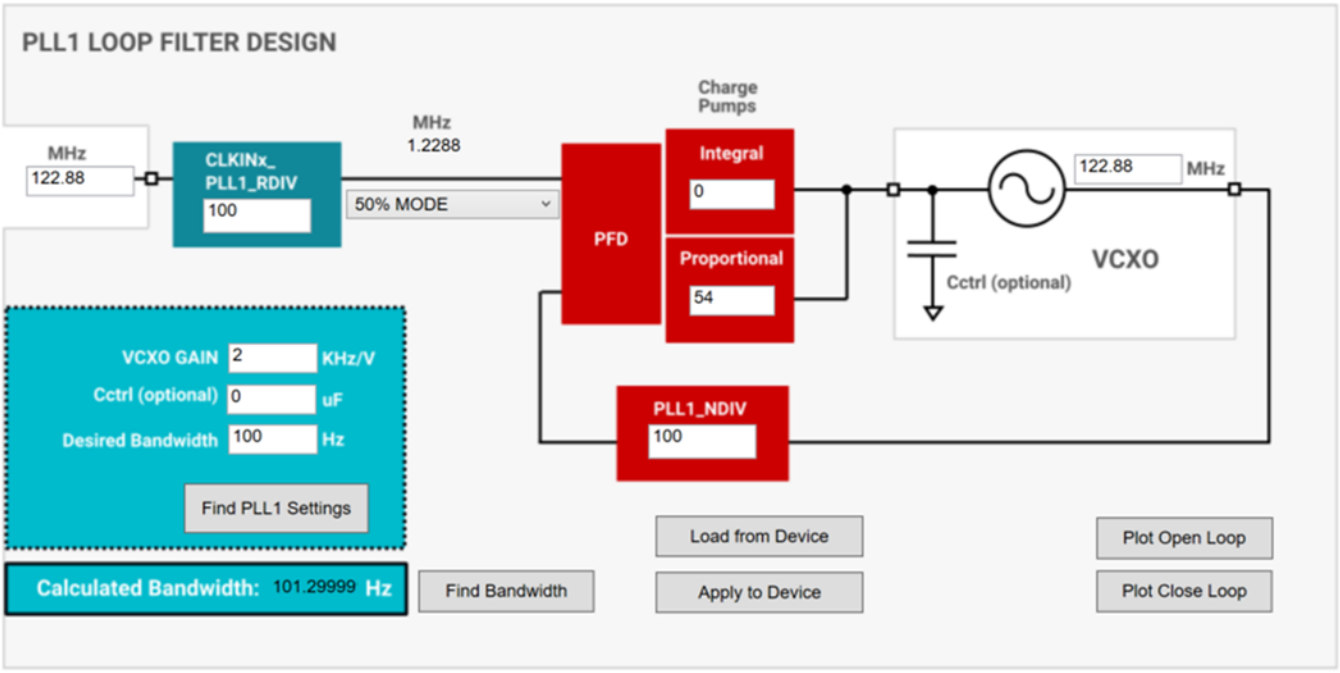
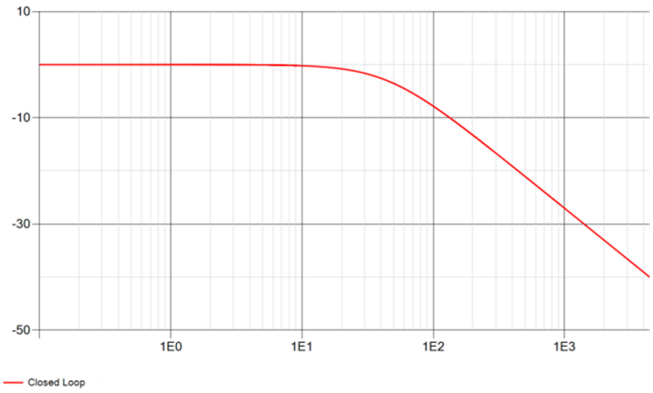


Figure 7. TICSpro PLL1 Loop Filter Tool

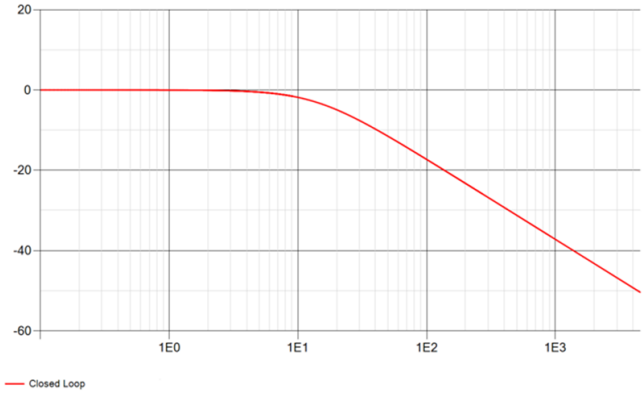
The user must enter the input clock frequency, VCXO frequency, PLL1_RDIV, PLL1_NDIV, and desired loop bandwidth. In addition, the VCXO gains must also be specified here, which can be found in the VCXO manufacturer specifications. The tool also provides option to load the settings directly from the control pages of the TICSpro if already available. By clicking the *Find PLL1 Settings* button, the tool automatically fills in the remaining fields based on the transfer function calculations, fulfilling the desired bandwidth. The user can also plot the open-loop and closed-loop responses using the two buttons *Plot Open Loop* and *Plot Close Loop*. After getting the desired settings, the PLL configuration can be loaded back to the device by clicking the *Apply to Device* button.

Figure 8 through Figure 10 shows the effect of changing the proportional setting (PLL1_PROP_SET) on the PLL bandwidth.



PLL1_PROP = 29

Figure 8. PLL1 Closed-Loop Responses With PROP Settings



PLL1_PROP = 9

Figure 9. PLL1 Closed-Loop Responses With PROP Settings

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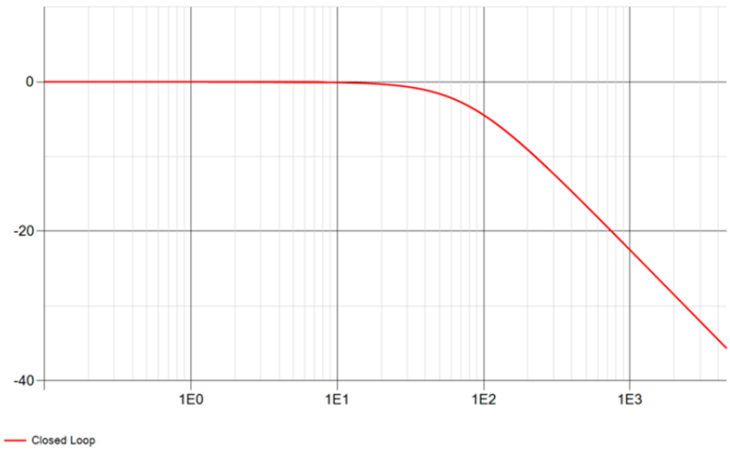
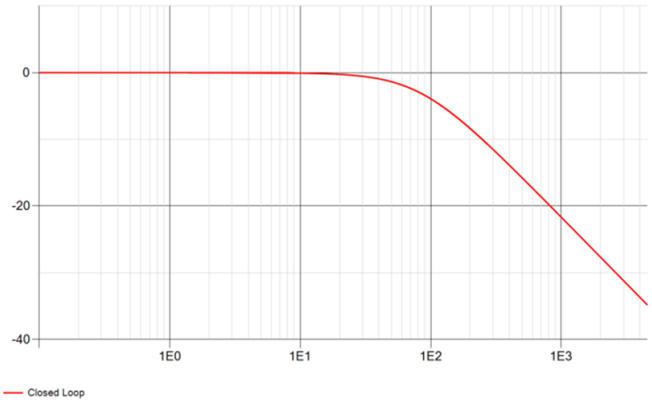


PLL1_PROP = 49

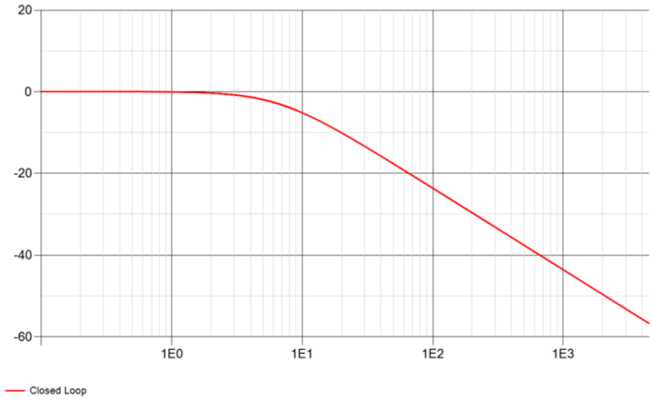
Figure 10. PLL1 Closed-Loop Responses With PROP Settings

As explained earlier, the input mode also affects the bandwidth of the PLL1. Figure 11 through Figure 13 shows the effect of changing the input mode on the bandwidth.



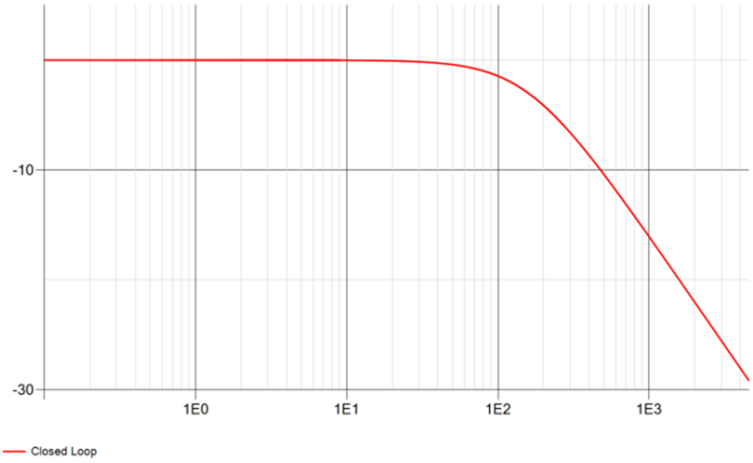
50% MODE

Figure 11. PLL1 Closed-Loop Responses With Input Modes



LOW PULSE MODE

Figure 12. PLL1 Closed-Loop Responses With Input Modes



HIGH PULSE MODE

Figure 13. PLL1 Closed-Loop Responses With Input Modes

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3.4 Higher Order Poles

As the control voltage is available off-chip, there is a possibility to add higher order poles in the PLL transfer function to clean the input clock better. As shown in Figure 5, a resistor RCTRL is integrated in the chip and typical value is 500 Ω. It is possible (optional) to add external capacitor or resistor and capacitor to create higher order pole as shown in Figure 14.

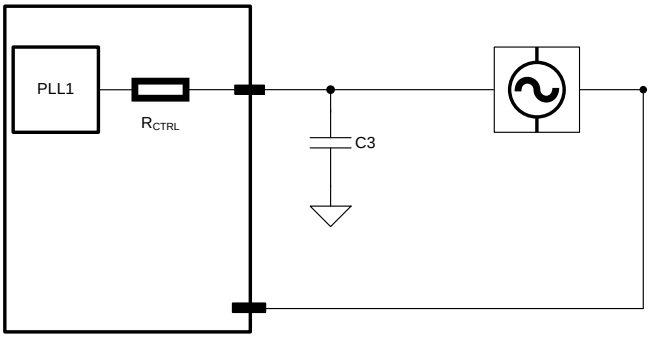
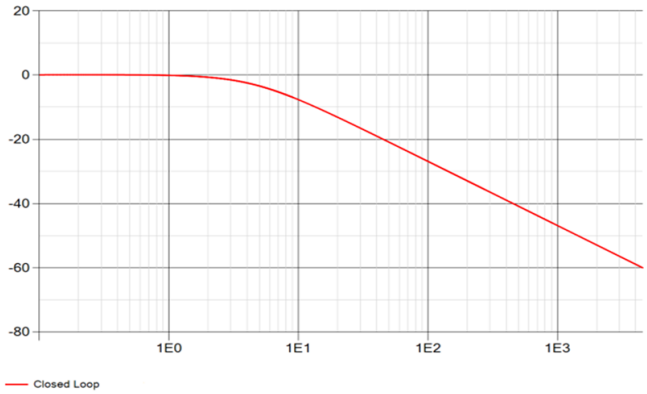


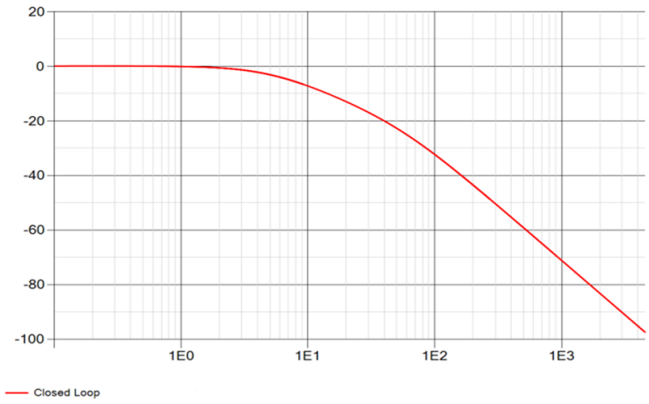
Figure 14. Adding 3rd Order Pole

Figure 15 and Figure 16 show two examples: one without an additional pole, and one with pole (where C3 = 4.7 µF is added). At 100 Hz, the input noise is filtered by –26 dB compared to –32 dB with the additional pole. At 1 KHz, the filtering is –46 dB without pole and –72 dB with the pole. The input is filtered with a slope of –40 dBc with one additional pole compared to a –20 dB slope without the additional pole.



Without C3

Figure 15. PLL1 Closed-Loop Response



With C3 = 4.7 µF

Figure 16. PLL1 Closed-Loop Response

Further higher order poles can be added by connecting additional RC pairs off chip as shown in Figure 17.

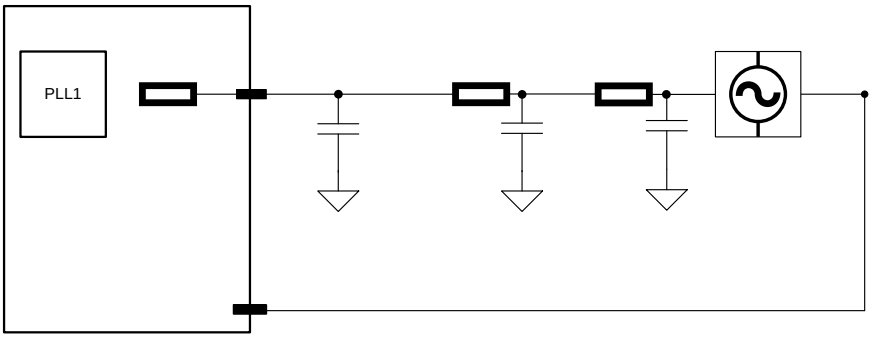


Figure 17. Higher Order Poles

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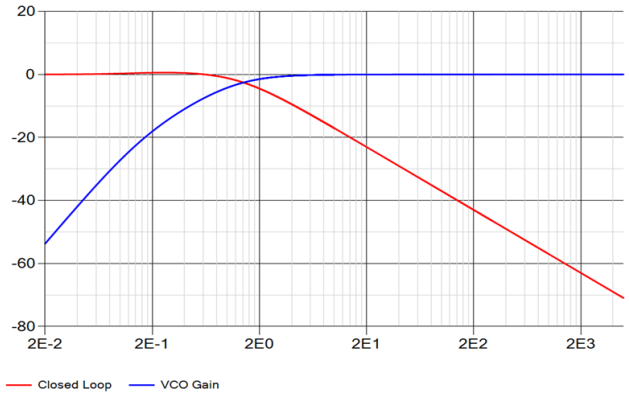
3.5 Integral Gain Settings

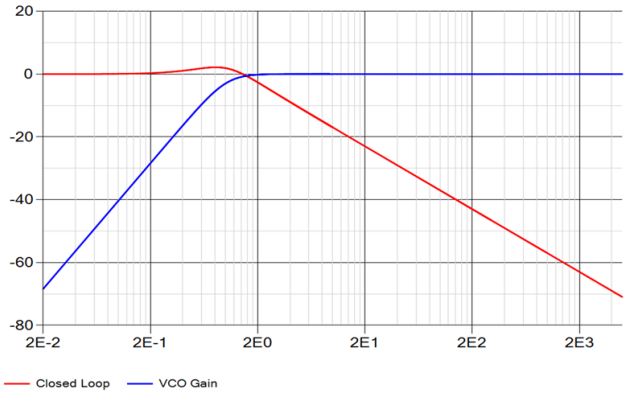
PLL1 integral gain can also be changed by using the PLL1_INTG settings, although TI recommends using the slowest setting 0. The integral gain settings influence the location of the Zero in the PLL transfer function. By using the higher settings, the Zero can be moved to the higher frequency giving better in-band VCXO noise cutting. It also degrades the PLL loop stability if moved too far out.

Figure 18 and Figure 19 show the PLL closed-loop transfer with PLL1_INTG = 0 and PLL1_INTG = 15. Looking at the VCO gain curve, the VCO noise is cut better in the case of PLL1_INTG = 15 compared to when PLL1_INTG = 1. Also note that the peaking in the closed-loop forward response increased. The noise in the storage path also increases while using the higher settings. TI recommends using the setting 0.



PLL1_INTG = 0

Figure 18. PLL1 Closed-Loop Response



PLL1_INTG = 15

Figure 19. PLL1 Closed-Loop Response

3.6 PLL1 Fast Locking

The lock time of the PLL1 can be reduced by using the fast locking feature. The PLL1_INTG_FL and PLL1_PROP_FL settings can be used in this case. At start-up, PLL1_INTG_FL and PLL1_PROP_FL are used to set the integral and proportional gain. When the PLL locks, the integral and proportional settings are replaced by PLL1_INTG and PLL1_PROP. As a result, the PLL1 locking can be started with high bandwidth and faster storage and later the settings are replaced by the second set of settings which are required for the final bandwidth. The fast lock settings ate automatically taken one time at start-up only.

3.7 PLL1 Phase Noise Bench Measurements

This section provides the phase noise measurements in PLL1 only mode. The TI standard LMK04616EVM is used for taking the measurements. As the PLLs in LMK0461x family of devices are same, the measurement results are also valid for LMK04610.

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3.7.1 Device Configuration

The device is configured in the PLL1 only mode as shown in the Figure 20.

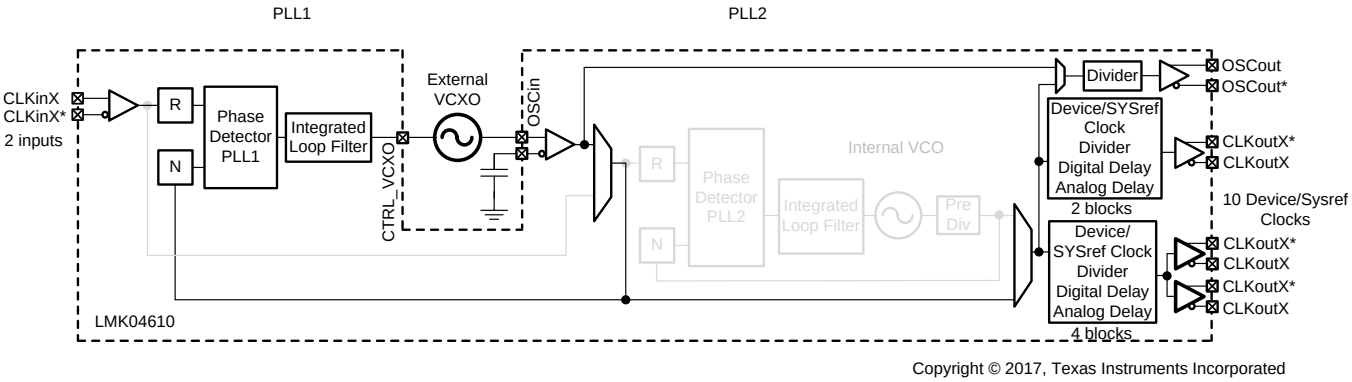

Figure 20. PLL1 Only Device Mode

All the phase noise measurements are performed at OSCout/OSCout* pins and PLL2 is disabled in this mode. For more information on the EVM and TICSpro setup, please refer to the EVM user guides of LMK04610 or LMK04616.

3.7.2 Input Clock

A differential input clock is used for these measurements and the phase noise performance of the clock is shown in the Figure 21.

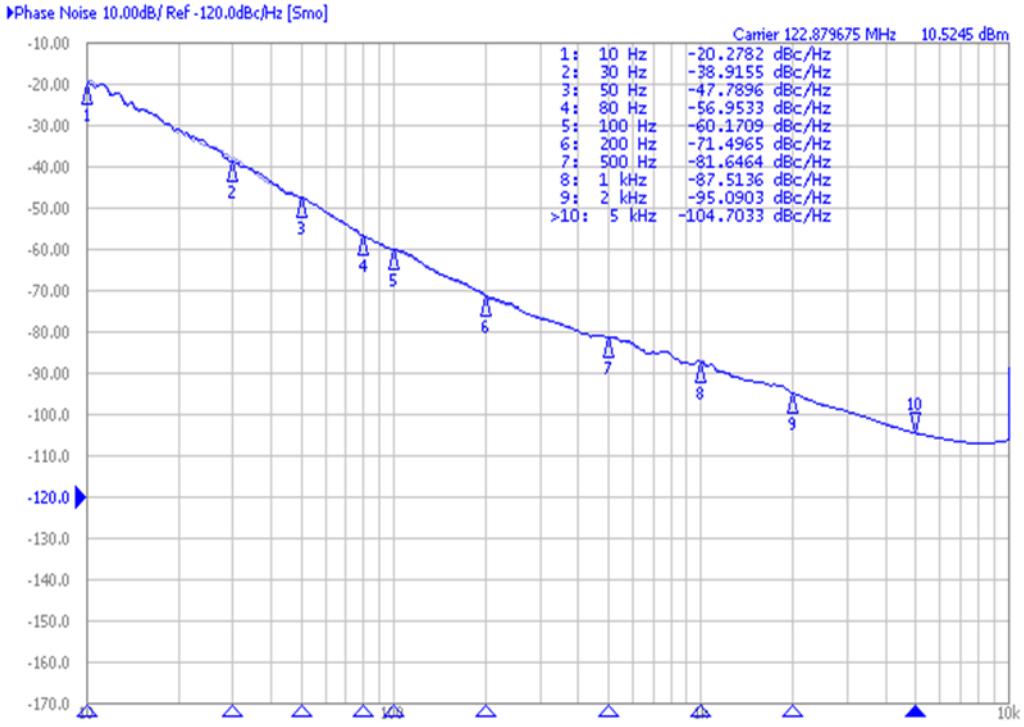

Figure 21. Input Clock Phase Noise

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3.7.3 Output Clock Phase Noise for Different Bandwidth Settings

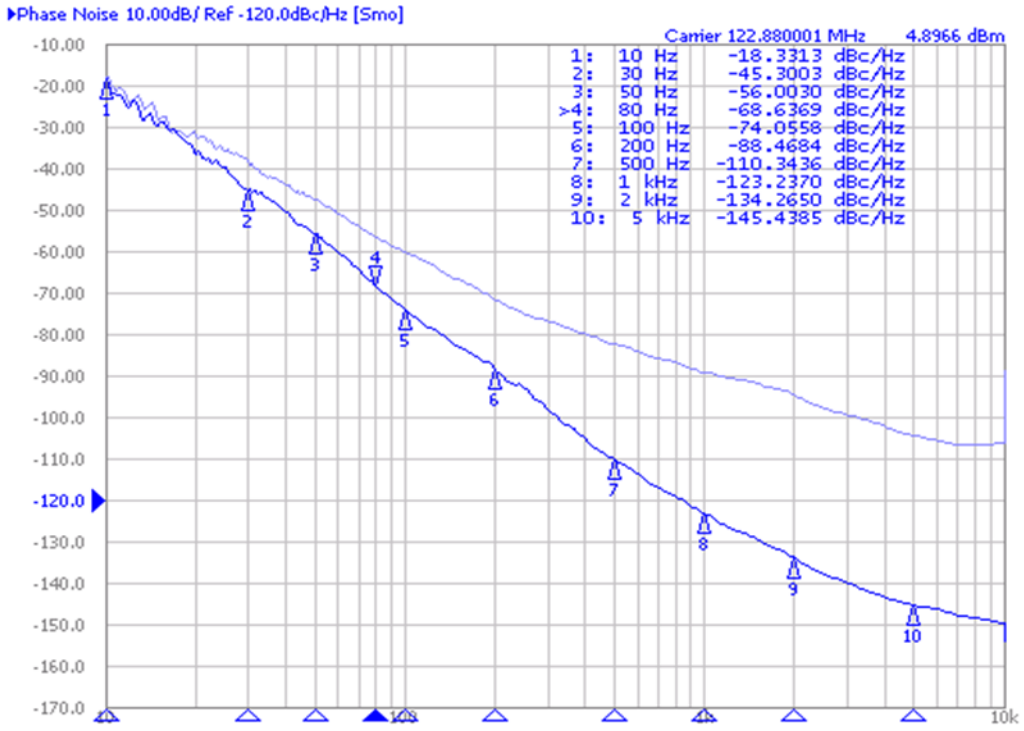

Figure 22. Output Clock Phase Noise With PLL1 BW = 20 Hz

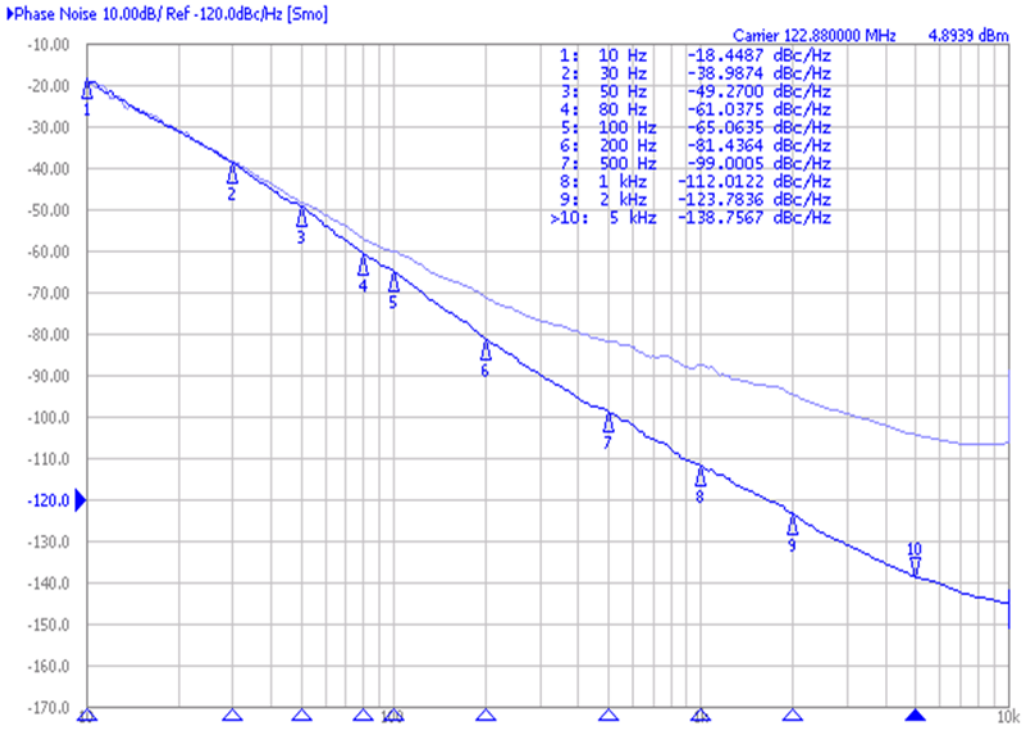

Figure 23. Output Clock Phase Noise With PLL1 BW = 60 Hz

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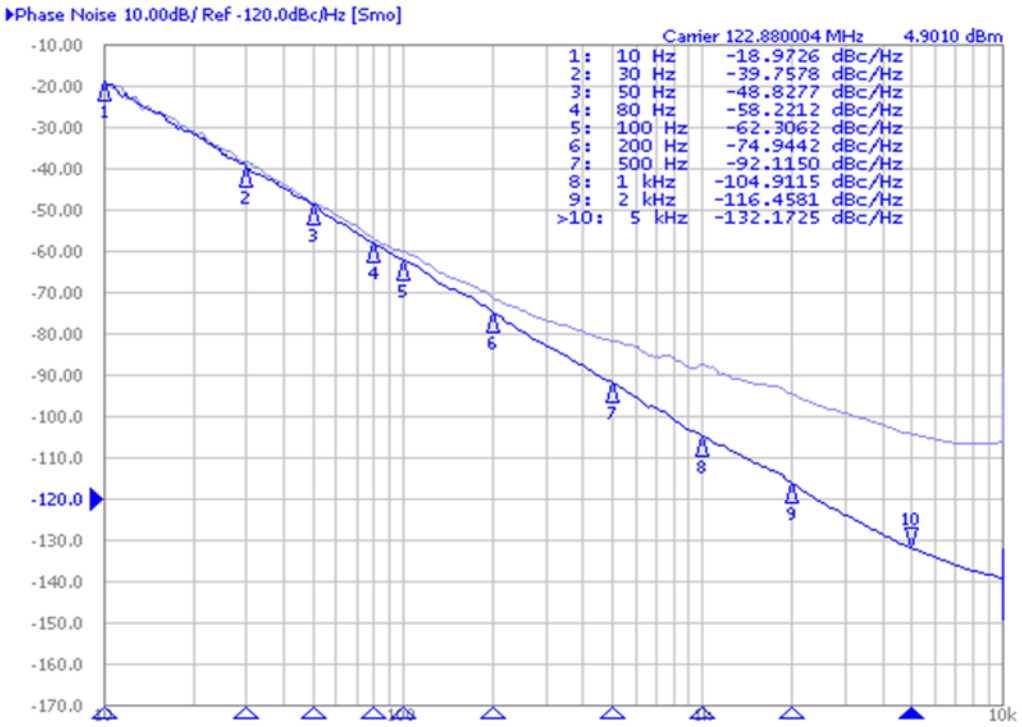

Figure 24. Output Clock Phase Noise With PLL1 BW = 100 Hz

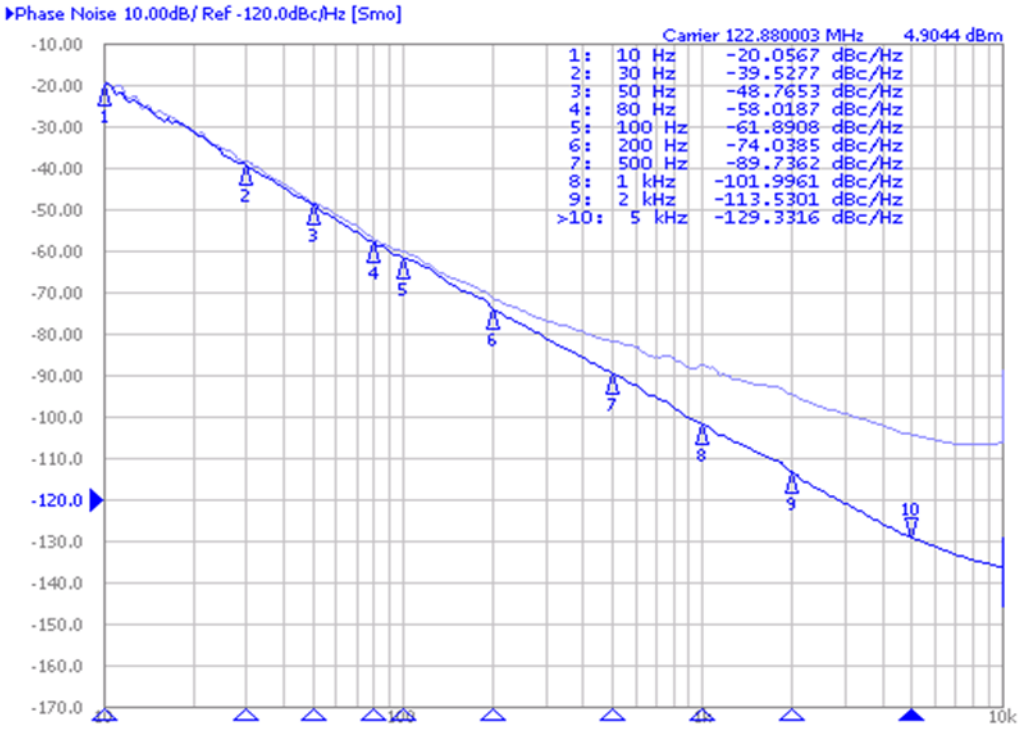

Figure 25. Output Clock Phase Noise With PLL1 BW = 250 Hz

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3.8 Output Clock Phase Noise With 3rd Order Pole

Phase noise plots in Figure 27 through Figure 30 show the impact of adding a third order pole. The PLL1 configuration is shown in the Figure 26. The on-chip RCTRL in combination with an external capacitor C3 creates an additional pole as explained in the previous sections.

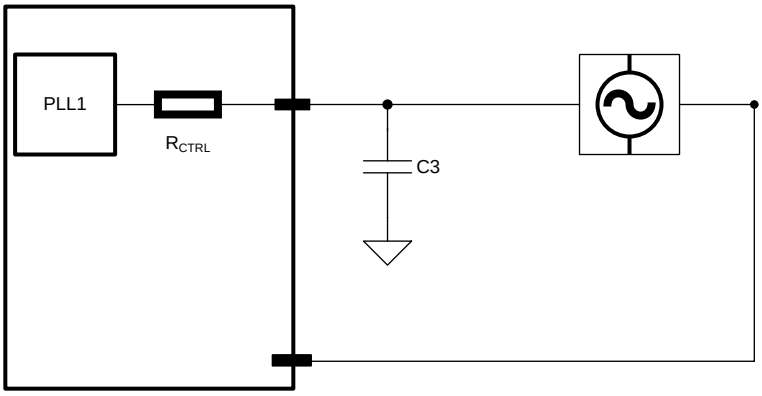

Figure 26. Adding 3rd Order Pole

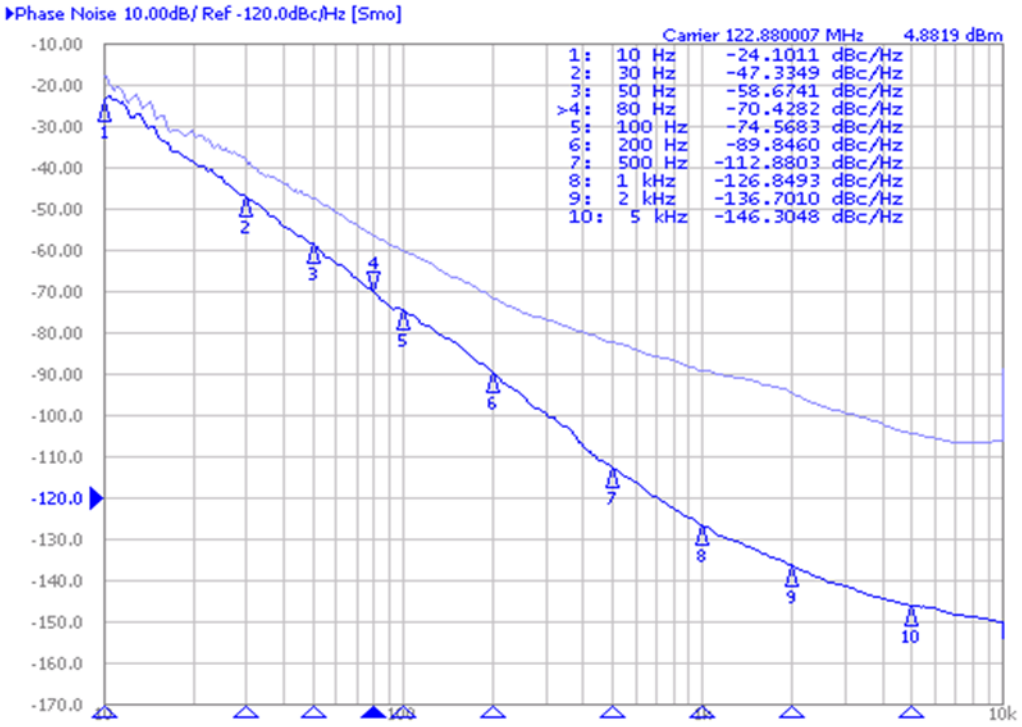

Figure 27. Output Clock Phase Noise With CCTRL = 200 nF

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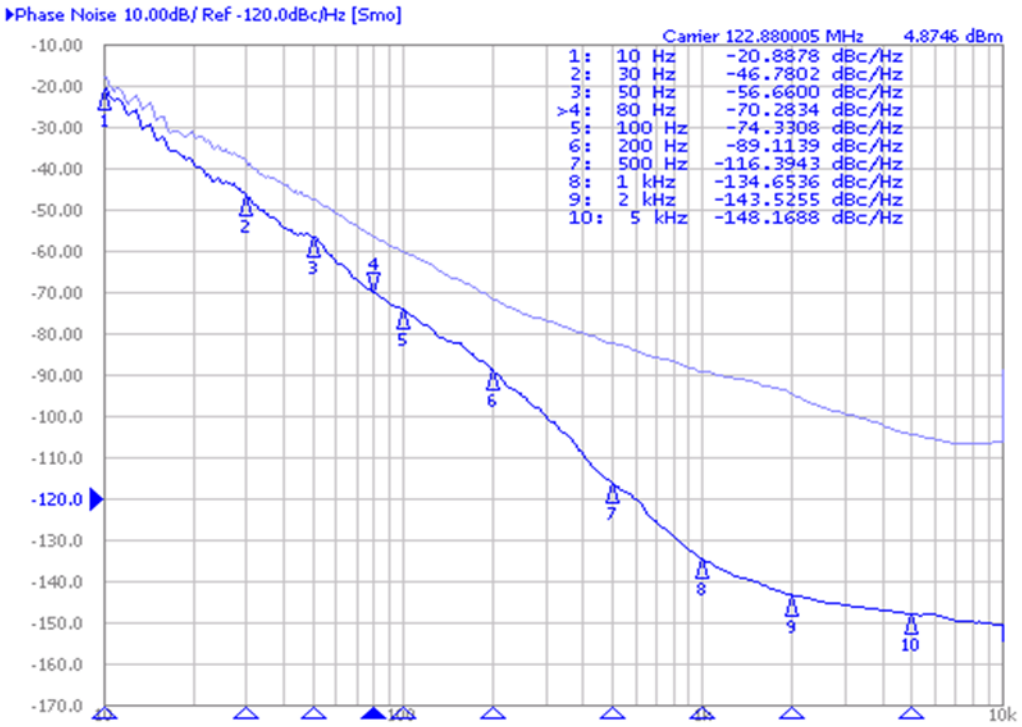

Figure 28. Output Clock Phase Noise With CCTRL = 1 µF

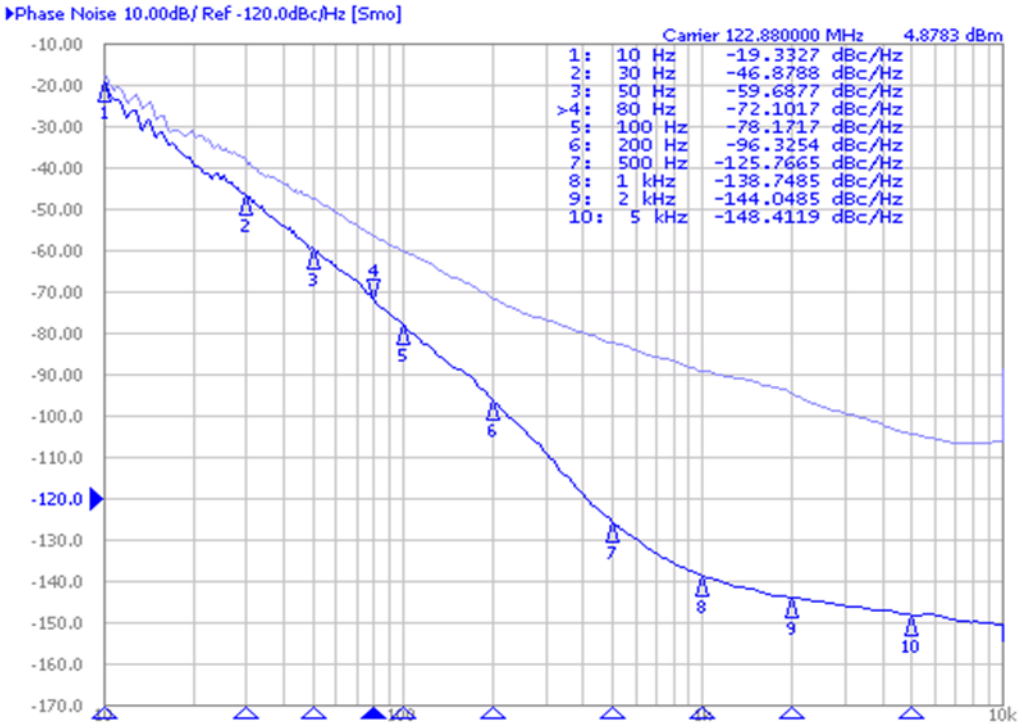

Figure 29. Output Clock Phase Noise With CCTRL = 4.7 µF

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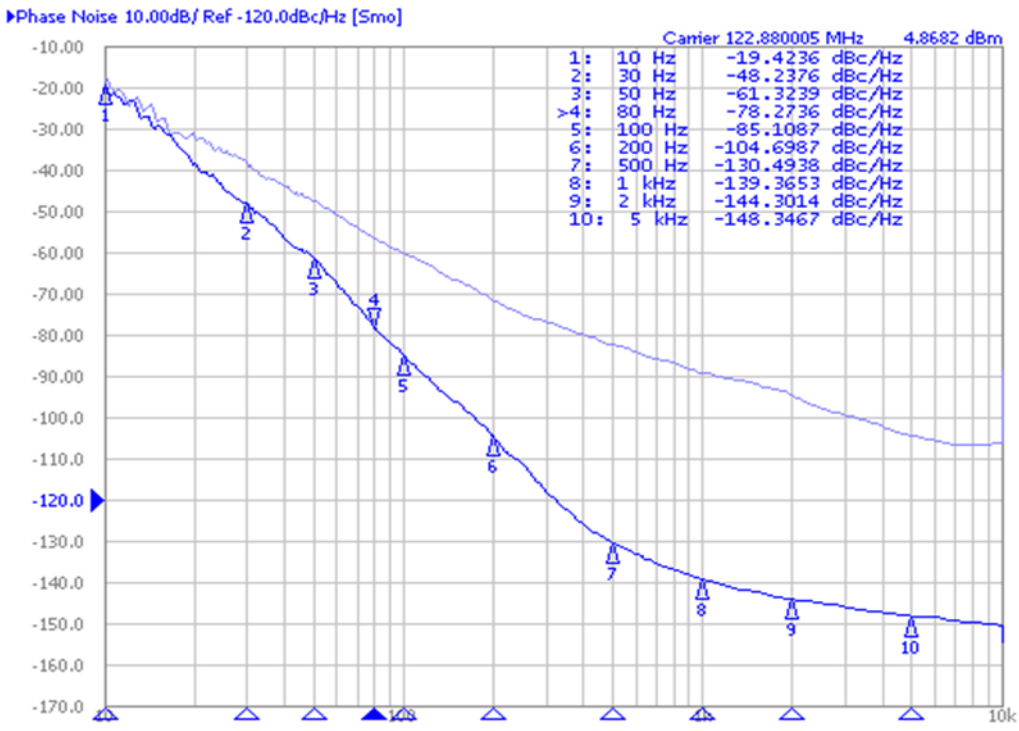

Figure 30. Output Clock Phase Noise With CCTRL = 10 µF

Bigger value of the CCTRL places the 3rd order pole at lower frequency, which helps to cut the input noise steeper. Looking at the phase noise plots, improvement can be clearly seen when comparing the phase noise at 100-Hz and 500-Hz offset frequencies.

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3.9 Achieving Very Low Bandwidths

Even lower bandwidths can be achieved by using lower PFD update frequencies. This can be achieved by using higher PLL1_RDIV and PLL1_NDIV divider values. Phase noise plots in Figure 31 and Figure 32 show very low bandwidths using lower PFD frequencies.

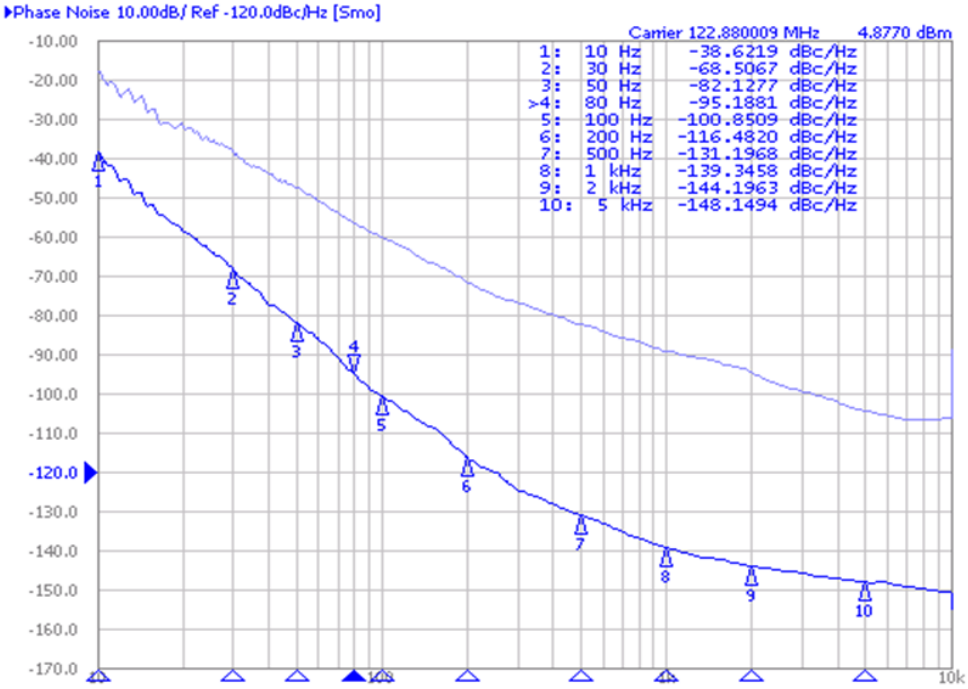

Figure 31. Output Phase Noise Using 1228.8-kHz PFD Frequency PLL1_RDIV = PLL1_NDIV = 100, Bandwidth = 1 Hz

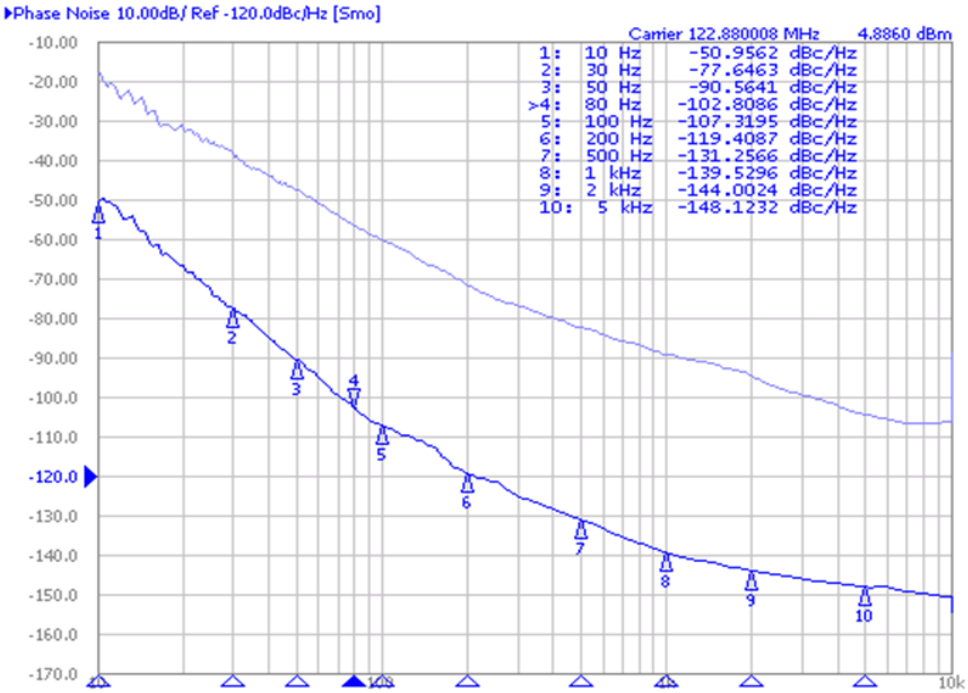

Figure 32. Output Phase Noise Using 307.2-kHz PFD Frequency Bandwidth = 0.7 Hz PLL1_RDIV = PLL1_NDIV = 400

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4 PLL2 in LMK046xx Devices: High Bandwidth PLL

The second PLL in LMK046xx is a high bandwidth PLL requiring no external components. The PLL contains a very low phase noise on-chip LC-based voltage-controlled oscillator (VCO). The PLL2 is very flexible and full programmable. Similar to PLL1, PLL2 is also based on semi-digital PLL architecture and is designed with an active damping concept. The bandwidth of the PLL can be programmed between 90 kHz to 1 MHz. PLL2 also has separated integral and proportional paths to control the VCO. The 3rd order pole can also be introduced by selecting the integrated resistors and capacitors. The block diagram of PLL2 is shown in Figure 33.

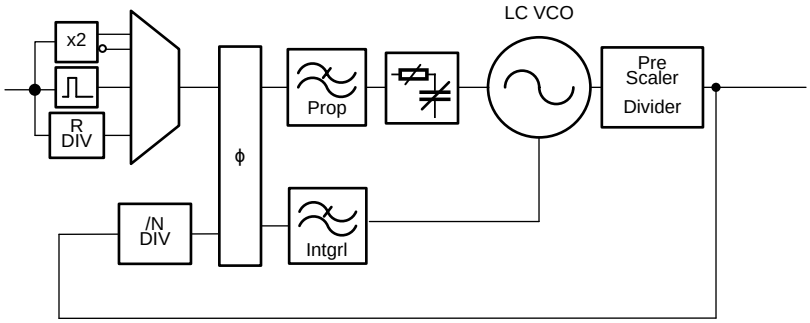

Figure 33. PLL2 Block Diagram

4.1 PLL2 Voltage-Controlled Oscillator

PLL2 contains a fully integrated high performance and very low phase noise LC oscillator. The frequency range of the oscillator is 5800 MHz to 6200 MHz. The VCO is tuned to the target frequency using the semi-digital control by the PLL2 loop. Due to the semi-digital control, the PLL loops tracks the temperature and input frequency change with its loop bandwidth. While selecting the PLL2 configuration, user must make sure that the VCO is always in this frequency range. To have a good supply rejection, VCO also contains a low noise on-chip LDO.

4.2 PLL2 Input Modes

PLL2 proportional path is also based on active damping principal as explained earlier. Four different input modes are supported to have more flexibility for bandwidth programming and are explained below:

- **Doubler mode:** In this mode, the input clock is multiplied by 2. The duty cycle of the clock in this mode is <50%.
- **Doubler invert mode:** This mode is same like the doubler mode, where the input clock gets multiplied by 2, but the duty cycle of the output clock is <50%.
- **Pulse mode:** In this mode, the duty cycle of the input clock is adjusted to a fixed value and is >50%.
- **RDIV mode:** In this mode, the input divider is used to divide down the frequency by user specified value with 50% duty cycle.

The output waveforms in these modes are shown in Figure 34.

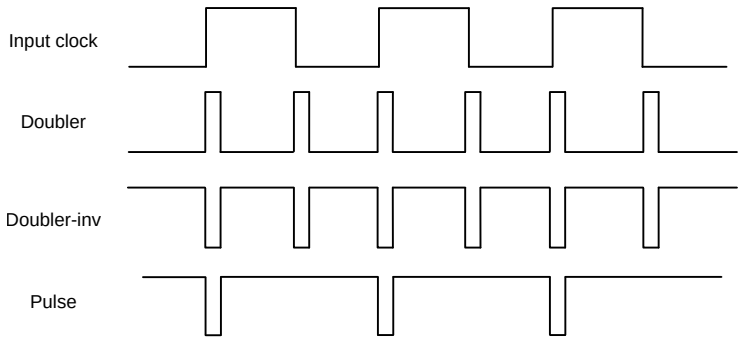

Figure 34. Clock in PLL2 Input Modes

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4.3 PLL2 Dividers

PLL2 has three different dividers and explained below:

- **PLL2_RDIV:** Input clock to the PLL2 can be divided down by 1 to 31 using reference divider PLL2_RDIV. The output duty cycle of the divider in this case is always 50%.
- **PLL2 Prescaler:** Prescaler in PLL2 is a high frequency divider and is used to divide down the VCO clock. The divider value can be selected from 3 to 6. The clock tree clock frequency going directly to the input of Channel dividers is always the output of the Prescaler.
- **PLL2 NDIV:** This divider is in the PLL2 feedback path which defines the PLL frequency multiplication ratio in combination with prescalar. PLL2_NDIV can be programmed from 1 to 65535 and always provides a 50% duty cycle output.

4.4 PLL2 Loop Filter

As mentioned already, PLL2 design is also based on semi-digital PLL architecture where the proportional and integral parts are separated from each other. Proportional gain and integral gain can be individually programmed by the user to define the bandwidth and noise transfer characteristics of the PLL2 in combination with the input modes.

4.5 PLL2 Loop Filter Tool in TICSpro

To ease the design process, TICSpro software comes with a tool for PLL2 also to automatically generate the loop filter settings based on the user specified bandwidth. In addition, user can change the settings manually and plot the open-loop and closed-loop response to optimize the loop filter settings as per the design need. A snapshot of the PLL2 Loop filter tool is shown in Figure 35.

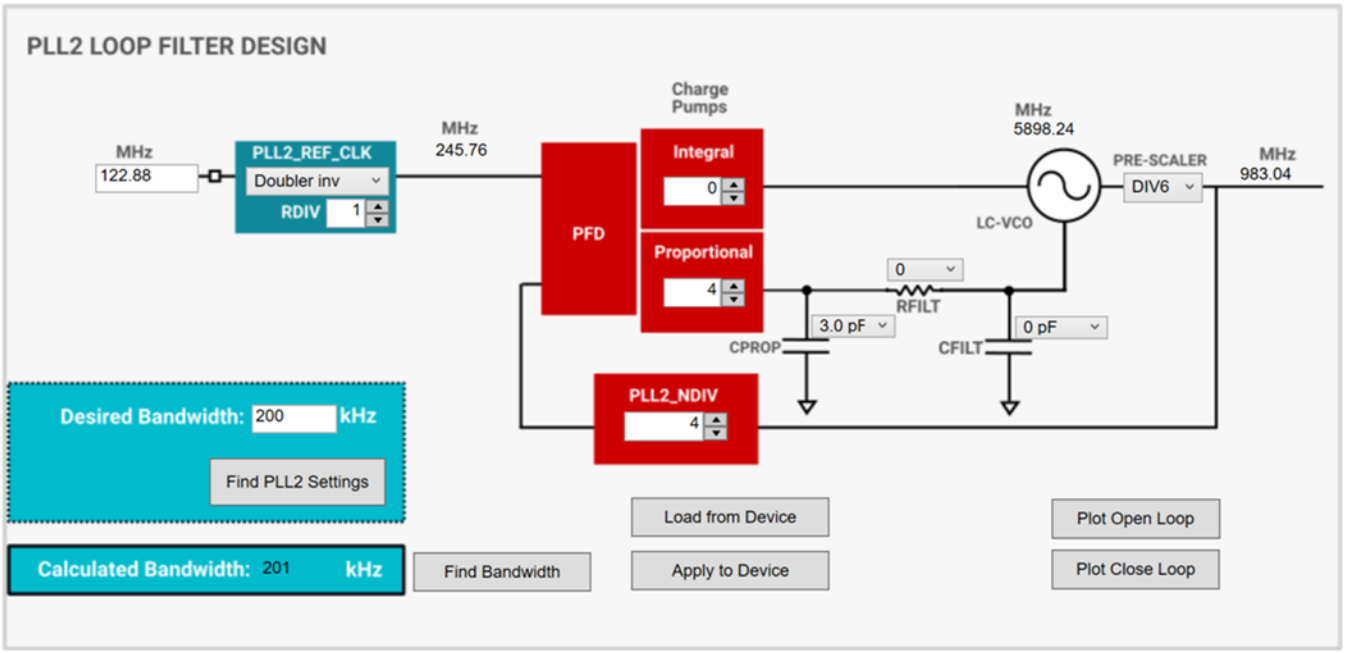

Figure 35. TICSpro PLL2 Loop Filter Design Tool

User must enter the input frequency field, the desired PLL bandwidth and the correct divider values. There is an option to load the settings from the *PLL2* page directly by clicking the *Load from Device* button. To get the correct loop filter settings, user must click *Find PLL2 Settings*. The open-loop and closed-loop responses can be plotted by clicking the corresponding buttons on the right-hand side.

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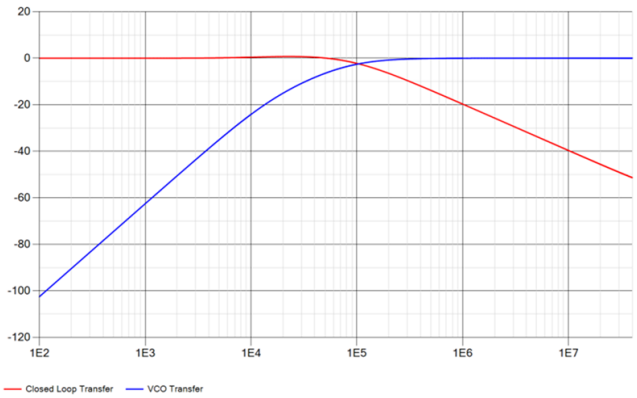
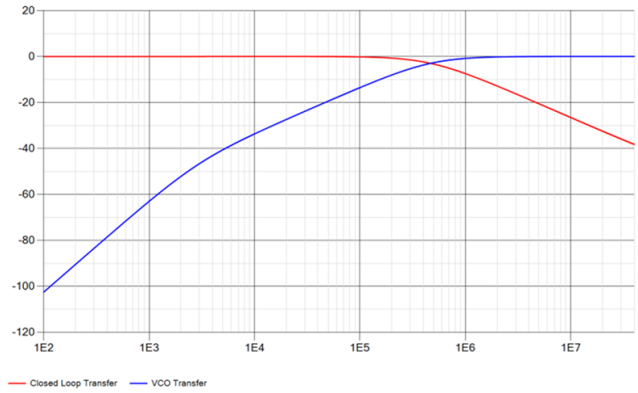
4.6 PLL2 Proportional Path

PLL2 proportional path employs active damping principal. The proportional gain can be changed using PLL2_PROP and PLL2_CPROP settings. The difference between the two modes is, PLL2_PROP controls the proportional charge pump current to define the proportional gain and PLL2_CPROP controls the on-chip capacitor used in active damping to define the proportional gain. PLL2_PROP can be selected from 1 to 63. There are four options to select from for PLL2_CPROP, from 3 pF to 5.4 pF.



PLL2_PROP = 2

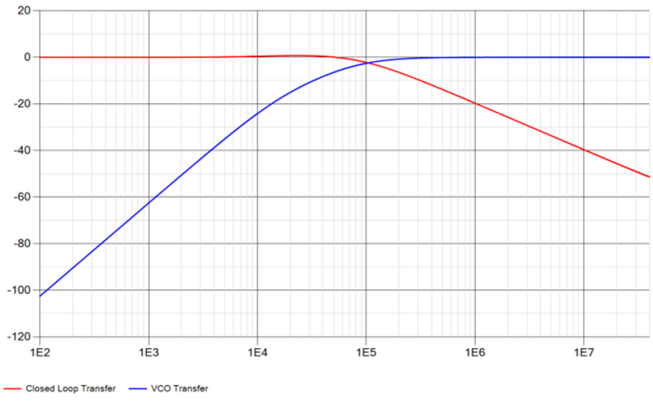
Figure 36. PLL Closed-Loop Response by Changing PLL2_PROP Settings



PLL2_PROP = 12

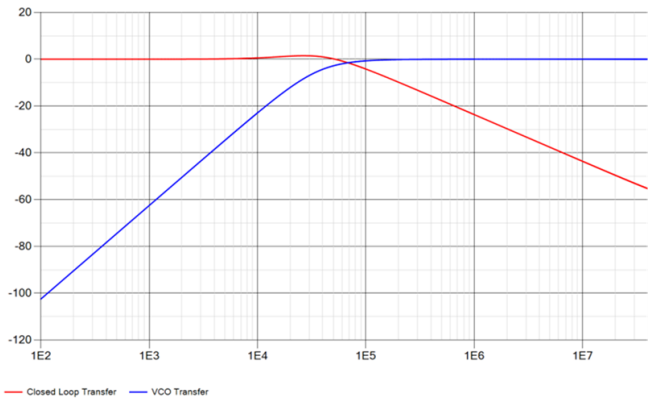
Figure 37. PLL Closed-Loop Response by Changing PLL2_PROP Settings

Higher values of PLL2_PROP result in higher proportional gain as shown in Figure 36 and Figure 37. Higher PLL2_CPROP values result in lower proportional gain (see Figure 38 and Figure 39). To lower the bandwidth further, 3rd order filter capacitor (CFILT) can also be used as a capacitor on proportional voltage by keeping the RFILT=0, although TI does not recommend this because the lower proportional gain also makes the loop stability worse as shown in Figure 40 and Figure 41



PLL2_CPROP = 3 pF

Figure 38. PLL Closed-Loop Response vs PLL2_CPROP Settings



PLL2_CPROP = 5.4 pF

Figure 39. PLL Closed-Loop Response vs PLL2_CPROP Settings

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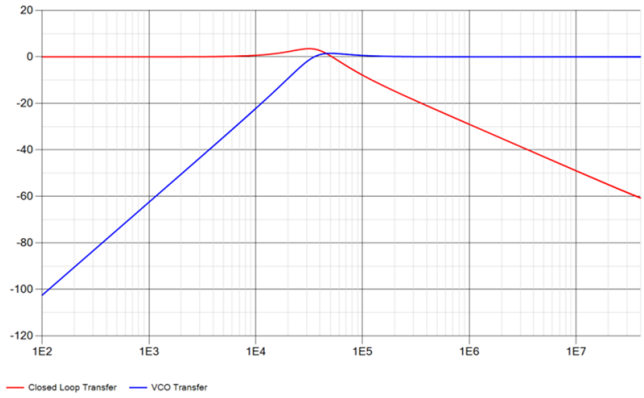
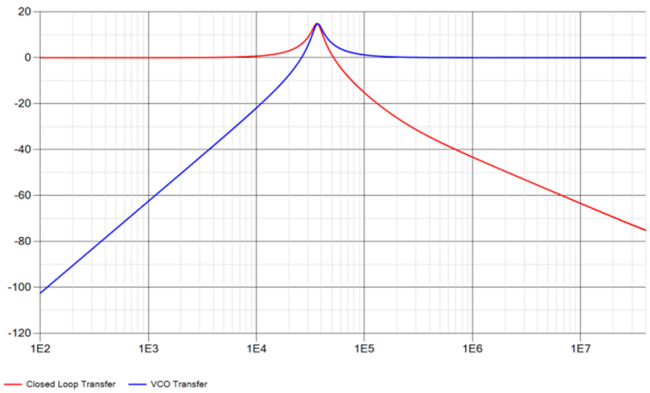


PLL2_CPROP = 3 pF, PLL2_CFILT = 8 pF

Figure 40. PLL Closed Response vs PLL2_CFILT Settings

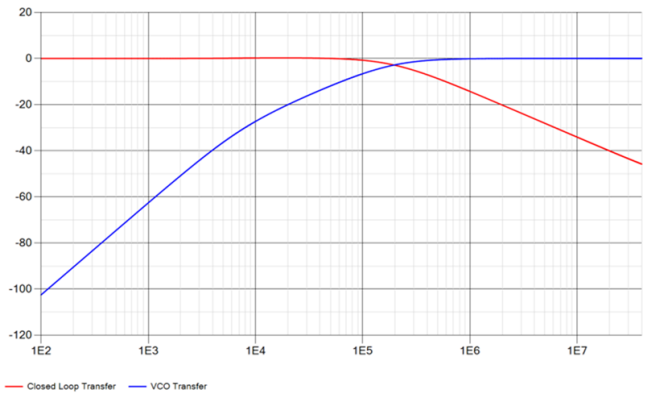


PLL2_CPROP = 3 pF, PLL2_CFILT = 60 pF

Figure 41. PLL Closed Response vs PLL2_CFILT Settings

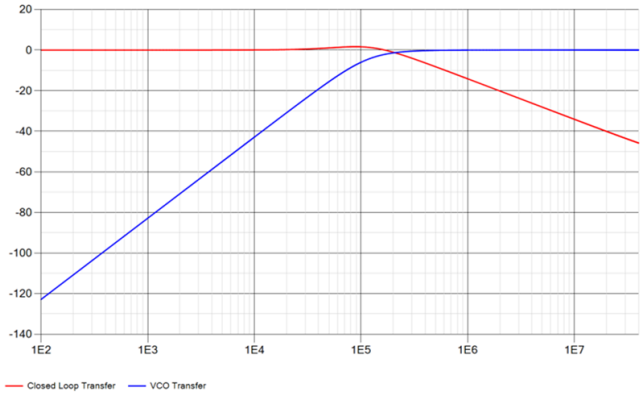
4.7 PLL2 Integral Path

PLL2 integral gain can also be programmed selecting PLL2_INTG from 0 to 31. As shown in Figure 42 and Figure 43, faster integral path helps to cut the VCO noise better. TI recommends using the setting 0 for integral gain, but it is not recommended. While using the higher settings, consider that the VCO noise can be cut better at the cost of higher noise from the integral path and worse stability. PLL2 plotting options in the PLL2 Loop Filter tool helps to analyze the stability while playing with the integral gain options.



PLL2_INTG = 0

Figure 42. PLL2 Closed-Loop Response vs PLL2_INTG Settings



PLL2_INTG = 10

Figure 43. PLL2 Closed-Loop Response vs PLL2_INTG Settings

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4.8 PLL2 Higher Order Pole

PLL2 also has programmable fully integrated 3rd order loop filter in the proportional path to create additional pole for better noise filtering. The resistor value RFILT can be selected as 4.7k or 9.2k. The capacitor value CFILT can be selected from 4 pF to 124 pF in 4-pF steps. Figure 44 shows the PLL closed-loop response without the third order pole, while Figure 45 shows the closed-loop response with an additional pole (RFILT = 9.2 kΩ, CFILT = 40 pF). The closed-loop PLL gain at 10 MHz is –68 dB with the pole compared to –40 dB without the pole.

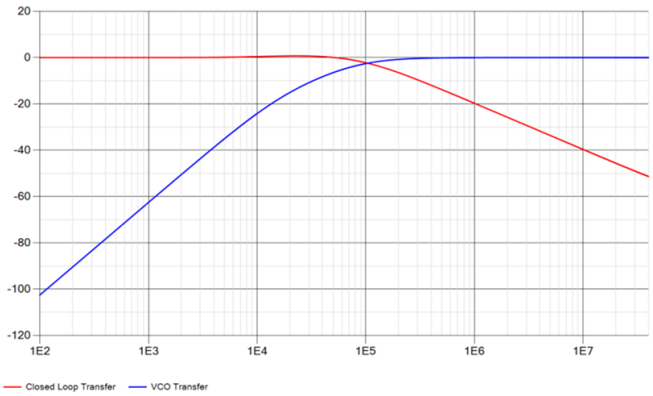

Figure 44. PLL Closed-Loop Response With 3rd Order Pole

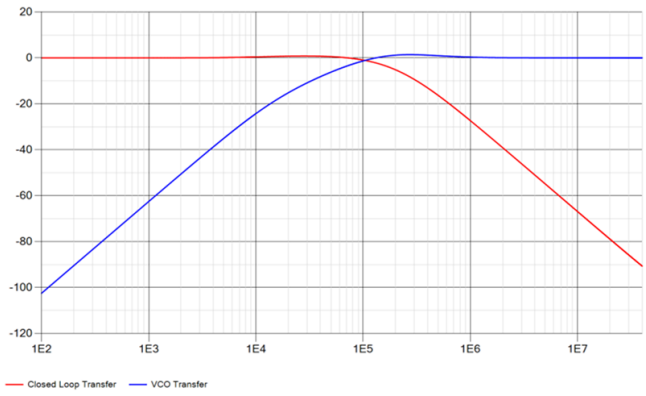

Figure 45. PLL Closed-Loop Response Without 3rd Order Pole

4.9 PLL2 Phase Noise Bench Measurements

Phase noise plots presented in this section are for PLL2 only mode using TI standard LMK04616EVM . As the PLLs in LMK0461x family of devices are same, the measurement results are also valid for LMK04610.

4.9.1 Device Configuration

The device is configured in the PLL2 only mode as shown in the Figure 46.

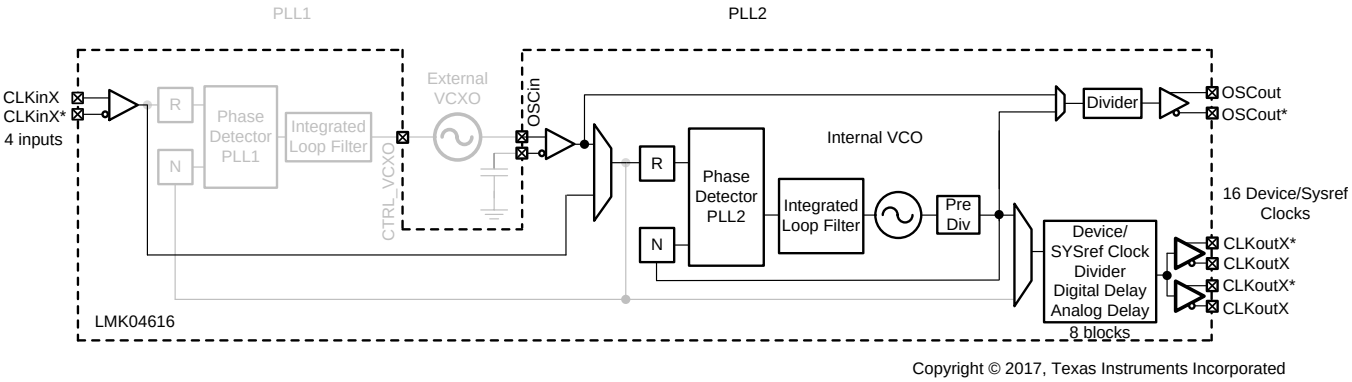

Figure 46. PLL2 Only Mode

PLL1 is disabled and CLKIN input is directly applied to the PLL2. The phase noise is measured at CLKoutX/CLKoutX* outputs.

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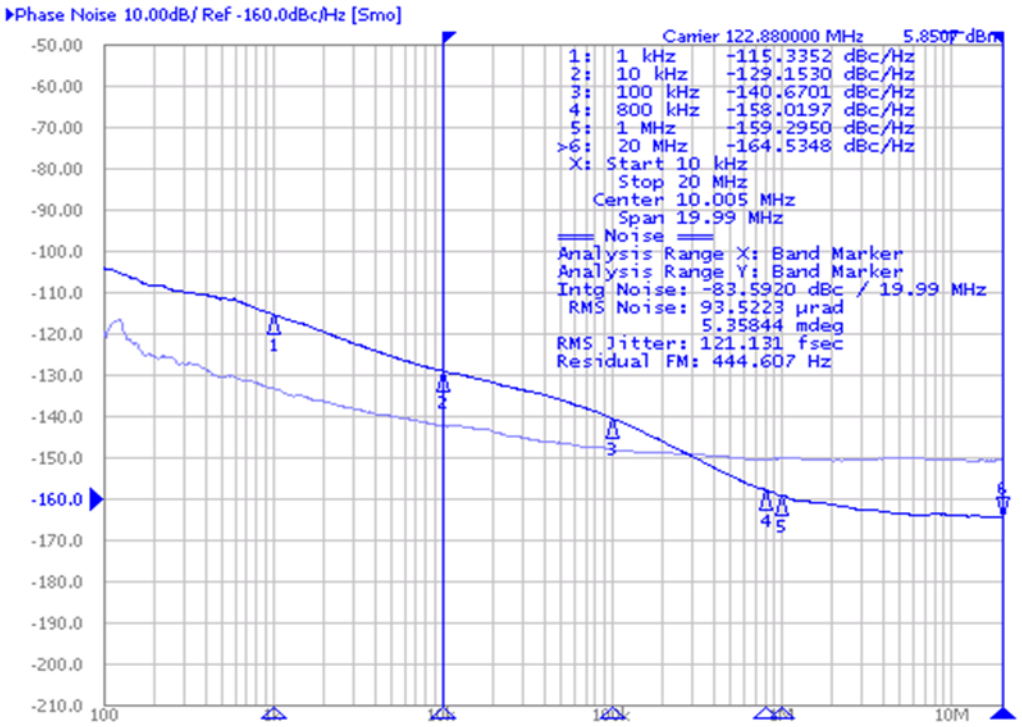

Figure 47. Output Clock Phase Noise With PLL2, BW = 75 kHz

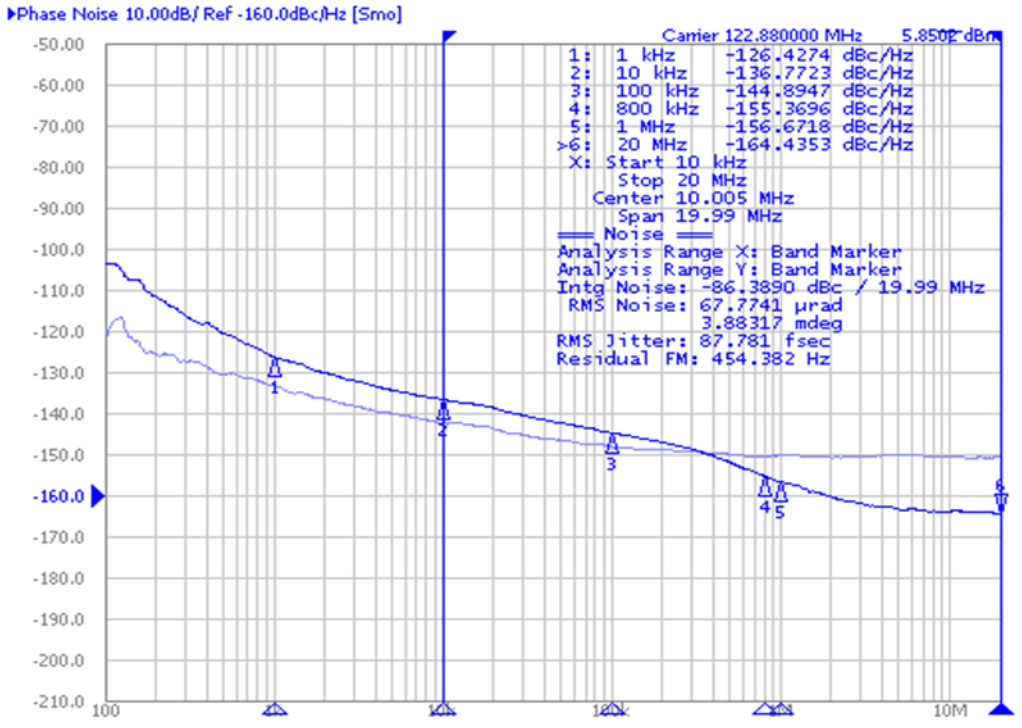

Figure 48. Output Clock Phase Noise With PLL2, BW = 400 kHz

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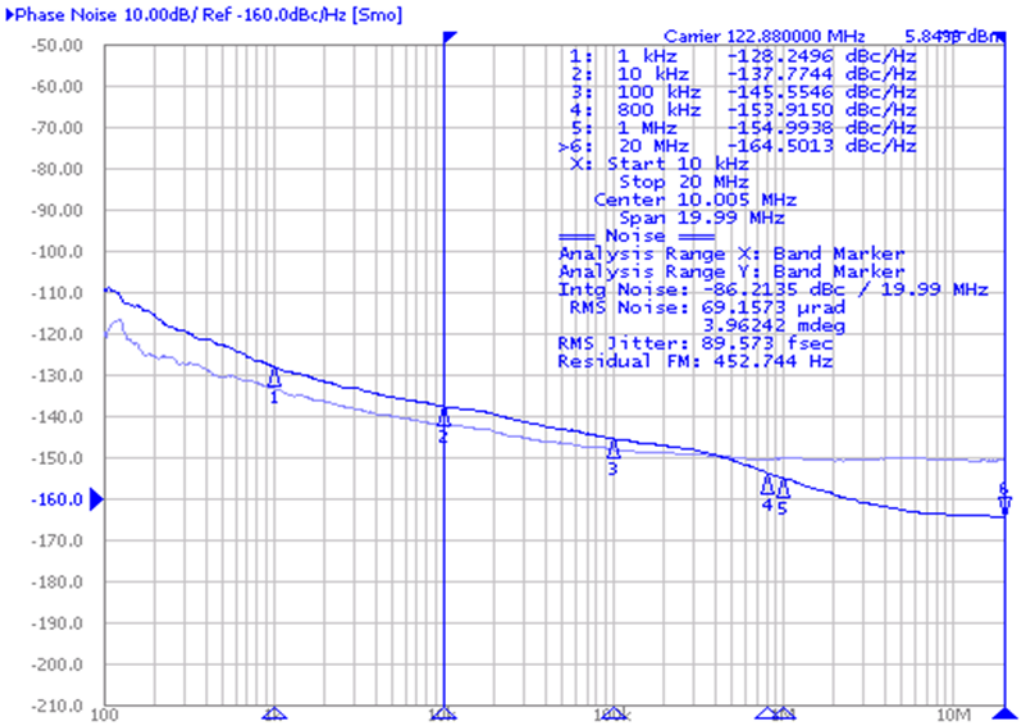

Figure 49. Output Clock Phase Noise With PLL2, BW = 600 kHz

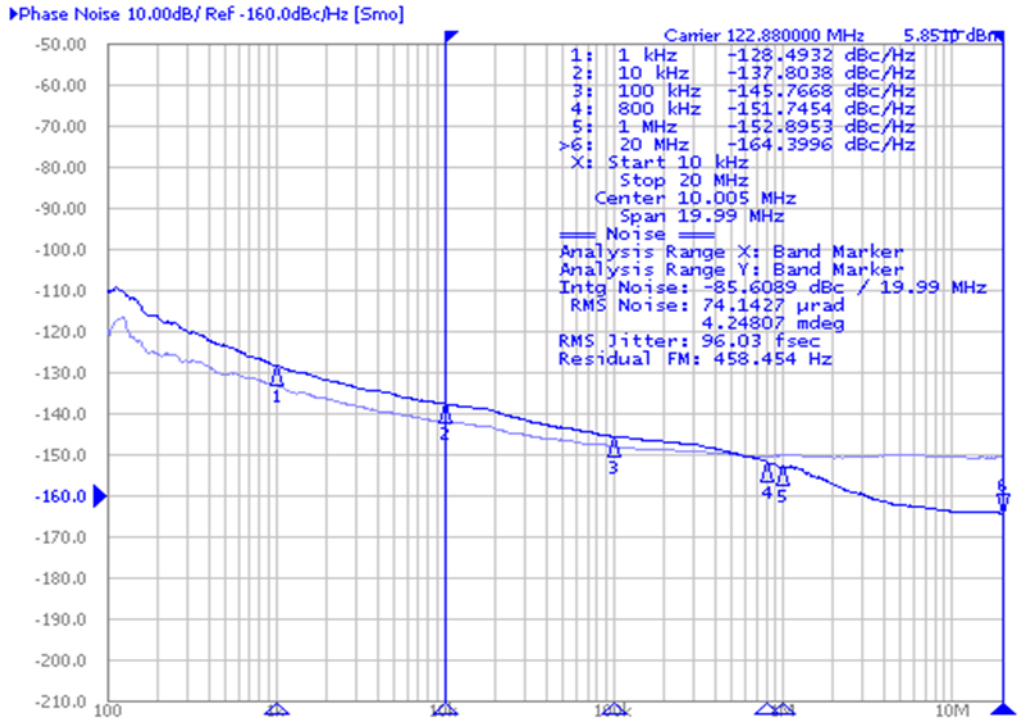

Figure 50. Output Clock Phase Noise With PLL2, BW = 1.5 MHz

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4.9.2 Output Clock Phase Noise With 3rd Order Pole

As explained previously, PLL2 has fully integrated and programmable 3rd order pole. The capacitor and resistor can be selected by user from the predefined values. Following measurements show the phase noise performance without and with 3rd order pole.

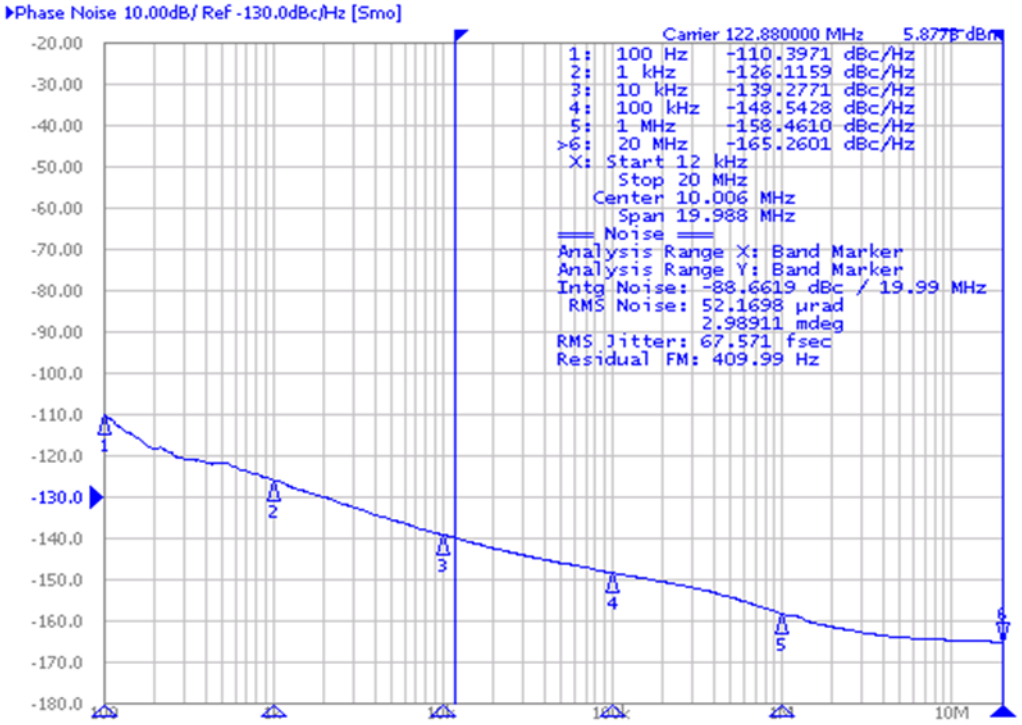

Figure 51. Output Clock Phase Noise Without 3rd Order Pole

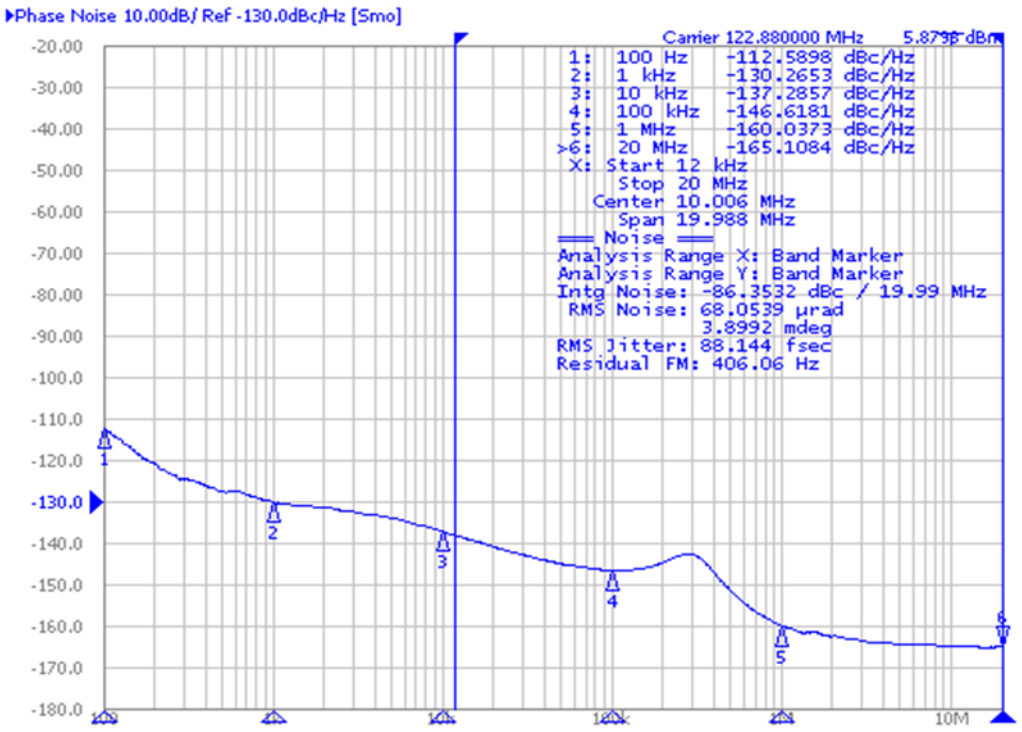

Figure 52. Output Clock Phase Noise With 3rd Order Pole, CFILT=64pF, and RFILT=4.7K

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Referring to Figure 52, a peaking in the phase noise curve can be seen because the pole is placed close to the PLL1 loop bandwidth. It reduces the phase margin but as can be seen comparting the two curves, steeper noise cutting is achieved with the 3rd order pole which results in improvement of the phase noise at 1-MHz offset from –158.46 dBc/Hz without the additional pole to –160.03 dBc/Hz with an additional pole.

5 Summary

PLL1 and PLL2 in the LMK0461x family of devices are based on the semi-digital architecture with fully integrated loop filters. The semi-digital architecture is very flexible to define the loop bandwidth without the need of external components due to the split proportional and integral controls. The PLL locking is fully analog due to the storage cell concept for the integral control. To ease the design, TICSpro software can be downloaded from the TI website. It comes with PLL1 and PLL2 loop filter tools with the transfer function plotting option. It helps to understand the PLL loop response for different programming options available to shape the PLL response. Also the PLLs can be automatically programmed by entering the desired bandwidth.

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