Application Report
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Multi-Clock Synchronization

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ABSTRACT

Synchronization of clocks sourced from a single device is often supported directly by the integrated circuit (IC) producing the clocks. Synchronization of multiple clocking ICs or synchronization of a clock input to various clock outputs may require additional signal timing requirements or frequency planning.

In a system with multiple clock frequencies created by dividers and phase locked loops (PLLs), there is a low frequency clock rate with the timing information necessary to synchronize all clocks. A low frequency clock or DC signal carries with it information about the moment of a synchronization request. This lowest frequency clock may be a reset signal to a divider or a clock frequency used for 0-delay feedback in a PLL. JESD204B uses a SYSREF clock, which is a low frequency synchronization signal by which the local multi-frame clock (LMFC) on JESD204B devices, such as data converters and logic devices, can be reset and synchronized to allow determinism within the period of the LMFC.

This application note discusses methods and requirements for synchronizing multiple devices by either a divider reset, 0-delay, or a combination of both of these methods.

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1 Definitions and acronyms

SYNC — A synchronization signal to hold a divider in reset.

SYSREF — In JESD204B subclass 1 systems, SYSREF is the signal in which the rising edge marks the device clock rising edge, which resets the local multi-frame clock (LMFC), and possibly other dividers in a JESD204B device, provided that the SYSREF is still high when the device clock rising edge occurs.

ZDM — Zero delay mode (or 0-Delay mode). A mode of operation of a PLL where an output divider is included in the PLL feedback path to lock phase of divider output with reference.

GCD — The greatest common divisor of two or more numbers is defined as the largest number which can divide into all the other numbers without a remainder. Traditionally an operation on integers, this also applies to non-integers. For example the GCD of 122.88 MHz and 19.2 MHz is 3.84 MHz. Checking this answer shows that 122.88 MHz / 3.84 MHz = 32 and 19.2 MHz / 3.84 MHz = 5.

PLL — Phase Lock Loop.

JESD204B — JEDEC standard which defines a method for synchronization of data between data converters and logic devices. JESD204B introduces device subclass 1 for deterministic latency. JESD204C increases data rates and adds 64B/66B and 64B/80B as options for encoding in the data link layer. JESD204B supports only 8B/10B encoding. This application note references JESD204B but applies equally to JESD204C.

2 Divider Phase Uncertainty

An issue with dividers occurs when a clock is divided to a lower frequency. The division introduces phase uncertainty, as illustrated in Figure 2. A divider of value D has an output clock with one of D possible phases with respect to the input clock. This phase uncertainty is caused when dividers start dividing the reference input frequency at different edges, or when the initial state of the dividers may have a different starting values at power up.

Figure 1. Clock Divider Block Diagram

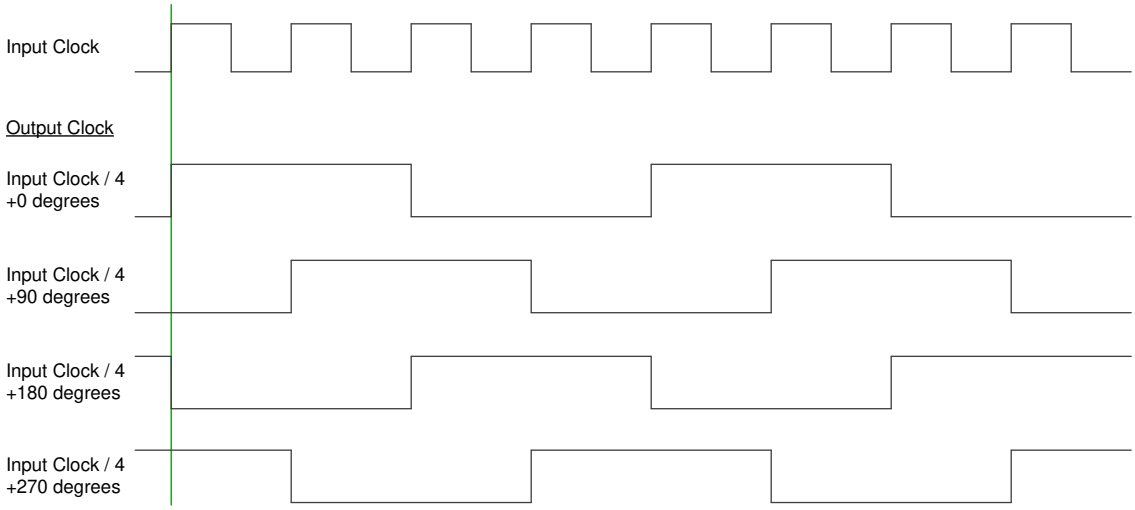

Figure 2. Timing Plot for Phase Uncertainty of a Divider

2.1 Divider Reset Synchronization

A solution to non-deterministic phase is to reset the dividers to a common starting value. To do this, a synchronization signal must reset the dividers while meeting a setup and hold time to the input clock. As the input clock frequency increases, the valid window for the reset signal becomes small, and adjusting the timing of the reset signal relative to the input clock to meet the setup and hold times may be difficult.

JESD204B subclass 1 achieves synchronization of dividers using a SYSREF clock, or SYSREF clock pulse. The SYSREF clock pulse resets dividers internal to the data converters and logic devices to align the LMFC (local multi-frame clock) deterministically between all devices. Because there may be several dividers in series, multiple SYSREF pulses may be required to fully synchronize the system. In a JESD204B system with different LMFCs, it is possible to use a SYSREF frequency, the GCD of all LMFCs, to produce a SYSREF clock valid for all devices. The SYSREF frequency is required to be an integer multiple of the LMFC period.

3 PLL Phase Uncertainty

An issue with PLLs and clock synchronization is they typically also contain dividers. An analog PLL is illustrated in Figure 3. The PLL forces the outputs of the R divider and N divider to a fixed phase alignment. When the phase between the R divider output and N divider output is fixed and no longer changing, frequency lock is achieved. However, the forward division of the reference frequency by the reference divider R may introduce phase uncertainty between the reference input clock and VCO output clock.

Phase certainty or a deterministic phase relationship from reference input clock to the VCO output clock can be achieved with the R divider equal to one. The N divider behaves as a multiplier to the reference frequency, so there is always a corresponding output clock edge for every input clock edge. Determinism of an input clock edge to an output clock edge is therefore achieved. It is not strictly required that R = 1 to have deterministic phase between reference input and VCO output. The frequency of the VCO = Reference Frequency * (N / R). Anytime the fraction N / R reduces to a lowest terms fraction of N' / R' such that R' = 1, then deterministic phase from input to VCO occurs. If the reduced R' value is still greater than one, then only every R'th reference clock edge aligns with a VCO clock edge.

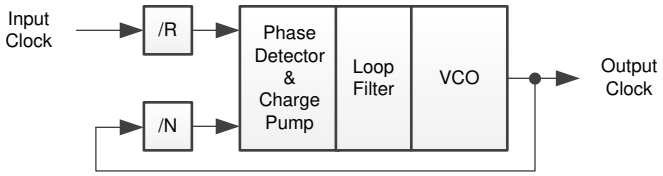

Figure 3. Basic PLL Block Diagram

NOTE: The mathematical maximum phase detector frequency for an integer PLL is the GCD of the reference frequency and the VCO frequency.

3.1 Example 1: All Reference Clocks have Deterministic Phase Alignment to VCO

Given the following conditions for system use case 1A:

- Reference frequency = 40 MHz
- VCO frequency = 160 MHz
- Every reference clock edge has a corresponding VCO clock edge

To lock phase with a 10-MHz phase detector frequency with the given inputs, R = 4 and N = 16. Because N / R = 16 / 4 and reduces to 4 / 1, the reference always has a VCO clock in phase with it. While instantaneously it is possible to have one of four different phases ® = 4), the PLL drives the output of the feedback divider to phase lock with the output of the reference divider.

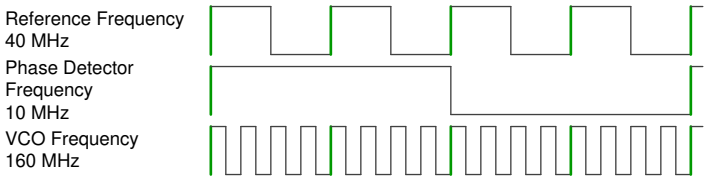

Figure 4. Timing Plot for Deterministic PLL Case

NOTE: The ability for the PLL to drive the phase of the output of the R and N dividers to a fixed relationship is how zero delay mode (ZDM) can synchronize output clocks with dividers. ZDM includes an output divider in the feedback path so the divider output is synchronized to the input clock.

3.2 Example 2: Reference Clock with Non-Deterministic Phase Alignment to VCO

Given the following conditions for system use case 2A:

- Reference frequency = 60 MHz
- VCO frequency = 160 MHz
- Every R'th reference clock edge has a corresponding VCO clock edge.

To lock phase with a 10-MHz phase detector frequency, R = 6 and N = 16. Because N / R = 16 / 6 reduces to 8 / 3, therefore R' = 3 and the reference has one of three different phase relationships to the VCO clock. This configuration is non-deterministic.

Because the GCD of 60 MHz and 160 MHz is 20 MHz, the highest phase detector useable for an integer PLL is 20 MHz. With a 20-MHz phase detector frequency, the N / R fraction would already have been in lowest terms and non-determinism would still exist.

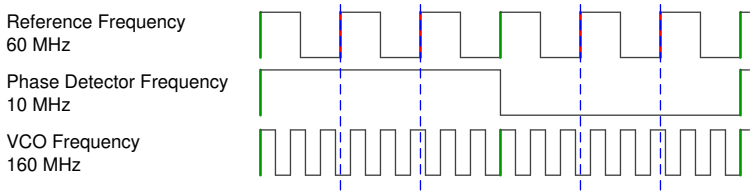

Figure 5. Timing Plot for Non-Deterministic PLL Case

To summarize, the requirement for the reference frequency (input clock) of a PLL to have a deterministic phase relationship to the VCO frequency (output clock) is that the GCD of the reference frequency and the VCO frequency must equal the reference frequency. In the case of non-determinism, the number of possible phase relationships between the reference frequency and VCO is the reference frequency / GCD (reference frequency, VCO frequency).

If the least terms fraction of N / R results in an R' value greater than one, it is still possible to deterministically synchronize the PLL if the R divider of the PLL supports synchronization. While the input clock to output clock does not always align, the input clock and output clock always has the same phase relationship with respect to the synchronization signal, which allows multiple PLLs in parallel to have their output clocks phase aligned.

NOTE: Devices including but not limited to LMK04832 and LMX2594 support synchronization of PLL R dividers.

NOTE: At the falling edge of the "Phase Detector Frequency" waveform in Figure 5, the reference clock and the VCO clock share common rising edges, because the GCD(60, 160) = 20 MHz. With GCD of 20 MHz, the clock edges align at a rate of 20 MHz. A phase detector as high as 20 MHz can be used to lock the 60-MHz reference to the 160-MHz VCO.

4 Zero Delay Mode Synchronization

Clocking ICs typically integrate a PLL and a clock distribution block with division. Figure 6 illustrates a PLL with two outputs, each output with its own output clock divider.

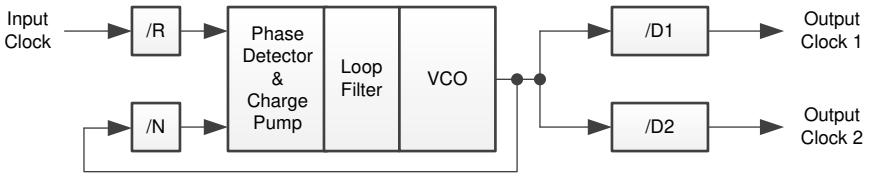

Figure 6. PLL Block Diagram with Clock Distribution

Most clock generators can synchronize the phase of the dividers D1 and D2 using the synchronization by divider reset technique described previously. Many clocking devices have digital or analog delays, which let the user specify a fixed delay between the clock distribution dividers. For many clock generation applications, the alignment of the phases of each individual output is sufficient.

If phase determinism between reference input and clock output is required, the zero delay mode (ZDM) method achieve this is by including the divided clock output in the feedback path from VCO to phase detector. This eliminates the many possible phases of the clock output divider relative to the reference by “disciplining” the clock output phase to the reference phase through the phase detector. When the output clock divider is not in the feedback path, the output clock divider introduces phase uncertainty between the reference input and output with phases spaced at the period of the VCO frequency.

Figure 7 illustrates the output of divider D2 in the feedback path with PLL N divider to the phase detector. Only one output must be fed back to the phase detector because all the other outputs can share the phase determinism by synchronization with the D2 divider.

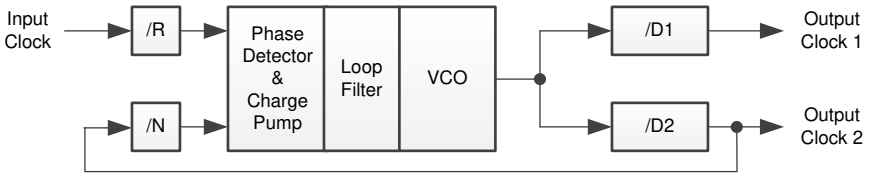

Figure 7. PLL Block Diagram with Clock Distribution and ZDM

This feedback can assure deterministic phase between input and output clock, but it does not alone assure a true “zero delay” from input waveform to output waveform. To achieve a delay of zero seconds from rising edge of input clock to rising edge of output clock, use delays on the PLL R and N paths or on the feedback output or non-feedback outputs. This may result in the feedback clock having a different phase than the other output clocks if adjustment is done in the clock output.

When using ZDM and including an output clock divider in the feedback loop, the VCO frequency equation also includes the output clock divider, for Figure 7 VCO frequency = reference frequency * (N * D2) / R.

4.1 ZDM Rules for Determinism

Select the input clock frequency and the feedback clock frequency to ensure ZDM results in deterministic clock phase. For a clock output to have deterministic phase to the clock input, it must meet the following two requirements:

4.1.1 First Rule, the GCD Between Input and Output Frequency must Equal Input Frequency

In the case of multiple output frequencies, calculate the GCD of all output frequencies and use this for the clock output frequency in the equation:

GCD(input clock frequency, output clock frequency) == input clock frequency.

If the output clock frequency is less than the input clock frequency, then a lower clock input frequency must be presented to ensure deterministic phase. Otherwise there is an unsynchronized divide between the input and the output.

If the output clock frequency is greater than the clock input frequency, but the result of the GCD of clock input and output frequency is still less than clock input frequency, the frequencies are poorly related and there is an unsynchronized divide between them. Change output frequencies to eliminate the poor relationship to the input or reduce the input clock frequency.

NOTE: Reducing the input frequency of a PLL may reduce the phase detector frequency of the PLL, which could reduce the in-band performance of the PLL. For PLLs with narrow loop bandwidths as commonly designed for PLL1 of the LMK0482x and LMK04832, reduced in-band PLL performance is of little concern because these PLLs are operating in a jitter cleaning mode.

4.1.2 Second Rule, Lowest Output Frequency Requiring Determinism used for ZDM Feedback

The feedback frequency of a clocking device with multiple clock output frequencies all requiring deterministic phase with the input shall be the lowest frequency.

4.2 ZDM Examples

The following are three cases using ZDM to achieve deterministic phase between input and output of a clocking device. Only the first and third case achieves zero delay without modification. The first two cases reuse the examples from the previous PLL section. The third case highlights complications which can occur when more than one output frequency must have phase determinism with the reference clock.

4.2.1 Case 1: ZDM Aligning 40-MHz Reference with 40-MHz Clock Output

Given the following conditions for system use case 1B, which are the same as system use case 1A but with an output divider:

- Reference frequency = 40 MHz
- VCO frequency = 160 MHz
- Output frequency = 40 MHz

It is possible to achieve deterministic phase between the 40-MHz reference input and 40-MHz clock output.

Setting PLL R = 4 and using a total PLL feedback divide value of 16 configures the PLL to lock phase at a 10-MHz phase detector frequency. Setting the output divider = 4 configures the device to divide 160-MHz VCO to a 40-MHz output clock frequency. Because this 40-MHz clock frequency drives the PLL N divider in ZDM, the PLL N divider must be programmed to "total PLL feedback divide value" / "output divide value." Thus, PLL N equals 4 which is 16 / 4. The total feedback divide is still 16 as in system use case 1A, Section 3.1, but the divide-by-16 is distributed between the clock divider and the PLL N divider.

Figure 8 illustrates the waveforms produced in this example. The reference frequency, phase detector frequency, and VCO frequency are as in Section 3.1. The clock output frequency has been added and upon lock is shown to have matching phase with the reference frequency. The PLL N = /4 does produce four possible phases of output from the PLL N divider in combination with 4 possible phases of output from the clock output divider, but no matter which edge occurs, the PLL drives the phase error to a deterministic minimum value to phase lock the other possibilities to all have the same phase as the waveform "Output of PLL N: #1" shown in Figure 8, which is phase aligned (by the PLL) to the "10-MHz Phase Detector Frequency" waveform above.

If ZDM was not used, the bottom of Figure 8 illustrates 3 other possible phase relationships the output clock could have to the input clock. Any number of possible phase relationships greater than one results in phase uncertainty from input to output.

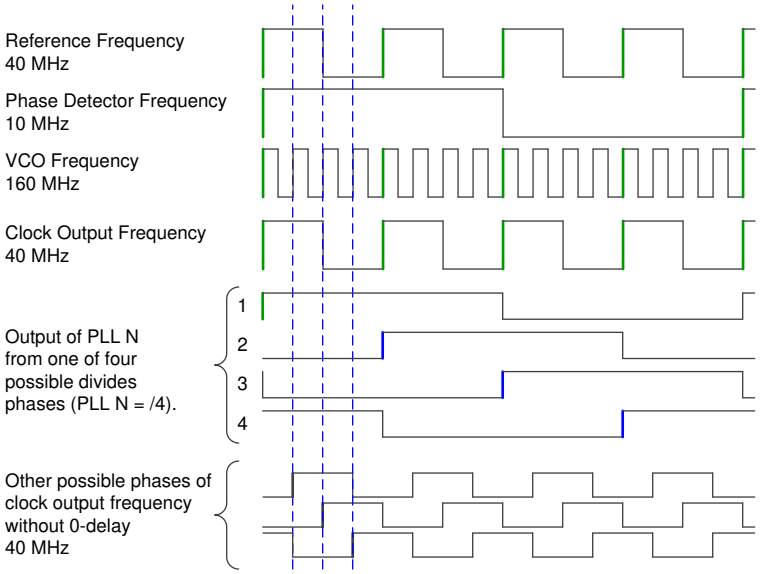

Figure 8. Timing Plot for ZDM with Phase determinism

4.2.2 Case 2: ZDM Aligning 60-MHz Reference with 40-MHz Clock Output

Given the following conditions for system use case 2B, which are the same as system use case 2A but with an output divider:

- Reference frequency = 60 MHz
- VCO frequency = 160 MHz
- Output frequency = 40 MHz

It is possible for every R'th 60-MHz reference clock edge to have a corresponding 40-MHz clock output edge.

Setting PLL R = 6 and using a total PLL feedback divide value of 16 configures the PLL to lock phase at a 10-MHz phase detector frequency. Setting the output divider = 4 configures the device to divide the 160-MHz VCO to a 40-MHz output clock frequency. Because this 40-MHz clock frequency drives the PLL N divider in ZDM, the PLL N divider must be programmed to "total PLL feedback divide value" / "output divide value." Thus, PLL N equals 4 which is 16 / 4. The total feedback divide is still 16 as in system use case 2A, Section 3.2, but the divide-by-16 is distributed between the clock divider and the PLL N divider. Reducing 16 / 6 to a least terms fraction results in N' / R' = 8 / 3, where R' = 3 indicates the number of possible phase relationships to the reference input clock. Any number of possible phase relationships greater than one results in phase uncertainty from input to output. However, if multiple PLLs are used in parallel, a divider reset to all R dividers would result in the deterministic phase between output clocks of the different PLLs.

Figure 9 illustrates the waveforms consistent with this example. The reference frequency, phase detector frequency, and VCO frequency are as before in system use case 2A, Section 3.2. However the clock output frequency has been added and has matching phase with the reference frequency. The PLL N / 4 does produce four possible phase of output from the PLL N divider, but no matter which edge occurs, the PLL phase locks the other possibilities to have the same phase. Refer to Figure 8, which illustrates this in more detail. Finally, if ZDM was not used, the bottom of Figure 9 illustrates the other three possible phase relationships the output clock could have to the input clock, making a total of four possible phase relationships. Any number of possible phase relationships greater than one results in phase uncertainty from input to output.

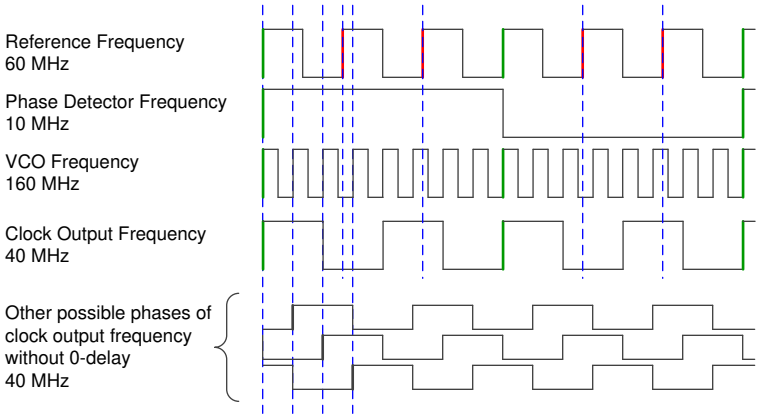

Figure 9. Timing Plot for ZDM with Least Terms R' > 1

4.2.2.1 Modification for Phase Certainty

If phase determinism from input to output is required, change the reference frequency or output frequencies so the two rules for ZDM determinism are true. Another option may be to synchronize the R divider of the PLL to allow multiple parallel PLLs to produce synchronized outputs.

4.2.3 Case 3: ZDM Aligning a Reference Frequency to Two Clock Output Frequencies

Given the following conditions for system use case 3:

- 25-MHz reference frequency
- 100-MHz and 125-MHz output frequencies
- 500-MHz VCO

It is possible to achieve deterministic phase between the 25-MHz reference input and the 100-MHz and 125-MHz clock outputs.

When multiple outputs must have deterministic phase with the input, first find the GCD of the output frequencies for which deterministic phase must be achieved, in this case GCD (100 MHz, 125 MHz) = 25 MHz. Thus the highest frequency that may be used for ZDM feedback is 25 MHz. Because the GCD of the reference frequency of 25 MHz and the feedback frequency of 25 MHz is also 25 MHz, the phase detector may be programmed to 25 MHz.

Because neither output clock is 25 MHz, a 3rd output clock must be created at 25 MHz for ZDM feedback.

Using a 500-MHz VCO, the clock divider D1 is calculated as /5 for the 100-MHz clock output 1, D2 is /4 for the 125-MHz clock output 2, and D3 is /20 for the 25-MHz feedback clock. To achieve a 25-MHz phase detector frequency using a 25-MHz reference PLL R = 1. The Total PLL N = 20, which is 500-MHz VCO / 25-MHz phase detector. However, because a 25-MHz clock is generated and the phase detector frequency is 25 MHz, the Total PLL N divide is implemented in the clock divider and thus PLL N = 1.

Figure 10 illustrates the waveforms produced in this example when all outputs have their dividers synchronized together. Because the Total PLL N divider is 20, there could be 20 different phases of the 25-MHz feedback clock from the 500-MHz VCO before the PLL phase locks. After lock, the waveforms look as shown below.

When an extra frequency is required for alignment, the LMK0482x and LMK04832 require only the clock divider to operate while the output driver may be powered down to reduce power consumption. In many cases, the feedback clock is the same frequency as the lowest output clock. For instance, if 50 MHz and 100 MHz are generated, the GCD (50 MHz, 100 MHz) = 50 MHz and the 50-MHz clock would have been used as the feedback clock, but could have also been used as an output clock. This case illustrates the necessity to add another feedback clock.

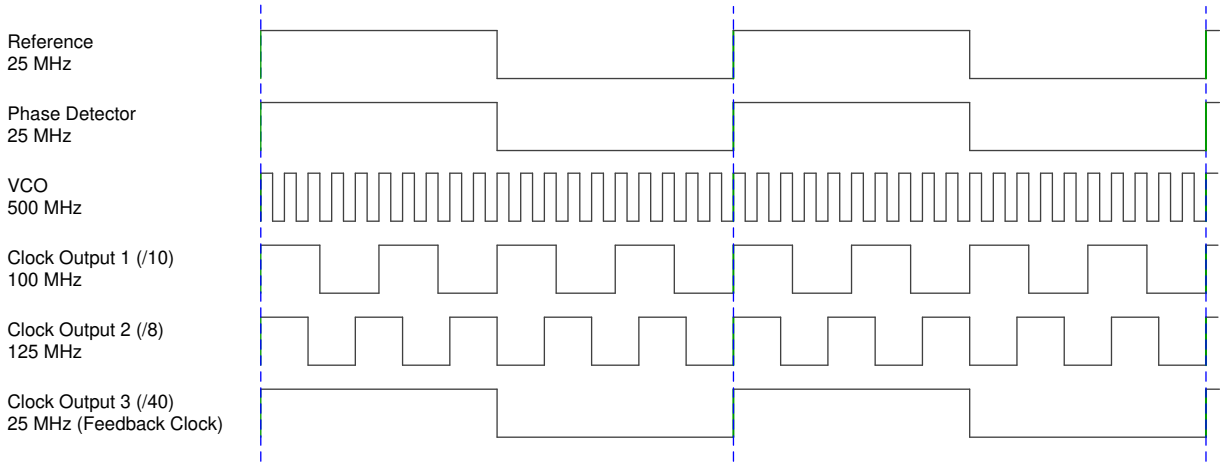

Figure 10. Timing Plot for ZDM with Phase Determinism for Multiple Frequencies

If only the 100-MHz or 125-MHz clock required synchronization, then a 3rd clock would not be needed. Also, phase detector frequencies of higher than 25 MHz would be possible if a higher input clock was also available and only the 100-MHz or 125-MHz clock required synchronization. It is best practice to operate PLLs with phase detector frequencies as high as possible to improve the PLL noise performance.

4.3 ZDM and SYSREF with LMK0482x and LMK04832

One simple method to align SYSREF clocks between multiple devices is to use the SYSREF clock as reference frequency and the SYSREF clock as the ZDM feedback clock. Using SYSREF as a reference clock or for ZDM feedback may reduce the performance of the PLL, because SYSREF frequencies are typically low. In the dual loop LMK0482x and LMK04832 PLLs, this ZDM method can be used while retaining high performance due to the dual loop architecture. PLL1 may receive the low frequency feedback clock of SYSREF while PLL2 receives a higher frequency reference from the selected VCXO frequency.

5 Synchronization using ZDM and Divider Reset

The LMK0482x and LMK04832 SYSREF divider clocks a D flip-flop that accepts an input from CLKin0 or the SYNC pin with the proper mux settings. Refer to Figure 11. The output of this D flip-flop can be selected through the re-clocked mode of the SYSREF_MUX to drive the SYNC/SYSREF distribution path. When the reference input to the LMK is the same frequency as the output of the SYSREF divider which clocks D flip-flop, and the PLL is using a ZDM feedback clock at the same frequency as the output of the SYSREF divider, then a CLKin0 or SYNC signal meeting setup and hold times to the reference input can be used to perform (1) a deterministic divider reset and/or (2) re-clock SYSREF clock onto the SYSREF outputs of the LMK.

Figure 11 shows CLKin0 being re-clocked by the SYSREF divider. It also shows the SYSREF divider configured as the feedback clock, which is not required but the typical use case for this mode of operation. There are two benefits of the SYSREF re-clocking configuration:

First, it is possible to reset clock dividers in the LMK from an external signal while meeting the setup and hold time to the relatively low frequency reference versus the high frequency VCO clock. For example, a 250-MHz reference has a period of 4 ns while a 3-GHz VCO has a period of approximately 333 ps. The SYSREF divider and feedback divider (if different than SYSREF divider) should be synchronized together by a local device synchronization at the start-up of the LMK, then have the SYNC input disabled to these dividers. ZDM then causes these dividers to be synchronized with the reference. Then the other clock dividers may be synchronized by an external source attached to CLKin0 or SYNC pin. Typically resetting the clock dividers from an external source is not required for determinism of the output clocks, as determinism of output clocks would normally be achieved through the ZDM. However, as illustrated in Section 4.2.3, the feedback frequency required for synchronization may be lower than the used output clock frequencies. Using divider synchronization eliminates the need for a lower ZDM feedback frequency *or a lower input frequency*.

Second, it is possible to operate in a SYSREF or SYNC repeating mode. If multiple LMK devices accept a common reference to a PLL and a SYSREF clock to CLKin0 or SYNC, the LMK04828 re-clocks this SYSREF input to the output. In addition to the input SYSREF being re-clocked onto the phase domain of the LMK's internal VCO or external clock if in distribution mode, the digital and analog delays on the LMK output path are available to further optimize the SYSREF placement against the paired device clock from the LMK. This method allows multiple LMK devices to output simultaneous SYSREF clock pulses provided the SYSREF input is re-clocked by the same SYSREF divider edge at the D flip-flop. Because the SYSREF divider is used for the re-clocking operation at the reference frequency, an upstream device provides the SYSREF pulses or continuous frequency, which is fanned out to all downstream devices operating in this SYSREF repeating mode.

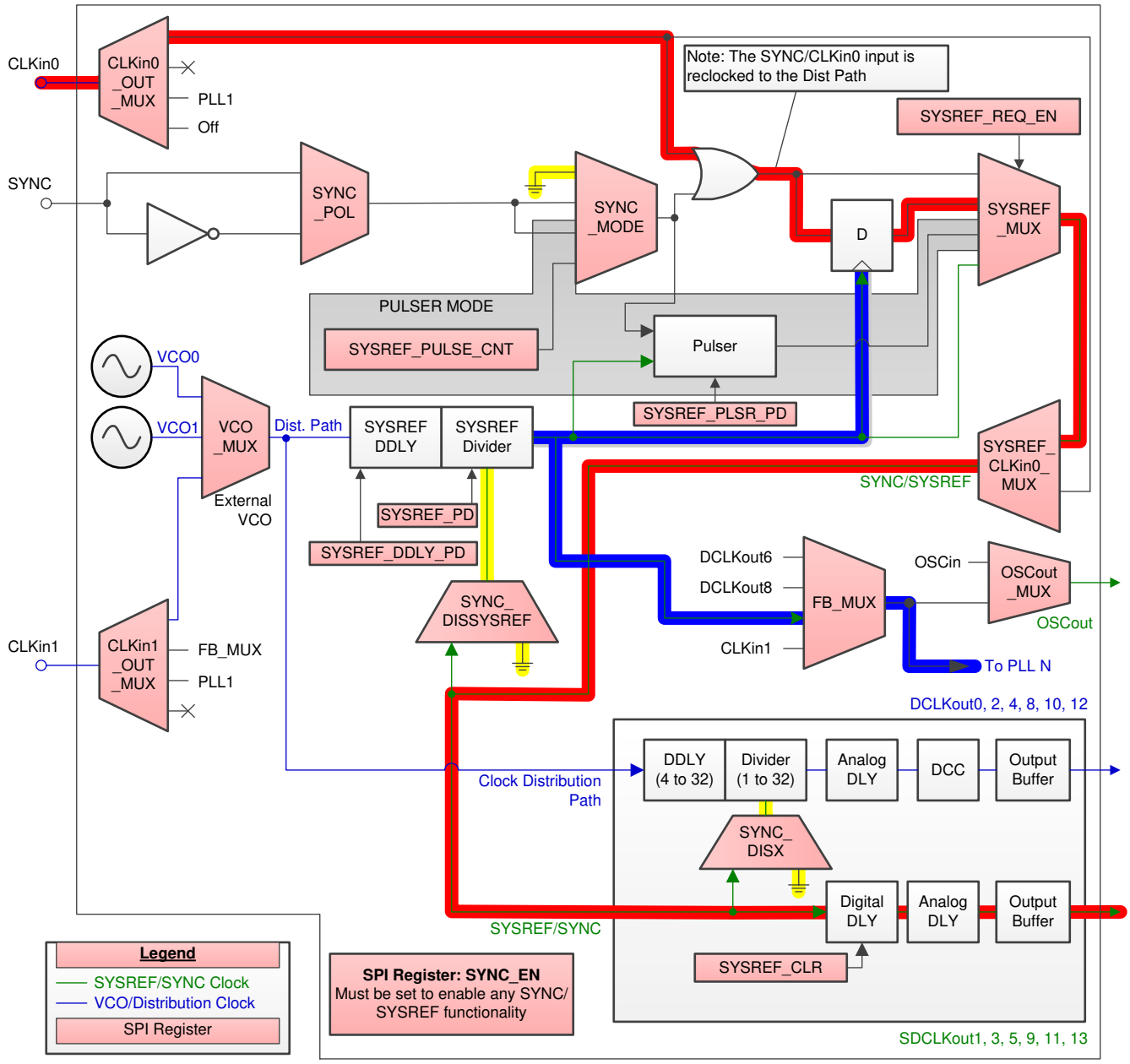

Figure 11. Functional Block Diagram of LMK0482x Configured to Re-clock CLKin0 for JESD204B SYSREF

Both LMK0482x and LMK04832 can be used as illustrated in Figure 11.

In all cases, setup and hold time of the CLKin0 or SYNC pin to the reference of the PLL must be met. Because CLKin0 is a high performance clock input path, TI recommends using CLKin0 over SYNC as setup and hold times are larger.

NOTE: On LMK0482x and LMK04832, it is possible to configure the device to cause the SYSREF divider to reset itself. If this occurs, the output of the SYSREF will not be well behaved. Especially when SYSREF is operating continuously, disable the SYNC to the clock output dividers or the clock outputs will not be well behaved. Be aware of and use the SYNC_DISSYSREF and SYNC_DIS# for each output to disable reset of the SYSREF divider and clock dividers as needed.

6 Conclusion

The primary reason for synchronization of multiple clocks is to fan-out large clocking trees which have deterministic phase relationships to one another. For example, deterministic phase between clocks is useful in phased array antenna systems or in JESD204B systems which distribute a SYSREF to multiple data converters or logic devices.

This application note has discussed achieving phase determinism from the input to output of a clocking device by divider reset, zero delay mode (ZDM), and a combination of ZDM and divider reset. Each method has advantages and disadvantages listed in Table 1.

Table 1. Synchronization Methods Pros and Cons

Synchronization method	Pro	Con
Divider reset Section 2	• All dividers synchronize to a single event or series of events. From the moment of divider reset, the phase of all output clocks is known.	• It can be hard or impossible to meet the setup and hold times to high frequency signals, such as multi-gigahertz VCOs.
Zero delay mode Section 4	• No timing requirements to align periodic clock outputs. • The PLL automatically aligns the phase of input and output clocks.	• Input and output frequencies must be chosen according to ZDM rules for determinism. – Some cases require divider reset of PLL R divider. • If a pulsed SYSREF output is to occur at the same moment across multiple clocking devices for reasons beyond JESD204B synchronization, setup and hold times must be met for requesting SYSREF pulses. – JESD204B does not require SYSREF to be output at the same moment to align the LMFC. • A low input frequency to the PLL may be required when using ZDM to synchronize the SYSREF frequency. Use dual loop mode, which requires external an VCXO on LMK0482x and LMK04832 to retain high performance.
Zero Delay Mode + Re-clocked divider reset or SYSREF Section 5	• ZDM with re-clocked divider reset reduces the setup and hold timing requirements external signals must meet for divider reset. • ZDM with re-clocked SYSREF allows an external SYSREF to be re-clocked onto the VCO phase domain for distribution to a target JESD204B device.	• JESD204B SYSREF generation requires an upstream device to produce the SYSREF clock frequency. This may be another LMK0482x or LMK04832.

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