LMK6x High-Performance BAW Oscillator

1 Features

- Differential and single-ended output, any frequency within the given range can be supported:
  - LMK6P: LVPECL output, 1 – 400 MHz
  - LMK6D: LVDS output, 1 – 400 MHz
  - LMK6H: HCSL output, 1 – 400 MHz
  - LMK6C: LVCMOS output, 1 – 200 MHz
- Ultra-low jitter:
  - LMK6P/LMK6D/LMK6H: 100-fs RMS jitter, Fout ≥ 100 MHz
  - LMK6C: 300-fs RMS jitter, Fout ≥ 25 MHz
  - LMK6H: PCIe Gen 1-6 compliant
- ±25-ppm total frequency stability inclusive of all factors and 10 year aging
- Smallest industry standard package: 2.50 mm × 2.00 mm (DLF)
  - 3.20 mm × 2.50 mm (DLE) also available
- Support extended industrial temperature grade:
  - LMK6P/LMK6D/LMK6H: –40°C to 85°C
  - LMK6C: –40°C to 105°C
- Integrated LDO for robust supply noise immunity
- < 5-ms start-up time
- Fixed-frequency devices, programmed at the factory. Short leadtime on new frequencies for sampling. Contact TI representative.

2 Applications

- High-performance crystal oscillator replacement
- 56G/112G PAM4 clocking
- 400G/800G Optical Transport Network and Coherent Optics
- PCIe Gen 1 to Gen 6 clock generation
- Network equipment, switches, routers, line cards, SAN, data centers and baseband units (BBU)
- Test and measurement
- Medical imaging
- Professional audio/video
- FPGA and ASIC clocking

3 Description

Texas Instruments' Bulk-Acoustic Wave (BAW) is a micro-resonator technology that enables the integration of high-precision and ultra-low jitter clocks directly into packages that contain other circuits. BAW is fully designed and manufactured at TI factories like other silicon-based fabrication processes.

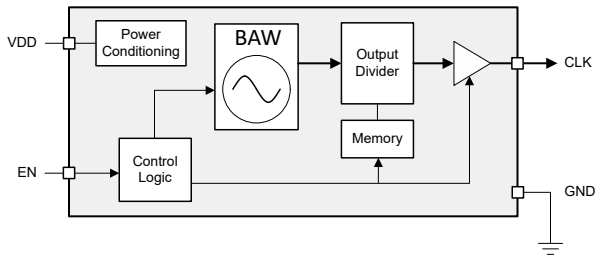
The LMK6x device is a low jitter, fixed-frequency oscillator which incorporates the BAW as the resonator source. With a high-performance fractional frequency divider, the LMK6x is capable of producing any frequency within the specified range providing a single device family for all frequency needs. The device is factory-programmed per specific operation mode, including frequency, voltage, output type, and function pin. Contact a TI representative for additional frequencies or other options.

The high-performance clocking, mechanical stability, flexibility and small package options for this device are designed for reference and core clocks in high-speed SERDES used in Telecommunications, Data and Enterprise Network and Industrial applications.

Packaging Information

PART NUMBER	OUTPUT TYPE	PACKAGE(1)	BODY SIZE (NOM)
LMK6C	LVCMOS	VSON (DLE-4)	3.20 mm × 2.50 mm
LMK6C		VSON (DLF-4)	2.50 mm × 2.00 mm
LMK6P(2), LMK6D(2), LMK6H(2)	LVPECL, LVDS, HCSL	VSON (DLE-6)	3.20 mm × 2.50 mm
LMK6P(2), LMK6D(2), LMK6H(2)		VSON (DLF-6)	2.50 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) Product preview.



LMK6x Simplified Block Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2022) to Revision A (July 2022)	Page
• Added HCSL support (LMK6H) to the data sheet	1
• Added new orderable variants to the data sheet	1

5 Device Comparison

Use Figure 5-1 and Figure 5-2 to understand the device nomenclature of the LMK6x orderable options.

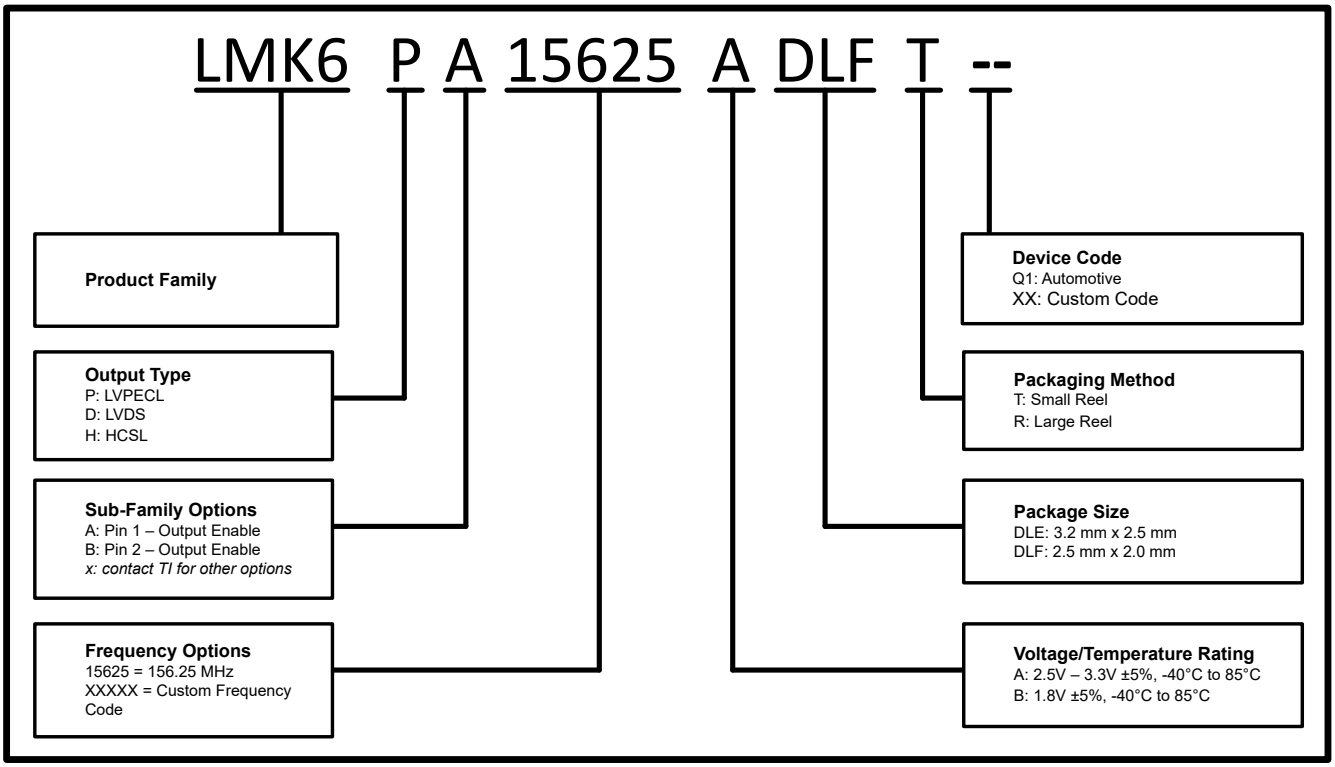

Figure 5-1. Part Number Guide: LMK6P, LMK6D, and LMK6H

Note: Contact a TI representative to pre-order specific devices. Email: ti_osc_customer_requirement@list.ti.com

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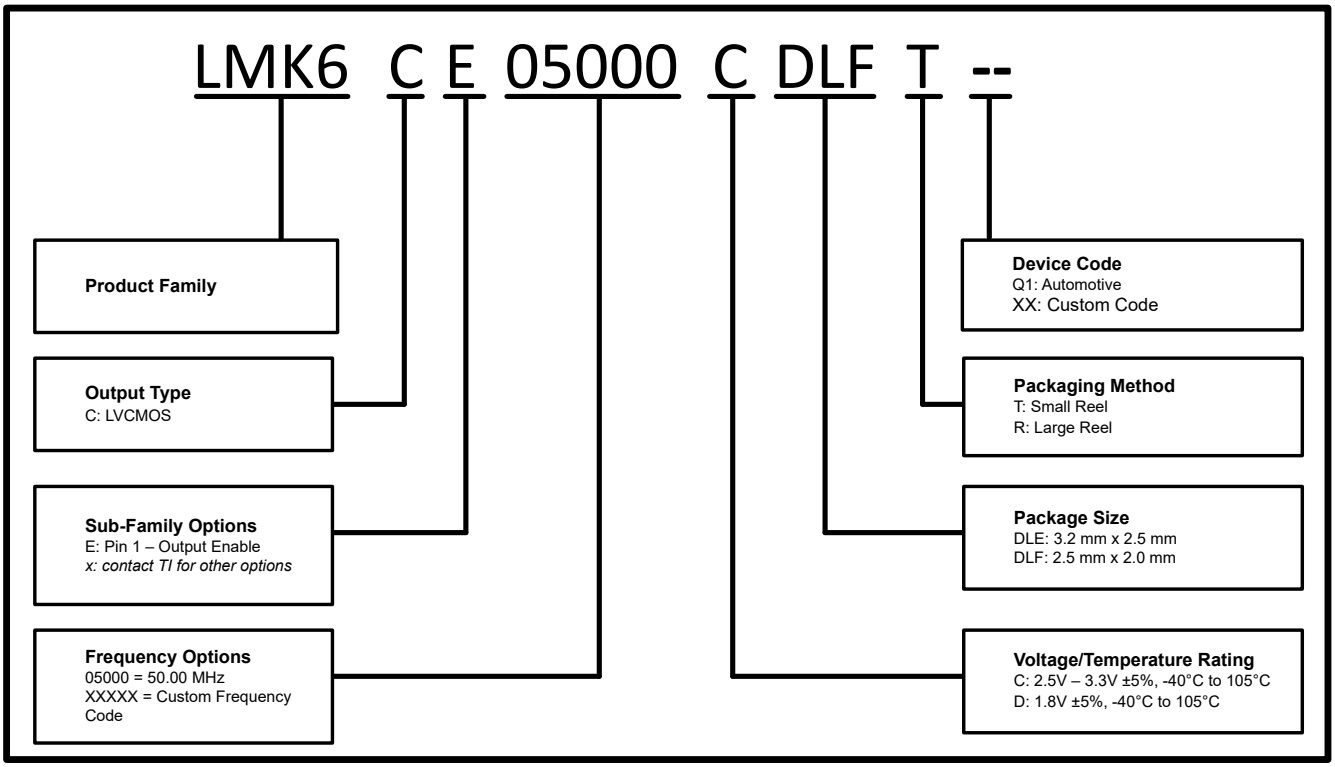

Figure 5-2. Part Number Guide: LMK6C

Note: Contact a TI representative to pre-order specific devices. Email: ti_osc_customer_requirement@list.ti.com

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6 Pin Configuration and Functions

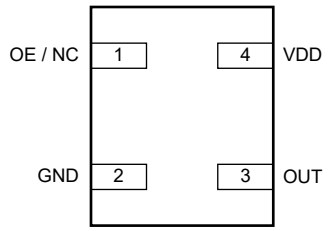

Figure 6-1. LMK6C 4-Pin VSON (Top View)

Table 6-1. LMK6C Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
OE / NC	1	I / NC	Output Enable (OE) pin. Internal pullup resistor. When pulled low, output is tri-stated. Internal pullup resistor > 90 kΩ. A No Connect (NC) option is available and must be left floating, if used.
GND	2	G	Device ground
OUT	3	O	LVCMOS output clock
VDD	4	P	Device power supply

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power, NC = No Connect.

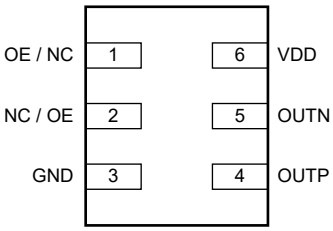

Figure 6-2. LMK6P, LMK6D, or LMK6H 6-Pin VSON (Top View)

Table 6-2. LMK6P, LMK6D, or LMK6H Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
OE / NC	1	I / NC	Output Enable (OE) pin. Internal pullup resistor. When pulled low, output is tri-stated. Internal pullup resistor > 90 kΩ. A No Connect (NC) option is available and must be left floating, if used.
NC / OE	2	NC / I	No Connect (NC). An Output Enable (OE) pin option is available. Internal pullup resistor. When pulled low, output is tri-stated. Internal pullup resistor > 90 kΩ
GND	3	G	Device ground
OUTP	4	O	Positive differential output clock
OUTN	5	O	Negative differential output clock
VDD	6	P	Device power supply

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power, NC = No Connect.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VDD	Device Supply Voltage(2)	–0.3	3.63	V
VDD	Device Supply Voltage(3)	–0.3	1.98	V
EN	Logic Input Voltage	–0.3	VDD + 0.3	V
OUTP, OUTN	Clock Output Voltage(4)	–0.3	VDD + 0.3	V
T_J	Junction Temperature		125	°C
T_{STG}	Storage Temperature		150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) For all devices with Recommended Operating Voltage of 2.5V +/- 5% and 3.3V +/- 5%
(3) For all devices with Recommended Operating Voltage of 1.8V +/- 5%
(4) For all differential outputs. LMK6P, LMK6D, LMK6H.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(3) (1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(3) (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) For Industrial Grade device

7.3 Environmental Compliance

			VALUE	UNIT
	Mechanical Shock Resistance	MIL-STD-883F, Method 2002, Condition A	1500	g
	Mechanical Vibration Resistance	MIL-STD-883F, Method 2007, Condition A	20	g
	Moisture Sensitivity Level	MSL1	NA	

7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Device Supply Voltage(1)	1.71	1.8	1.89	V
VDD	Device Supply Voltage(2)	2.375	2.5	2.625	V
		3.135	3.3	3.465	V
T_A	Ambient temperature(3)	–40		85	°C
T_A	Ambient temperature(4)	–40		105	°C
T_J	Junction temperature			125	°C
t_{RAMP}	VDD power-up ramp time(5) (2)	0.1		100	ms

(1) For all devices with Recommended Operating Voltage of 1.8V +/- 5%
(2) For all devices with Recommended Operating Voltage of 2.5V +/- 5% and 3.3V +/- 5%
(3) For all differential outputs. LMK6P, LMK6D, and LMK6H.
(4) For all single-ended outputs. LMK6C.
(5) For Automotive LVCMOS only

7.5 Thermal Information

THERMAL METRIC[1]		LMK6P/D/H		UNIT
		DLE (VSON)	DLF (VSON)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	101.2	107.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.6	70.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.3	39.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.7	2.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	31.1	39.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.6 Thermal Information

THERMAL METRIC[1]		LMK6C		UNIT
		DLE	DLF	
		4 PINS	4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.8	128.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.2	73.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.5	39.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.8	2.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	42.3	39.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.7 Electrical Characteristics

Over Recommended Operating Conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current Consumption Characteristics						
I_{DD}	Device Power Consumption	LVPECL output, F_{out} ≤ 200 MHz[1]		60	TBD	mA
I_{DD}	Device Power Consumption	LVPECL output, 200 MHz < F_{out} ≤ 400MHz[1]		90	TBD	mA
I_{DD}	Device Power Consumption	LVDS output, F_{out} ≤ 200 MHz[1]		52	TBD	mA
I_{DD}	Device Power Consumption	LVDS output, 200 MHz < F_{out} ≤ 400MHz[1]		80	TBD	mA
I_{DD}	Device Power Consumption	LVCMOS output, F_{out} ≤ 200 MHz, C_L = No Load		50	TBD	mA
I_{DD-PD}	Device Power-Down Current	OE = GND			TBD	mA
LVPECL Output Characteristics						
F_{out}	Output Frequency		1		400	MHz
V_{OD}	Output Voltage Swing (V_{OH} - V_{OL})	AC Load, VDD = 3.3V	550	650	750	mV
V_{OD}	Output Voltage Swing (V_{OH} - V_{OL})	AC Load, VDD = 2.5V	500	600	700	mV
V_{OD}	Output Voltage Swing (V_{OH} - V_{OL})	AC Load, VDD = 1.8V	325	400	450	mV
V_{OD}	Output Voltage Swing (V_{OH} - V_{OL})	DC Load, VDD = 2.5 V/ 3.3V[2]	700	800	900	mV
V_{OD}	Output Voltage Swing (V_{OH} - V_{OL})	DC Load, VDD = 1.8 V[2]	500	600	700	mV
$V_{OD,DIFF}$	Differential Output peak-peak swing			2x|V_{OD}|		V
V_{OS}	Output Common Mode Voltage	VDD = 3.3 V[2]	1.5	1.6	1.7	V
		VDD = 2.5 V[2]	0.825	0.9	0.975	V
V_{OS}	Output Common Mode Voltage	VDD = 1.8 V[2]	0.45	0.5	0.55	V

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Over Recommended Operating Conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R/t_F	Output Rise/Fall Time	20% to 80% of $V_{OD,DIFF}$		120	200	ps
ODC	Output Duty Cycle		45	50	55	%
PN-Floor	Output Phase Noise Floor (f_{OFFSET} > 10 MHz)	Fout = 156.25 MHz		–158		dBc/Hz
LVDS Output Characteristics						
F_{out}	Output Frequency		1		400	MHz
V_{OD}	Output Voltage Swing (V_{OH} - V_{OL})	Under LVDS Load condition	250	350	450	mV
$V_{OD,DIFF}$	Differential Output peak-peak swing			2x|V_{OD}|		V
V_{OS}	Output Common Mode Voltage	VDD = 2.5V/3.3 V	1.025	1.2	1.375	V
V_{OS}	Output Common Mode Voltage	VDD = 1.8 V	0.80	0.9	1.0	V
t_R/t_F	Output Rise/Fall Time	20% to 80% of $V_{OD,DIFF}$		150	250	ps
ODC	Output Duty Cycle		45	50	55	%
PN-Floor	Output Phase Noise Floor (f_{OFFSET} > 10 MHz)	Fout = 156.25 MHz		–158		dBc/Hz
HCSL Output Characteristics						
F_{out}	Output Frequency		1		400	MHz
V_{OL}	Output Low Voltage	VDD = 3.3V	-150	0	150	mV
V_{OH}	Output High Voltage	VDD = 3.3V	660	750	850	mV
V_{OL-ABS}	Absolute Low Voltage Including Undershoot	VDD = 3.3V	-300			mV
V_{OH-ABS}	Absolute High Voltage Including Overshoot	VDD = 3.3V			1.15	V
V_{cross}	Absolute Crossing Point Voltage	VDD = 3.3V, f_{out} = 100 MHz	250		550	mV
ΔV_{cross}	Absolute Crossing Point Voltage	VDD = 3.3V, f_{out} = 100 MHz			140	mV
dV/dt	Out Slew Rate	± 150 mV around center point	2		4	V/ns
ΔdV/dt	Out Slew Rate				20	%
ODC	Output Duty Cycle		45	50	55	%
PN-Floor	Output Phase Noise Floor (f_{OFFSET} > 10 MHz)	Fout = 156.25 MHz		–158		dBc/Hz
LVCMOS Output Characteristics						
F_{out}	Output Frequency		1		200	MHz
V_{OL}	Output Low Voltage	I_{OL} = 3.6mA, VDD = 1.8V			0.36	V
V_{OL}	Output Low Voltage	I_{OL} = 5.0mA, VDD = 2.5V			0.5	V
		I_{OL} = 6.6mA, VDD = 3.3V			0.66	V
V_{OH}	Output High Voltage	I_{OH} = 3.6mA, VDD = 1.8V	1.44			V
V_{OH}	Output High Voltage	I_{OH} = 5.0mA, VDD = 2.5V	2			V
		I_{OH} = 6.6mA, VDD = 3.3V	2.64			V
t_R/t_F	Output Rise/Fall Time	20% to 80% of V_{OH}-V_{OL}, C_L = 2 pF		0.5	1	ns
ODC	Output Duty Cycle		45	50	55	%
PN-Floor	Output Phase Noise Floor (f_{OFFSET} > 10 MHz)	Fout = 50 MHz		–155		dBc/Hz
R_{out}	Output Impedance		40	50	60	Ω
C_L	Maximum capacitive load	Fout > 50 MHz			15	pF
C_L	Maximum capacitive load	Fout < 50 MHz			30	pF
EN Input Characteristics						
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		1.3			V

Over Recommended Operating Conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IL}	Input Low Current	EN = GND			–40	µA
I_{IH}	Input High Current	EN = VDD			40	µA
C_{IN}	Input Capacitance			2		pF
LVPECL, LVDS, and HCSL Frequency Tolerance						
F_T	Total Frequency Stability	Inclusive of: solder shift, initial tolerance, variation over -40℃ to 85℃, variation over rated supply voltage range, and 10 year aging at 25℃.			±25	ppm
LVCMOS Frequency Tolerance						
F_T	Total Frequency Stability	Inclusive of: solder shift, initial tolerance, variation over -40℃ to 105℃, variation over rated supply voltage range, and 10 year aging at 25℃.			±25	ppm
Power-On Characteristics						
t_{START_UP}	Start-up Time	Time elapsed from 0.95 x VDD until output is enabled and output is within specification			5	ms
t_{OE-EN}	Output Enable Time	Time elapsed from OE = V_{IH} until output is enabled and output is within specification, F_{out} > 10 MHz			25	µs
t_{OE-DIS}	Output Disable Time	Time elapsed from OE = V_{IL} until output is disabled, F_{out} > 10 MHz			25	µs
LVPECL - Clock Output Jitter						
R_J	RMS Phase Jitter, Integration BW: 12 kHz - 20 MHz	F_{out} > 100 MHz			125	fs
R_J	RMS Phase Jitter, Integration BW: 12 kHz - 20 MHz	F_{out} = 100 MHz		110	TBD	fs
R_J	RMS Phase Jitter, Integration BW: 12 kHz - 20 MHz	F_{out} = 125 MHz		95	125	fs
R_J	RMS Phase Jitter, Integration BW: 12 kHz - 20 MHz	F_{out} = 156.25 MHz		90	125	fs
$R_{JITT,RMS}$	RMS Period Jitter	F_{out} ≥ 25 MHz		0.7		ps
$R_{JITT,PK}$	Peak-peak Period Jitter	F_{out} ≥ 25 MHz		7		ps
LVDS - Clock Output Jitter						
R_J	RMS Phase Jitter, Integration BW: 12 kHz - 20 MHz	F_{out} > 100 MHz			125	fs
R_J	RMS Phase Jitter, BW: 12 kHz - 20 MHz	F_{out} = 100 MHz		115	TBD	fs
R_J	RMS Phase Jitter, BW: 12 kHz - 20 MHz	F_{out} = 125 MHz		100	125	fs
R_J	RMS Phase Jitter, BW: 12 kHz - 20 MHz	F_{out} = 156.25 MHz		95	125	fs
$R_{JITT,RMS}$	RMS Period Jitter	F_{out} ≥ 25 MHz		0.7		ps
$R_{JITT,PK}$	Peak-peak Period Jitter	F_{out} ≥ 25 MHz		7		ps
HCSL - Clock Output Jitter						
R_J	RMS Phase Jitter, Integration BW: 12 kHz - 20 MHz	F_{out} > 100 MHz			125	fs
R_J	RMS Phase Jitter, Integration BW: 12 kHz - 20 MHz	F_{out} = 100 MHz		110	TBD	fs
R_J	RMS Phase Jitter, Integration BW: 12 kHz - 20 MHz	F_{out} = 125 MHz		95	125	fs
R_J	RMS Phase Jitter, Integration BW: 12 kHz - 20 MHz	F_{out} = 156.25 MHz		90	125	fs
$J_{PCIe1-cc}$	PCIe Gen 1 Common Clock jitter (jitter limit = 86 ps)	F_{out} = 100 MHz			TBD	ps

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Over Recommended Operating Conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$J_{PCIe1-SRNS}$	PCIe Gen 1 SRNS jitter	F_{out} = 100 MHz			TBD	ps
$J_{PCIe2-cc}$	PCIe Gen 2 Common Clock jitter (jitter limit = 3 ps)	F_{out} = 100 MHz			TBD	ps
$J_{PCIe2-SRNS}$	PCIe Gen 2 SRNS jitter	F_{out} = 100 MHz			TBD	ps
$J_{PCIe3-cc}$	PCIe Gen 3 Common Clock jitter (jitter limit = 1 ps)	F_{out} = 100 MHz			TBD	ps
$J_{PCIe3-SRNS}$	PCIe Gen 3 SRNS jitter	F_{out} = 100 MHz			TBD	ps
$J_{PCIe4-cc}$	PCIe Gen 4 Common Clock jitter (jitter limit = 500 fs)	F_{out} = 100 MHz		140	TBD	fs
$J_{PCIe4-SRNS}$	PCIe Gen 4 SRNS jitter	F_{out} = 100 MHz			TBD	fs
$J_{PCIe5-cc}$	PCIe Gen 5 Common Clock jitter (jitter limit = 150 fs)	F_{out} = 100 MHz		45	TBD	fs
$J_{PCIe5-SRNS}$	PCIe Gen 5 SRNS jitter	F_{out} = 100 MHz			TBD	fs
$J_{PCIe6-cc}$	PCIe Gen 6 Common Clock jitter (jitter limit = 100 fs)	F_{out} = 100 MHz			TBD	fs
$J_{PCIe6-SRNS}$	PCIe Gen 6 SRNS jitter	F_{out} = 100 MHz			TBD	fs
LVCMOS - Clock Output Jitter						
R_J	Random Phase Jitter	F_{out} = 24 MHz, Integration BW: 12 kHz - 5 MHz		200		fs
R_J	Random Phase Jitter	F_{out} = 156.25 MHz, Integration BW: 12 kHz - 20 MHz		200	500	fs
$R_{JITT,RMS}$	RMS Period Jitter	F_{out} ≥ 25 MHz		0.7		ps
$R_{JITT,PK}$	Peak-peak Period Jitter	F_{out} ≥ 25 MHz		7		ps

(1) Excluding Load current
(2) DC Load condition

7.8 Timing Diagrams

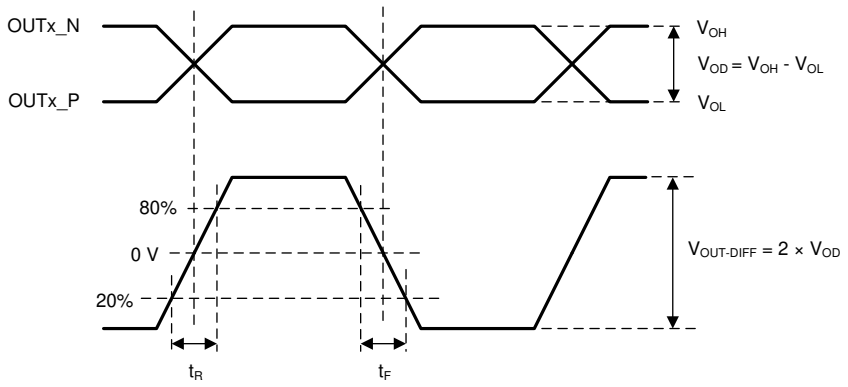

Figure 7-1. Differential Output Voltage and Rise/Fall Time

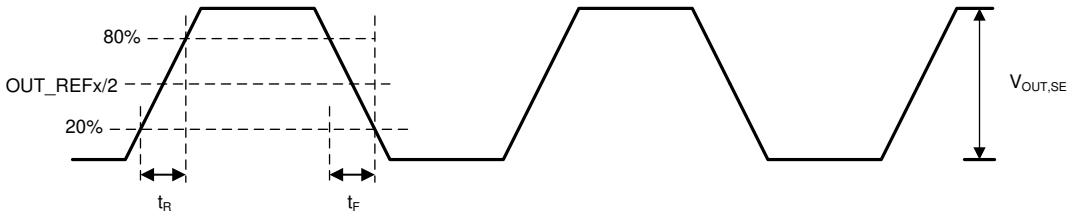

Figure 7-2. Single-Ended Output Voltage and Rise/Fall Time

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8 Parameter Measurement Information

8.1 Device Output Configurations

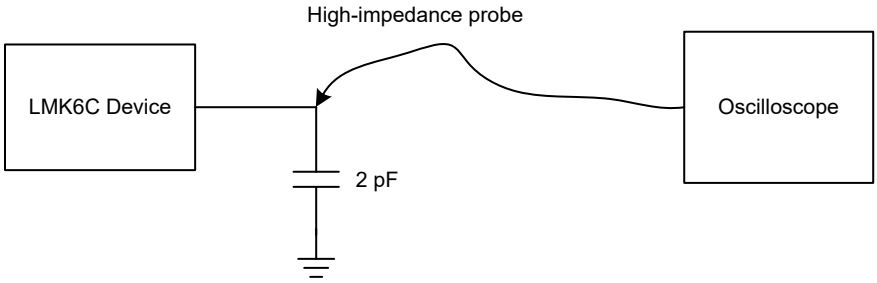


Figure 8-1. LMK6C Output Test Configuration

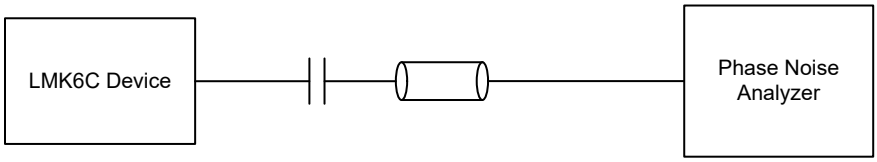


Figure 8-2. LMK6C Output Phase Noise Test Configuration

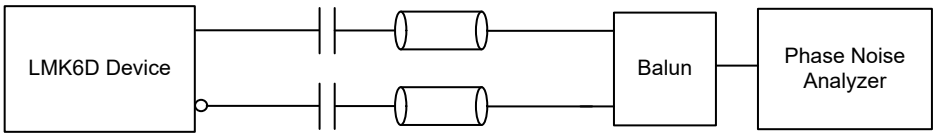


Figure 8-3. LMK6D Output Phase Noise Configuration

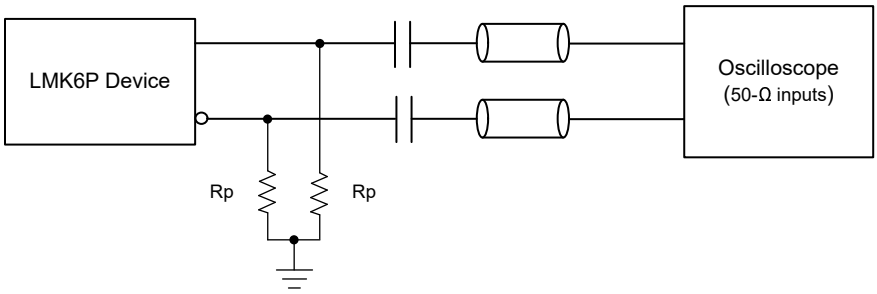


Figure 8-4. LMK6P Output Test Configuration

Table 8-1. LMK6P Output Test Configuration Rp Values

SUPPLY (V)	Rp (Ω)
3.3 V	207.5
2.5 V	112.5
1.8 V	83.3

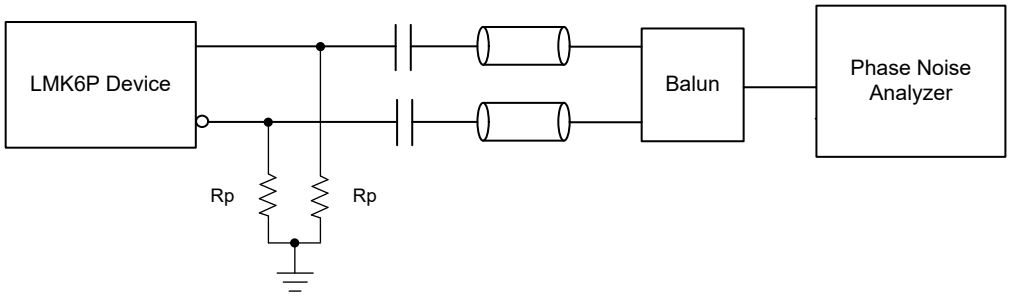


Figure 8-5. LMK6P Output Phase Noise Configuration

Table 8-2. LMK6P Output Phase Noise Configuration Rp Values

SUPPLY (V)	Rp (Ω)
3.3 V	207.5
2.5 V	112.5
1.8 V	83.3

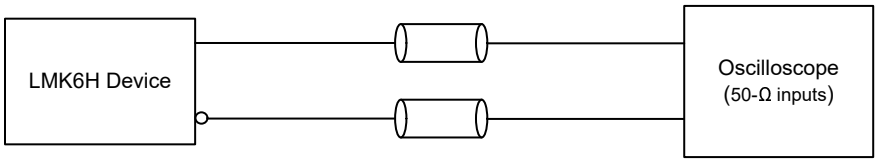


Figure 8-6. LMK6H Output Test Configuration

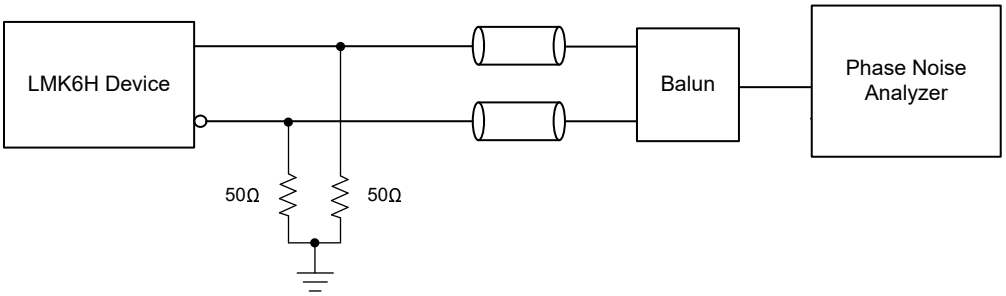


Figure 8-7. LMK6H Output Phas Noise Configuration

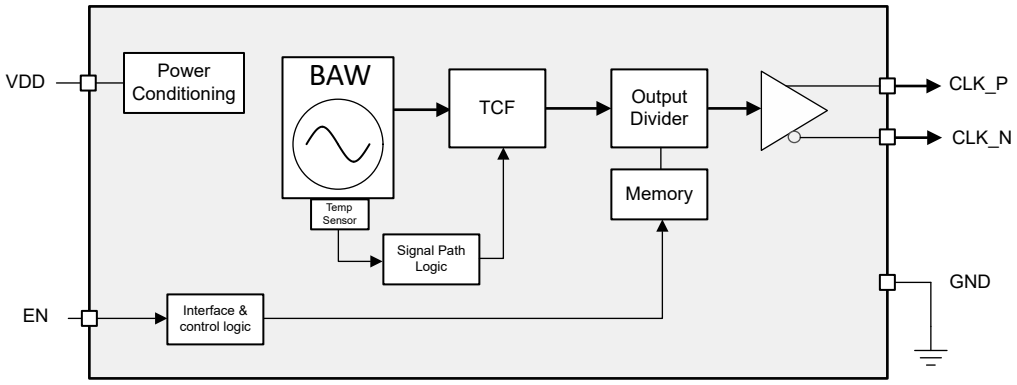
ADVANCE INFORMATION

9 Detailed Description

9.1 Overview

The LMK6x is a fixed-frequency BAW based oscillator that can provide ultra-low jitter both for differential and single-ended output types.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Bulk Acoustic Wave (BAW)

TI's BAW resonator technology uses piezoelectric transduction to generate high-Q resonance at 2.5 GHz. The resonator is defined by the quadrilateral area overlaid by top and bottom electrodes. Alternating high- and low-acoustic impedance layers form acoustic mirrors beneath the resonant body to prevent acoustic energy leakage into the substrate. Furthermore, these acoustic mirrors are also placed on top of the resonator stack to protect the device from contamination and minimize energy leakage into the package materials. This unique dual-Bragg acoustic resonator (DBAR) allows efficient excitation without the need of costly vacuum cavities around the resonator. As a result, TI's BAW resonator is immune to frequency drift caused by adsorption of surface contaminants and can be directly placed in a non-hermetic plastic package with the oscillator IC in small standard oscillator footprints.

9.3.2 Device Block-Level Description

High-Q resonant tank of BAW die is complimented with an ultra-low noise oscillator on a base die, designed in CMOS process node. Temperature variations of oscillation frequency are continuously monitored by a co-located precision temperature sensor. Correction for frequency is done using an advance signal processing algorithm which runs continuously in the background while making use of per part calibration coefficients, stored in NVM, to compensate frequency within ±10 ppm. A very low jitter, low power fractional output divider (FOD) in the frequency correction path allows necessary compensation with minimum impact to the phase jitter while generating a per-programmed output frequency clock. The output driver is capable of providing both single-ended LVCMOS and differential LVPECL, LVDS, and HCSL output formats. Finally, a small power-reset-clock management system consisting of several low noise LDOs and digital controller makes sure noise sensitive modules work with enough isolation while maintaining output clock fidelity.

9.3.3 Function Pin(s)

The function pin is identified as pin 1 on the LMK6C and pin 1 or pin 2, depending on the grade of the device, for the LMK6P, LMK6D, and LMK6H. In addition to output enable, the function pin is also capable of providing a chip disable / standby feature. In this mode, all blocks will be powered down to provide a maximum current consumption savings for a non-operation mode, meaning the output clock is not available. The return to the output clock active time corresponds to the initial start-up time.

The function pin can also be designed to be active high or active low. This allows for compatibility and drop in replacement with hardware that may have terminated to ground. Contact your TI representative to discuss options not listed on Figure 5-1 and Figure 5-2.

9.3.4 Clock Output Interfacing and Termination

These figures show the recommended output interfacing and termination circuits.

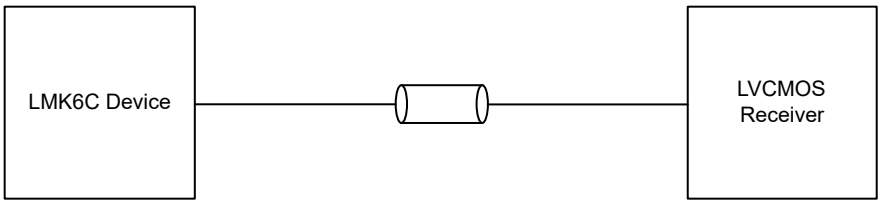


Figure 9-1. LMK6C Output to LVCMOS Receiver

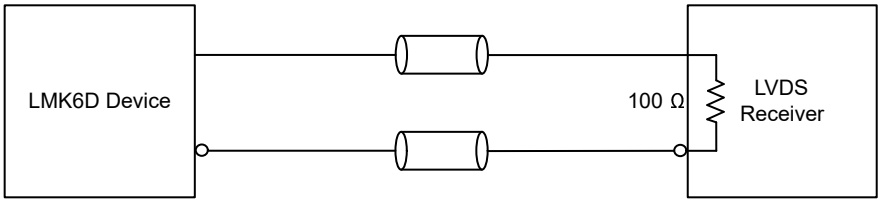


Figure 9-2. LMK6D Output DC-Coupled to LVDS Receiver With Internal Termination/Biasing

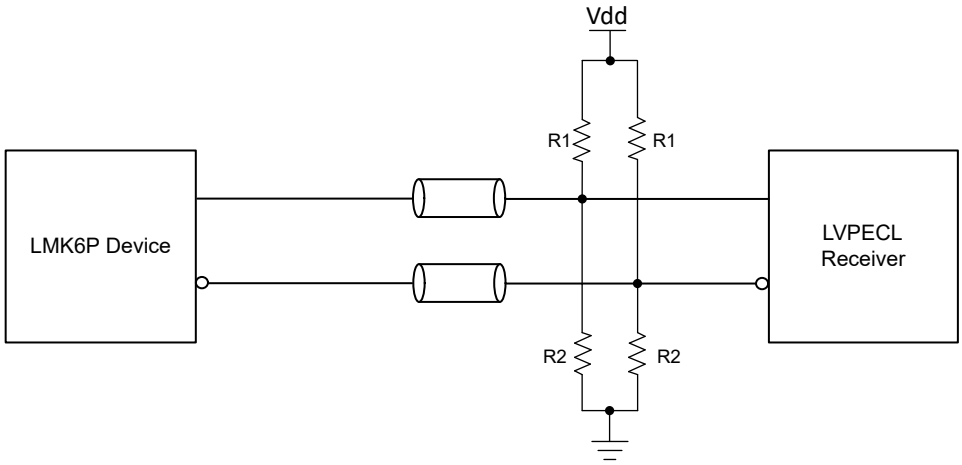


Figure 9-3. LMK6P Output DC-Coupled to LVPECL Receiver With External Termination/Biasing (T-Network)

Table 9-1. LMK6P T-Network DC-Coupled Resistor Values

SUPPLY (V)	R1 (Ω)	R2 (Ω)
3.3	133	82
2.5	250	62.5
1.8	450	56.5

ADVANCE INFORMATION

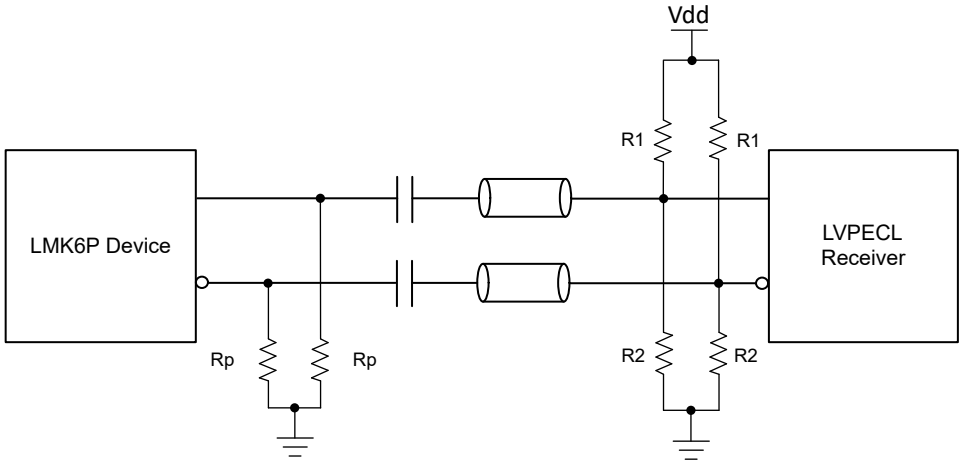


Figure 9-4. LMK6P Output AC-Coupled to LVPECL Receiver With External Termination/Biasing (T-Network)

Table 9-2. LMK6P T-Network AC-Coupled Resistor Values

SUPPLY (V)	Rp (Ω)	R1 (Ω)	R2 (Ω)
3.3	207.5	133	82
2.5	112.5	250	62.5
1.8	83.3	450	56.6

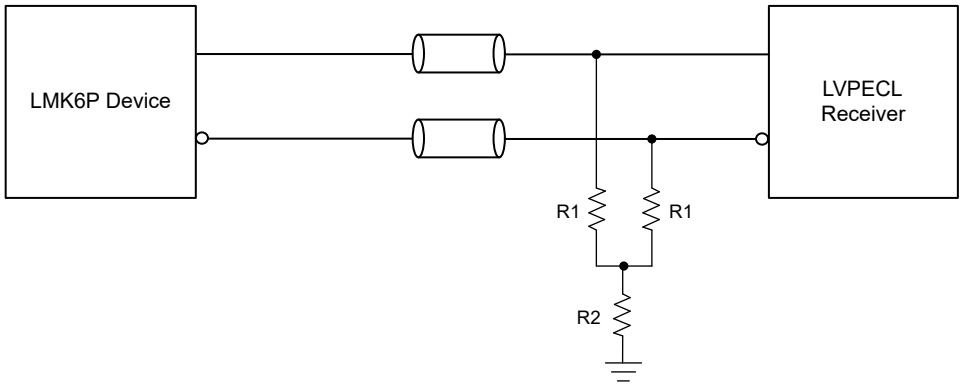


Figure 9-5. LMK6P Output DC-Coupled to LVPECL Receiver With External Termination/Biasing (Y-Network)

Table 9-3. LMK6P Y-Network DC-Coupled Resistor Values

SUPPLY (V)	R1 (Ω)	R2 (Ω)
3.3	50	78.8
2.5	50	31.3
1.8	50	16.7

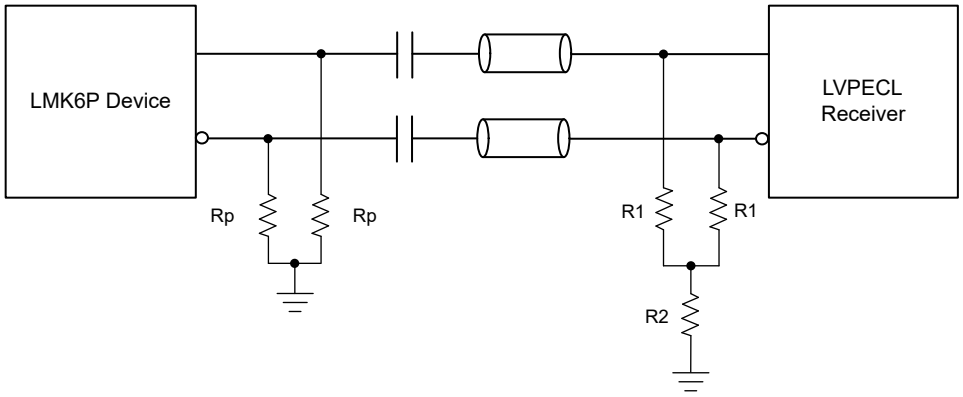


Figure 9-6. LMK6P Output AC-Coupled to LVPECL Receiver With External Termination/Biasing (Y-Network)

Table 9-4. LMK6P Y-Network AC-Coupled Resistor Values

SUPPLY (V)	Rp (Ω)	R1 (Ω)	R2 (Ω)
3.3	207.5	50	78.8
2.5	112.5	50	31.3
1.8	83.3	50	16.7

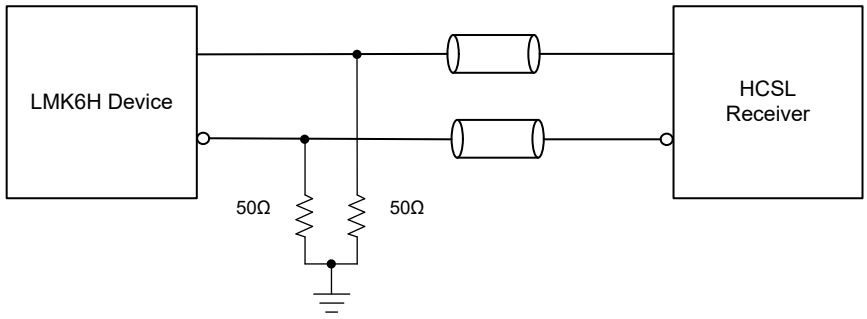


Figure 9-7. LMK6H Output to HCSL Receiver With External Termination

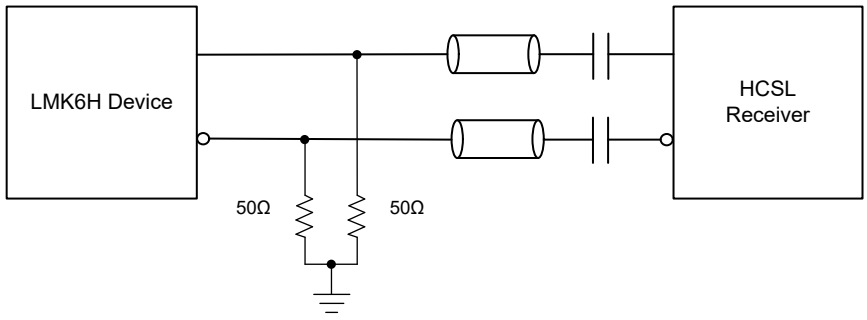


Figure 9-8. LMK6H Output AC-Coupled to HCSL Receiver With External Termination

9.3.5 Temperature Stability

Figure 9-9 shows the frequency stability of LMK6x BAW oscillator over the full temperature range –40°C to 105°C on 64 units. This represents the typical temperature stability of the device, remaining below ±10-ppm.

ADVANCE INFORMATION

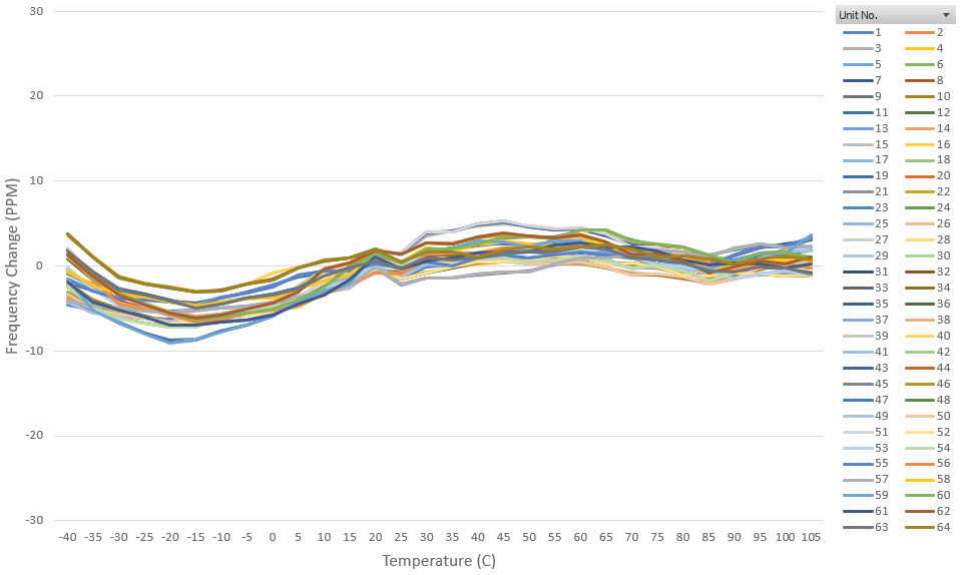


Figure 9-9. Frequency Change Over Temperature

9.3.6 Mechanical Robustness

For reference oscillators, vibration and shock are common causes for increased phase noise and jitter, frequency shift and spikes, or even physical damages to the resonator and its package. Compared to quartz crystals, the BAW resonator is more immune to vibration and shock due to its orders of magnitude smaller mass and higher frequency—that is force applied to the device from acceleration is much smaller due to smaller mass.

Figure 9-10 shows the LMK6x BAW oscillator vibration performance. In this test, the LMK6x oscillator mounted on an EVM is subject to 10g acceleration force, ranging from 50 Hz to 2 kHz in x, y, and z-axis. Frequency deviation is measured in Hz through the E5052 phase noise analyzer under transient mode. The measurement is then converted to ppb and normalized to ppb/g and plotted below. LMK6x performance under vibration is approximately 1 ppb/g while most quartz oscillators best case is 3 ppb/g and worse can be above10 ppb/g.

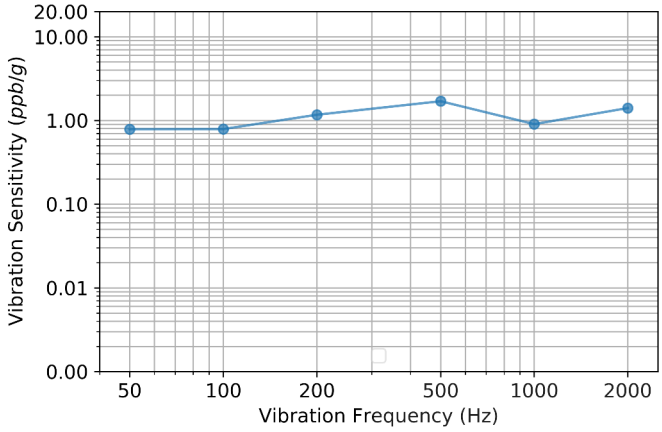


Figure 9-10. LMK6X BAW Oscillator Vibration Performance

9.4 Device Functional Modes

The device has one mode of operation that applies when operated within the *Recommended Operating Conditions*.

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The LMK6x is high-performance, fixed-frequency oscillator that can be used as a reference clock. The product family supports any output frequency, differential or singled-ended output types, and 1.8-V or 2.5-V through 3.3-V supply rails.

10.2 Typical Application

For reference schematic to help implement the LMK6x family of oscillators, refer to the *Power Supply Recommendations* for supply rail decoupling and *Clock Output Interfacing and Termination* for output clock required termination and biasing. Figure 10-1 shows the LMK6x EVM schematic which can be used as a reference, as well.

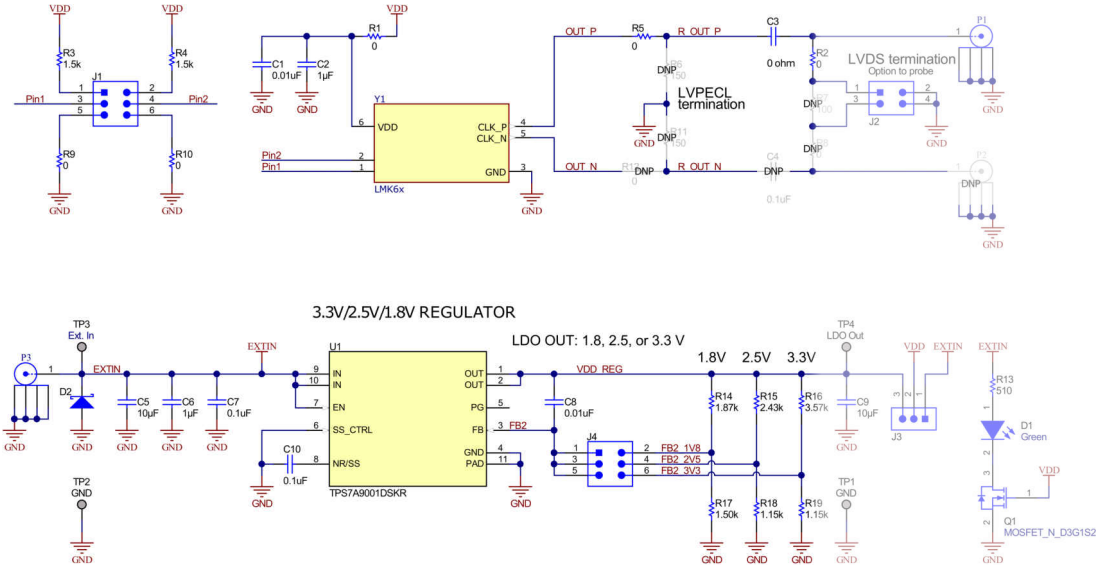


Figure 10-1. LMK6x EVM Schematic

10.2.1 Design Requirements

The LMK6x is a fixed-frequency oscillator with no programming needed. Make sure to follow the recommended termination options as described in the *Clock Output Interfacing and Termination* section closely.

ADVANCE INFORMATION

11 Power Supply Recommendations

For the best electrical performance of the LMK6x, TI recommends using a combination of 10 µF, 1 µF, and 0.1 µF on its power supply bypass network. TI also recommends using component side mounting of the power-supply bypass capacitors, and it is best to use 0201 or 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low impedance connection to the ground plane.

12 Layout

12.1 Layout Guidelines

The following sections provides recommendations for board layout, solder reflow profile and power-supply bypassing when using the LMK6x to ensure good thermal and electrical performance and signal integrity of the entire system.

12.1.1 Ensuring Thermal Reliability

The LMK6x is a high-performance device. Therefore, pay careful attention to device configuration and printed circuit board (PCB) layout with respect to power consumption. The ground pin must be connected to the ground plane of the PCB through three vias or more, as shown in Figure 12-1, to maximize thermal dissipation out of the package.

The equation below describes the relationship between the PCB temperature around the LMK6x and its junction temperature.

$$T_B = T_J - \Psi_{JB} \times P \quad (1)$$

where

- T_B: PCB temperature around the LMK6x
- T_J: Junction temperature of LMK6x
- Ψ_{JB}: Junction-to-board thermal resistance parameter of LMK6x (refer to the *Thermal Information* tables in the *Specifications* section for this information)
- P: On-chip power dissipation of LMK6x

ADVANCE INFORMATION

12.1.2 Best Practices for Signal Integrity

For the best electrical performance and signal integrity of entire system with the LMK6x, TI recommends routing vias into decoupling capacitors and then to the LMK6x. TI also recommends increasing the via count and width of the traces wherever possible. These steps ensure the lowest impedance and shortest path for high-frequency current flow. Figure 12-1 shows the layout recommendation for the LMK6x.

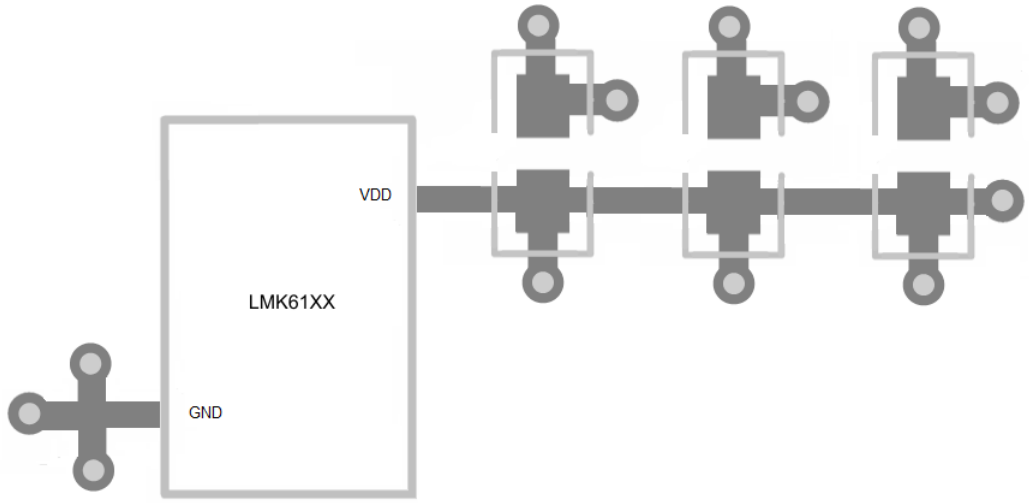


Figure 12-1. LMK6x Layout Recommendation for Power Supply and Ground

12.1.3 Recommended Solder Reflow Profile

TI recommends following the solder paste supplier's recommendations to optimize flux activity and to achieve proper melting temperatures of the alloy within the guidelines of J-STD-20. It is preferable for the LMK6x to be processed with the lowest peak temperature possible while also remaining below the components peak temperature rating as listed on the MSL label. The exact temperature profile would depend on several factors including maximum peak temperature for the component as rated on the MSL label, Board thickness, PCB material type, PCB geometries, component locations, sizes, densities within PCB, as well solder manufactures recommended profile, and capability of the reflow equipment to as confirmed by the SMT assembly operation.

12.2 Layout Examples

Figure 12-2 through Figure 12-5 show the printed circuit board (PCB) layout examples as done on the evaluation module (EVM) for the LMK6x.

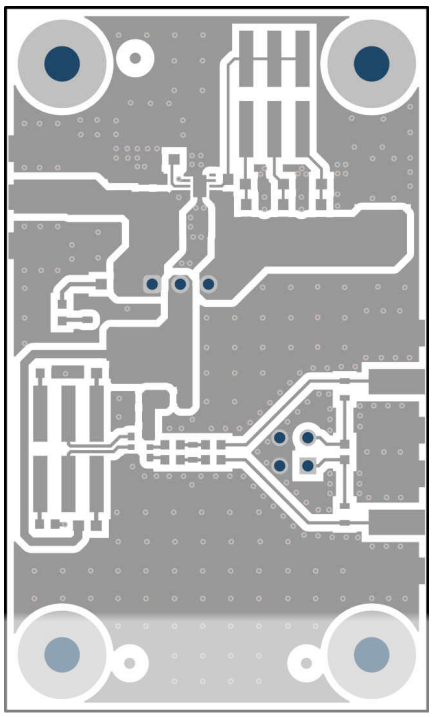


Figure 12-2. PCB Layout Example from LMK6 EVM, Top Layer

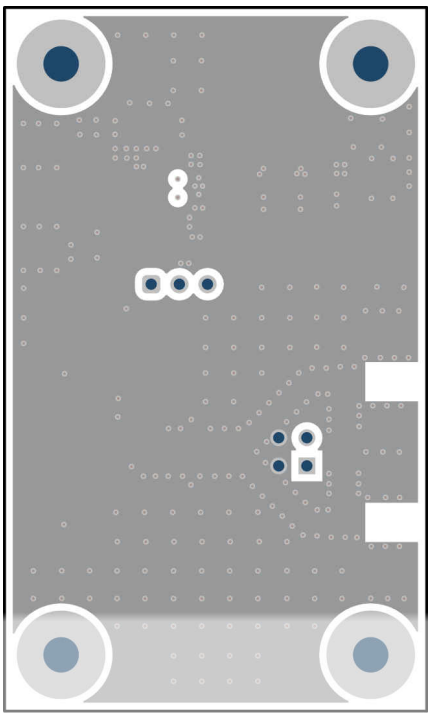


Figure 12-3. PCB Layout Example from LMK6 EVM, GND Layer

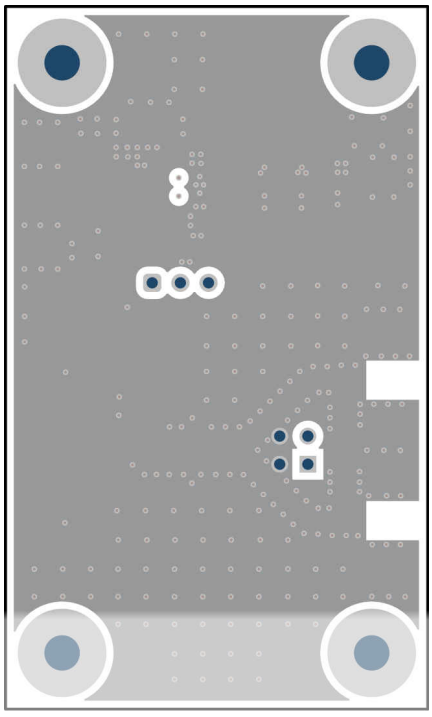


Figure 12-4. PCB Layout Example from LMK6 EVM, GND Layer

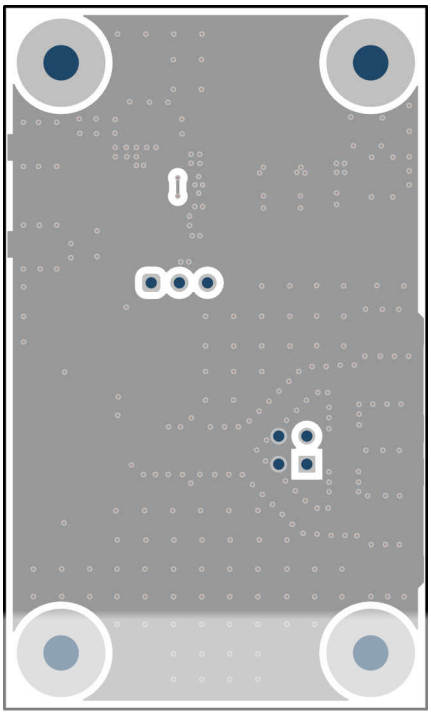


Figure 12-5. PCB Layout Example from LMK6 EVM, Bottom Layer

13 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation, see the following:

Texas Instruments, *LMK6xxEVM Evaluation Instructions*

13.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, *your device*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (for example, *your device*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX and TMDX) through fully qualified production devices and tools (TMS and TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

TMP Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

TMS Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

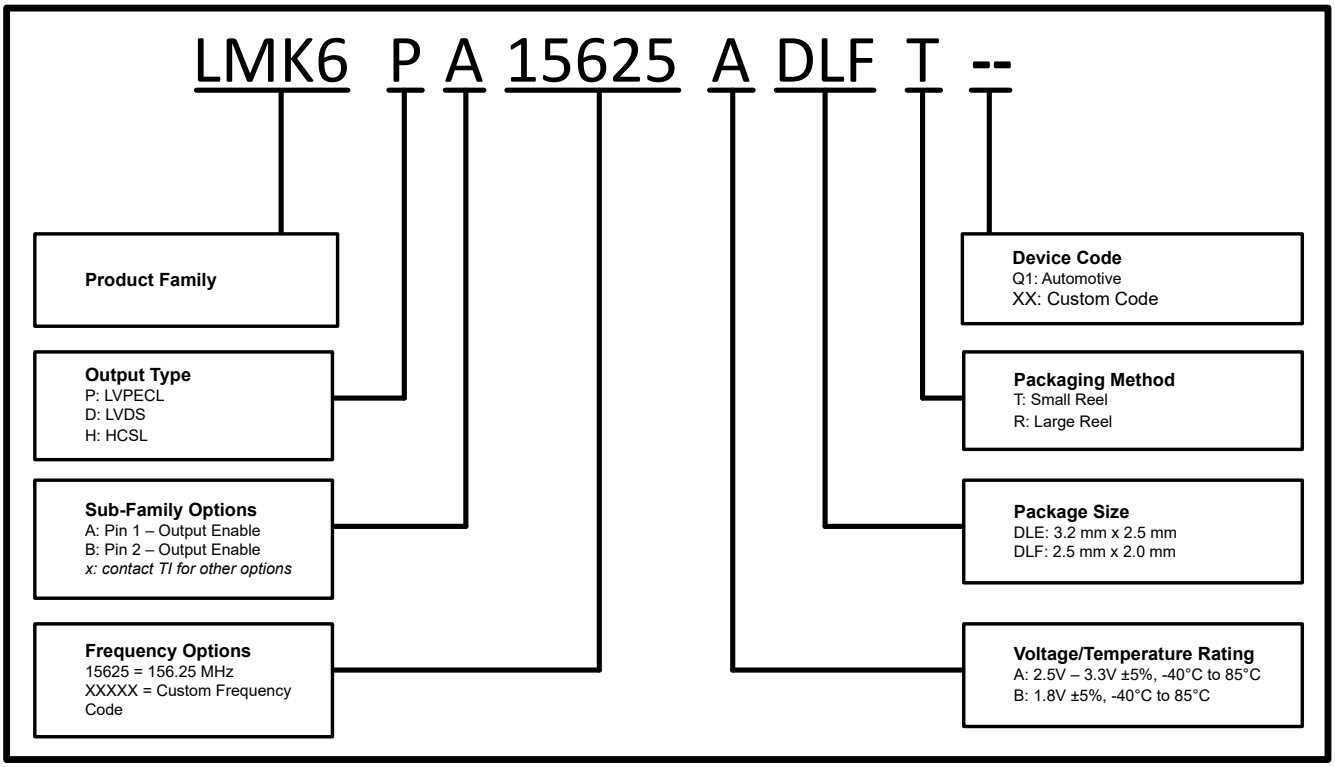
ADVANCE INFORMATION

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, *your package*), the temperature range (for example, blank is the default commercial temperature range), and the device speed range, in megahertz (for example, *your device speed range*). Figure x provides a legend for reading the complete device name for any *your device* device.

For orderable part numbers of *your device* devices in the *your package* package types, see the Package Option Addendum of this document, ti.com, or contact your TI sales representative.

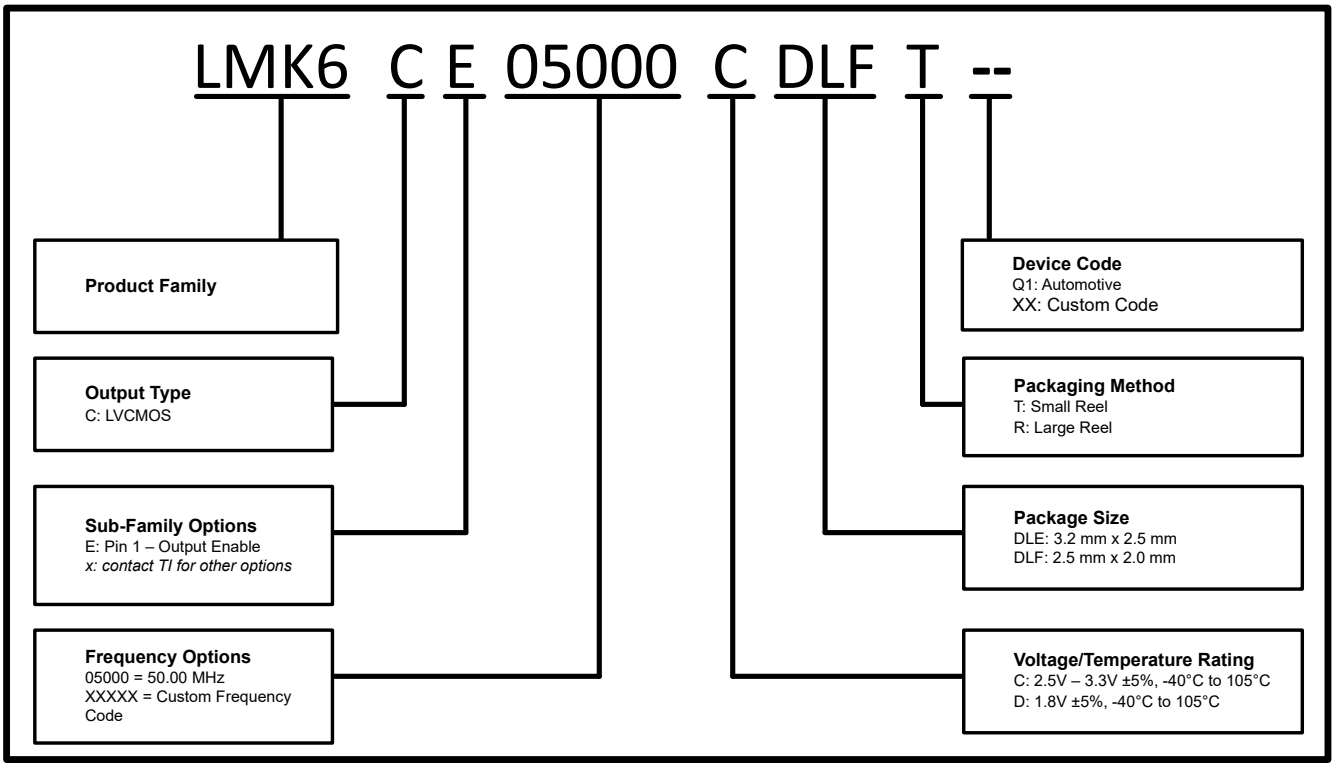
For additional description of the device nomenclature markings on the die, see the *Silicon Errata*.



Note: Contact your TI representative to pre-order specific devices. Email: ti_osc_customer_requirement@list.ti.com

Figure 13-1. Part Number Guide: LMK6P, LMK6D, and LMK6H Device Nomenclature

ADVANCE INFORMATION



Note: Contact your TI representative to pre-order specific devices. Email: ti_osc_customer_requirement@list.ti.com

Figure 13-2. Part Number Guide: LMK6C Device Nomenclature

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

14 Mechanical, Packaging, and Orderable Information

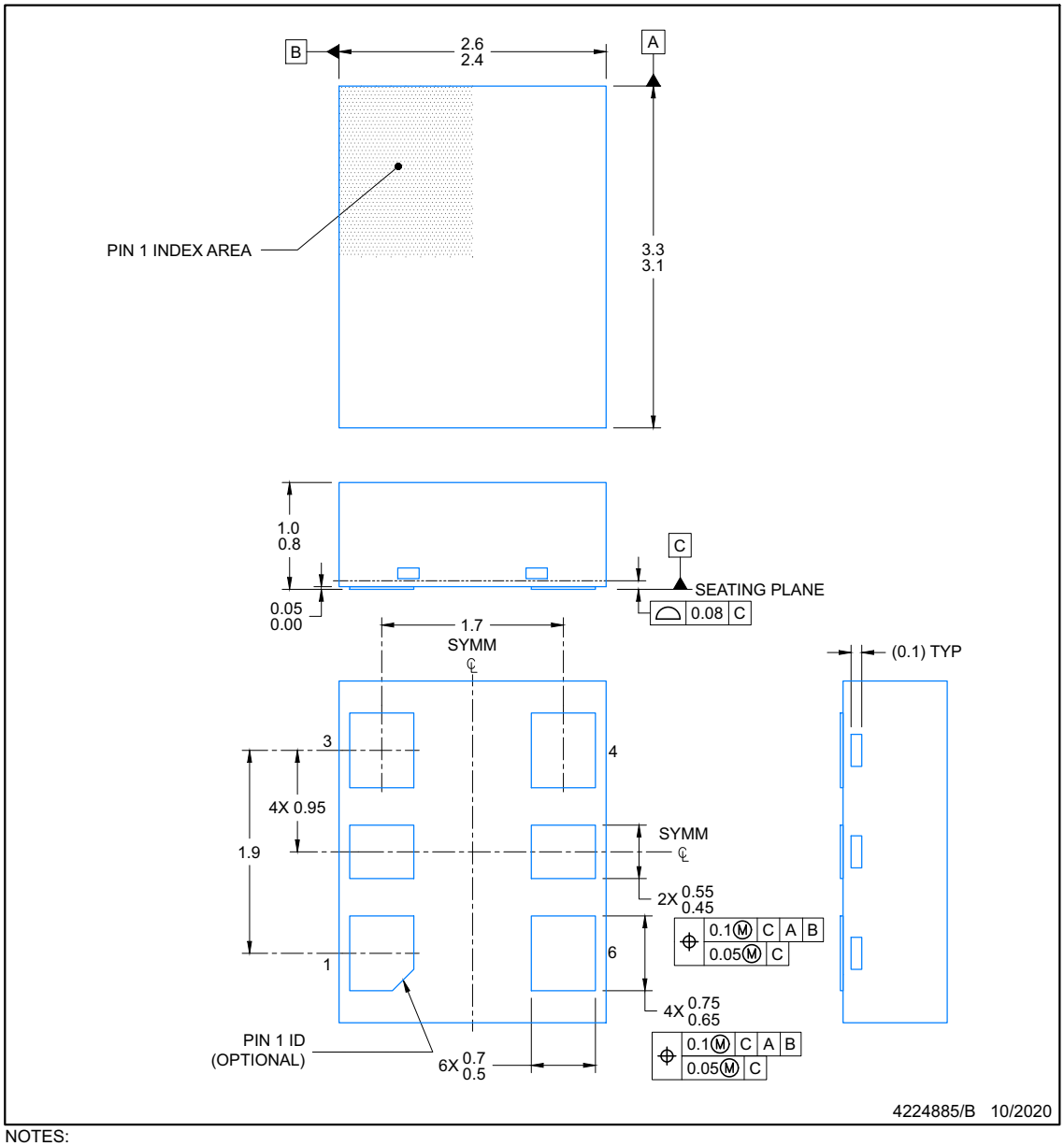
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DLE0006A

VSON - 1 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

www.ti.com

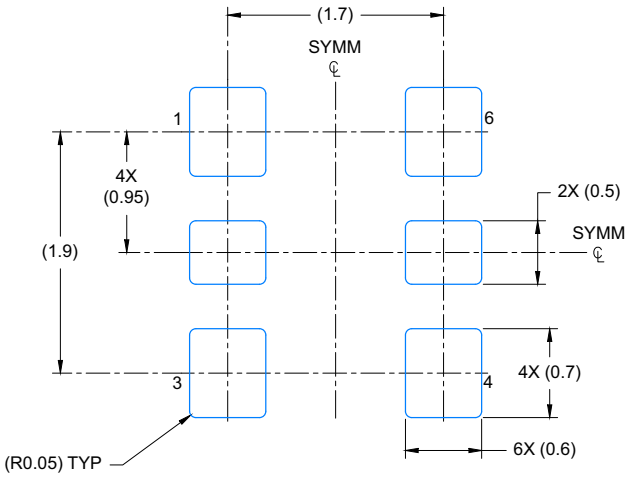
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

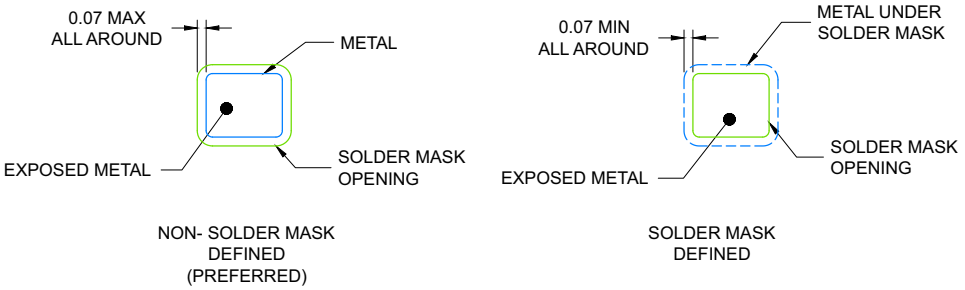
DLE0006A

VSON - 1 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224885/B 10/2020

NOTES: (continued)

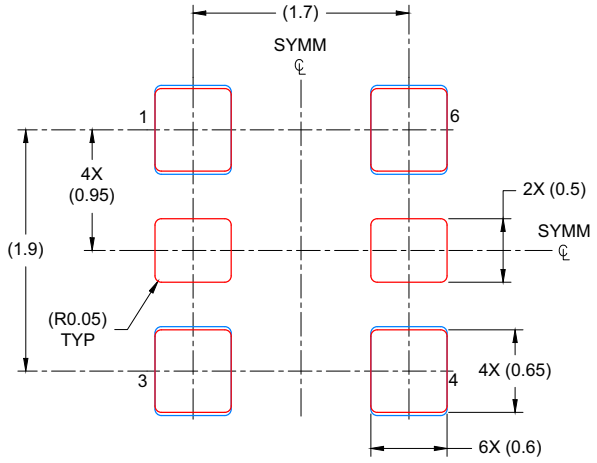
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .

EXAMPLE STENCIL DESIGN

DLE0006A

VSON - 1 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 1,3,4 & 6: 93%
SCALE: 20X

4224885/B 10/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

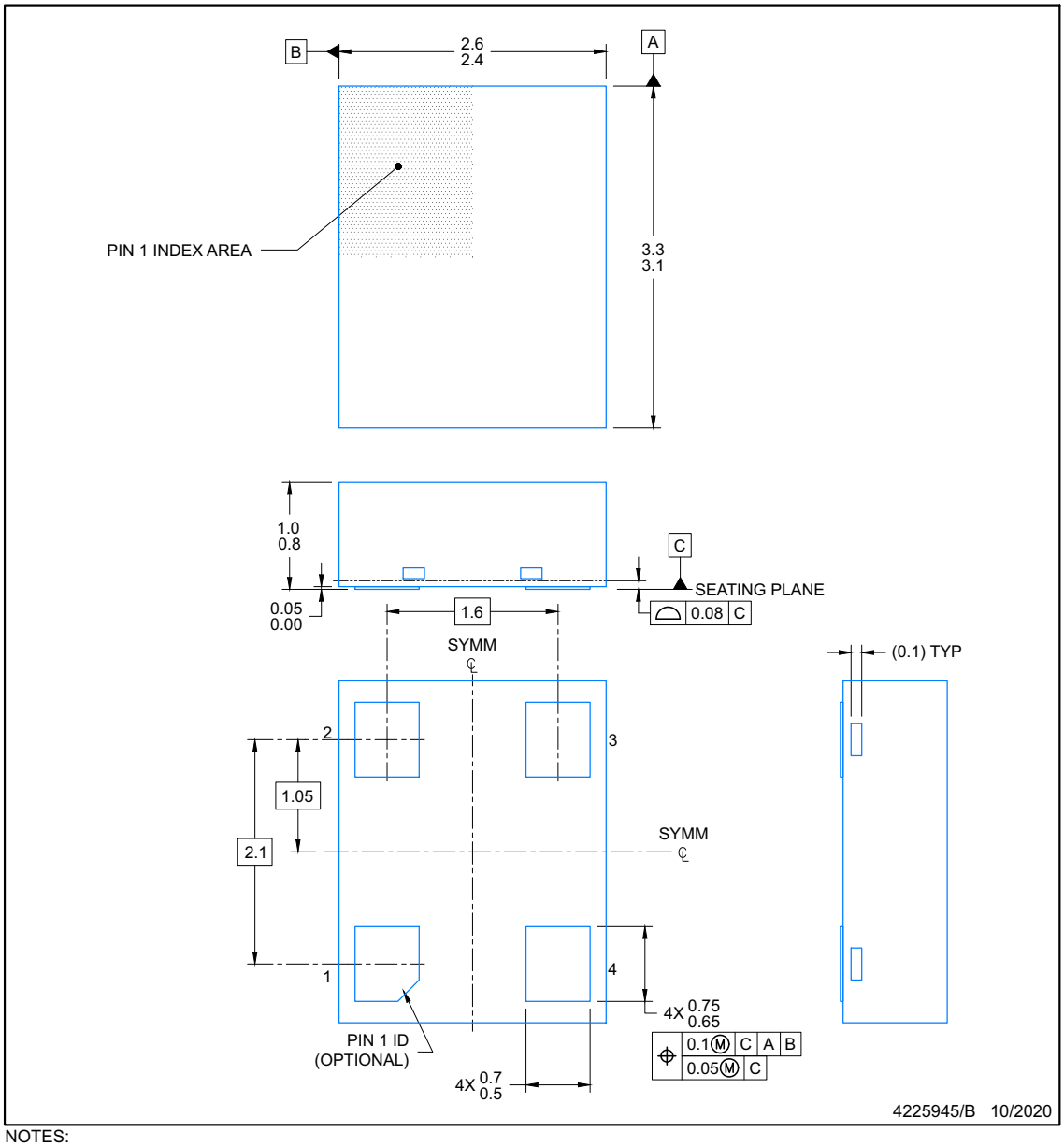
ADVANCE INFORMATION

PACKAGE OUTLINE

DLE0004A

VSON - 1 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



NOTES:

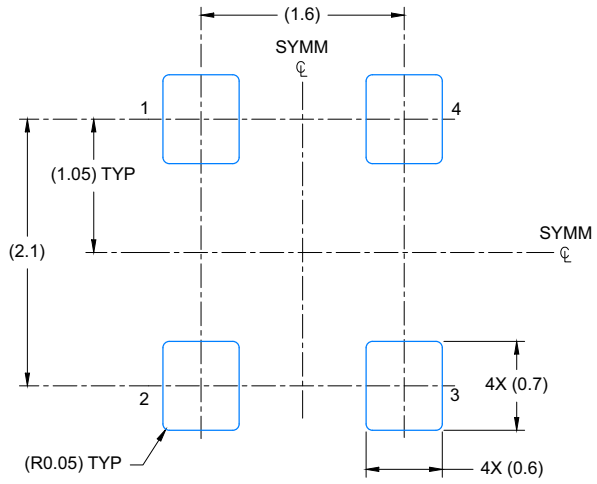
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

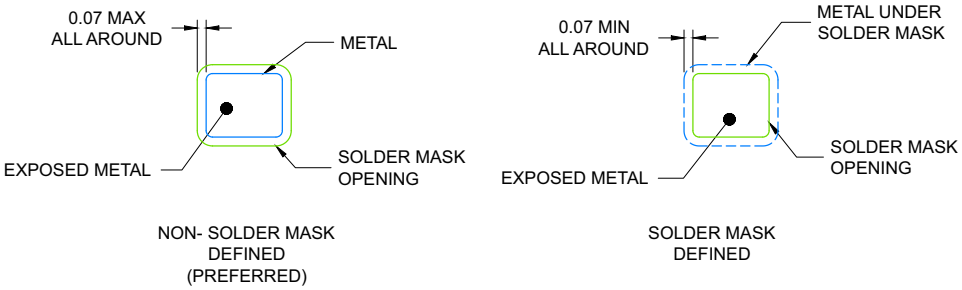
DLE0004A

VSON - 1 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4225945/B 10/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .

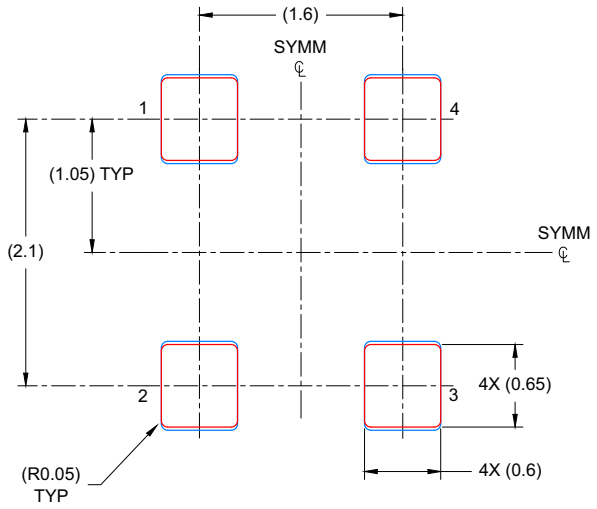
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DLE0004A — **VSON - 1 mm max height**

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
ALL PADS: 93%
SCALE: 20X

4225945/B 10/2020

NOTES: (continued)

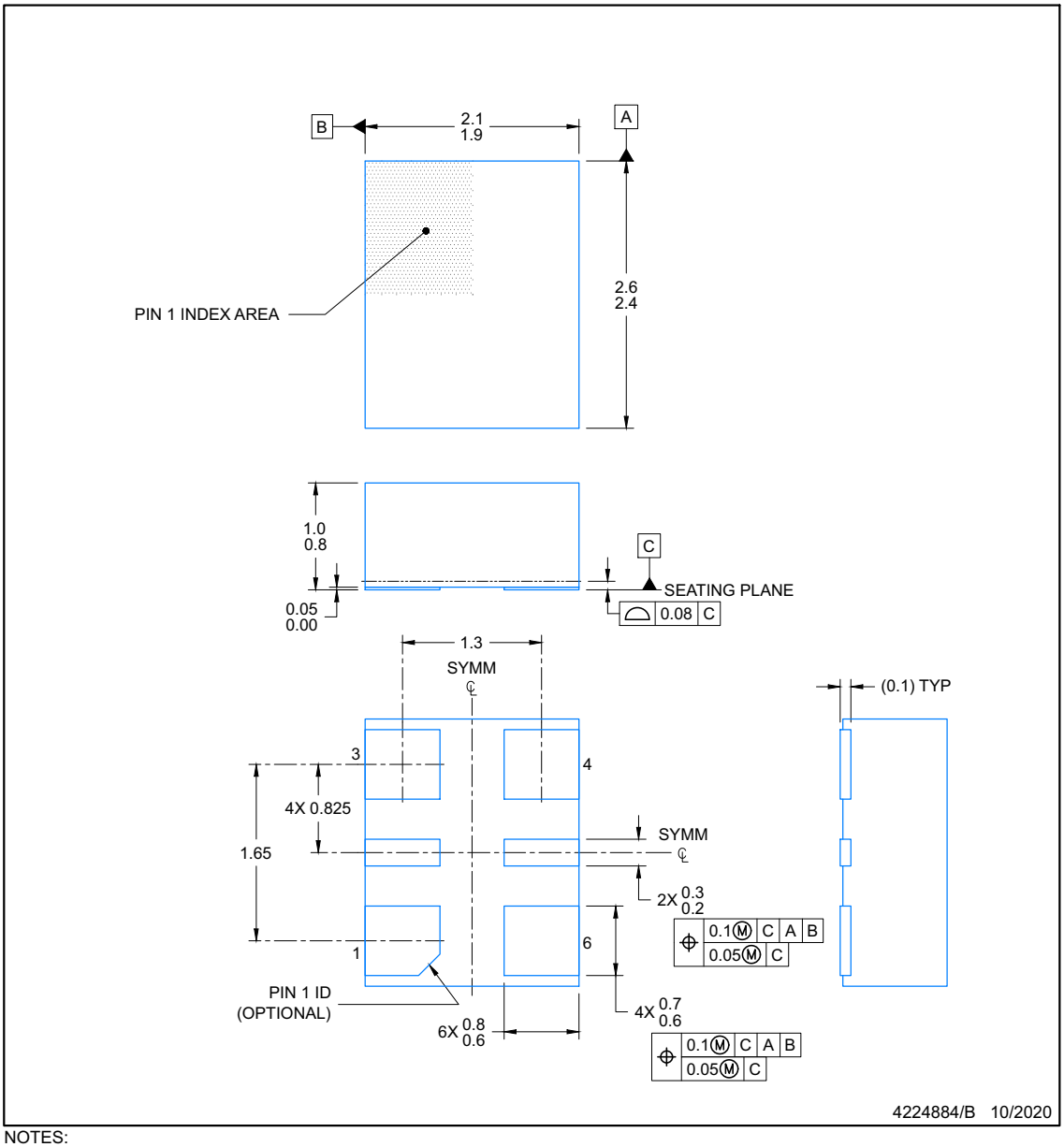
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DLF0006A

VSON - 1 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

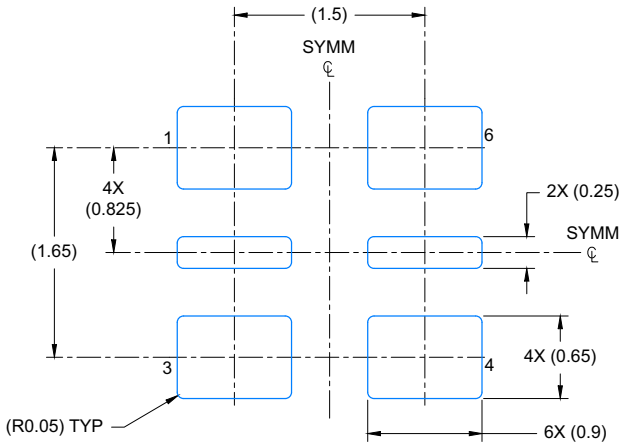
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

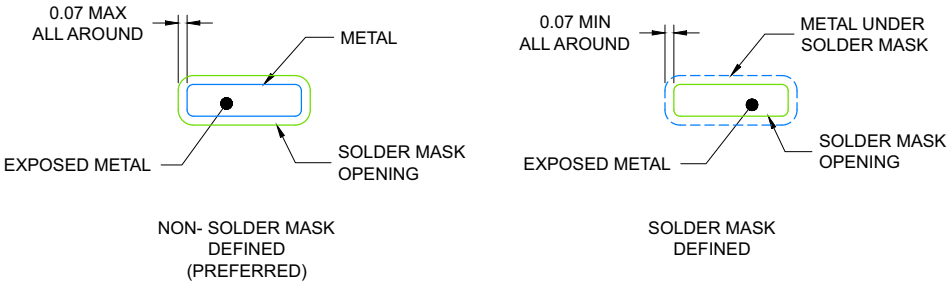
DLF0006A

VSON - 1 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224884/B 10/2020

NOTES: (continued)

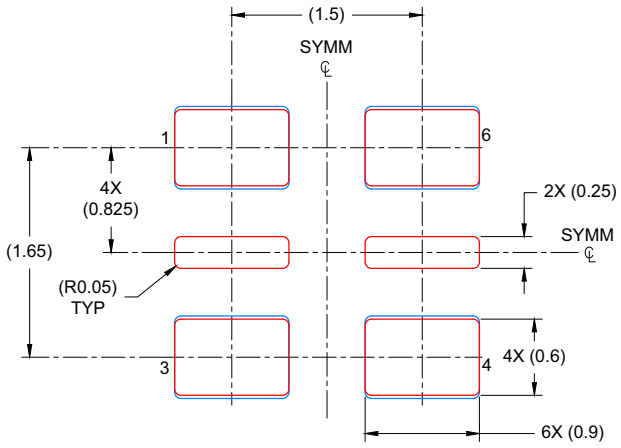
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .

EXAMPLE STENCIL DESIGN

DLF0006A

VSON - 1 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 1,3,4 & 6: 92%
SCALE: 20X

4224884/B 10/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

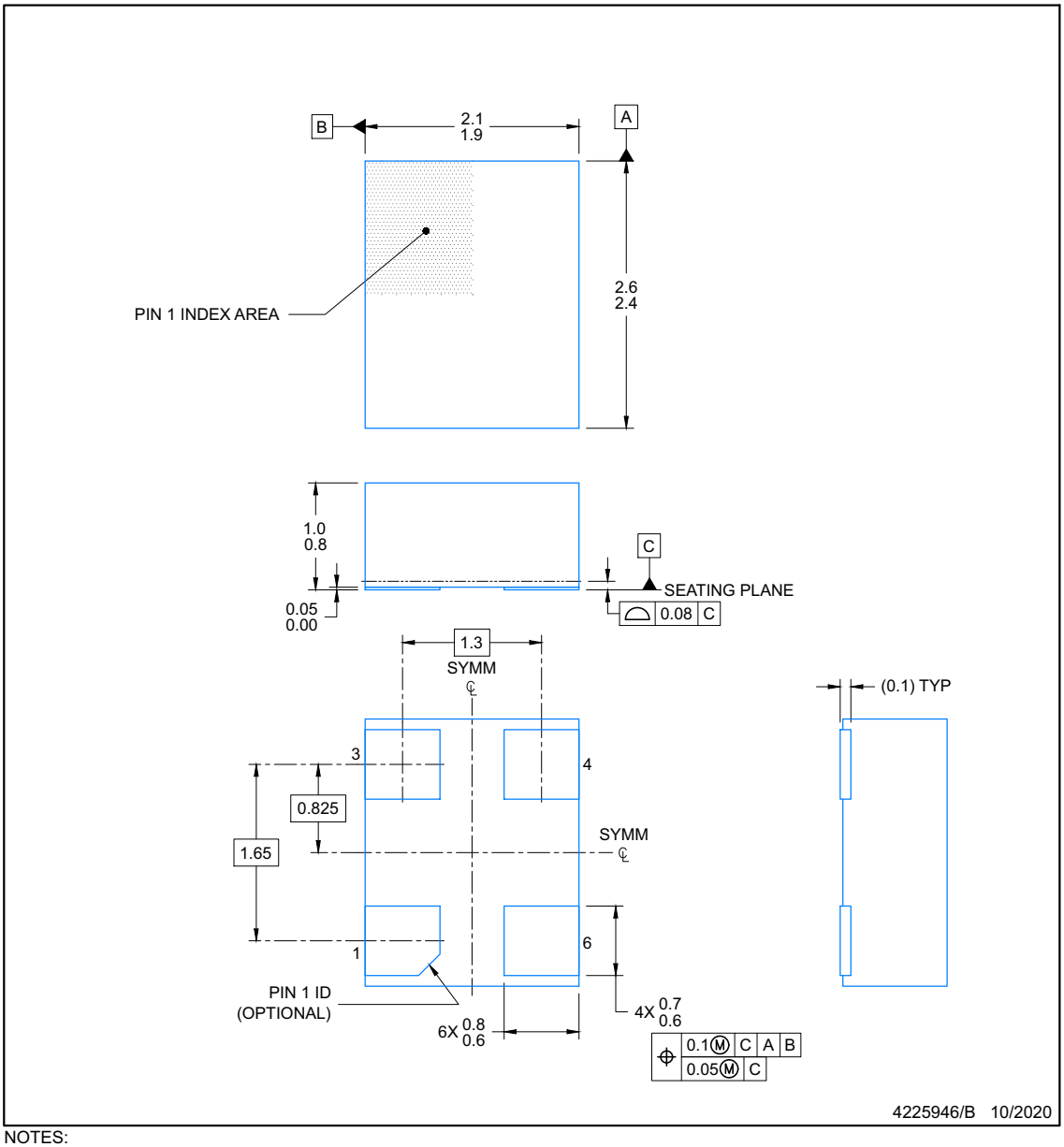
ADVANCE INFORMATION

PACKAGE OUTLINE

DLF0004A

VSON - 1 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



NOTES:

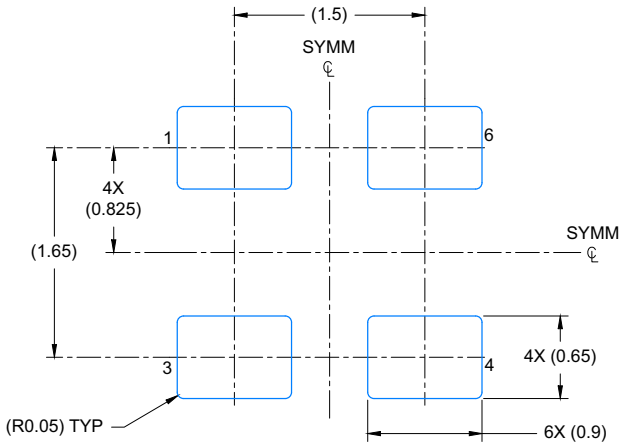
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

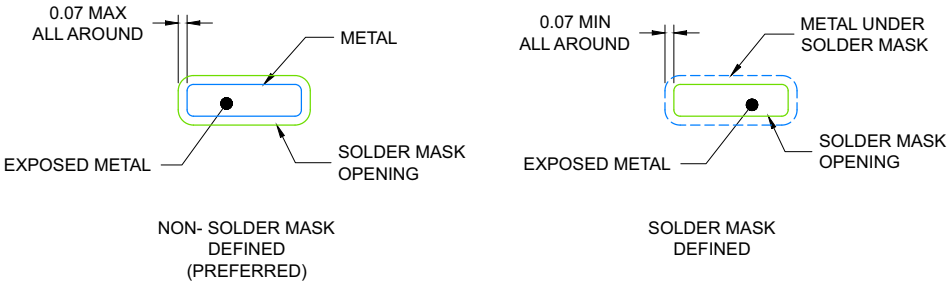
DLF0004A

VSON - 1 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4225946/B 10/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .

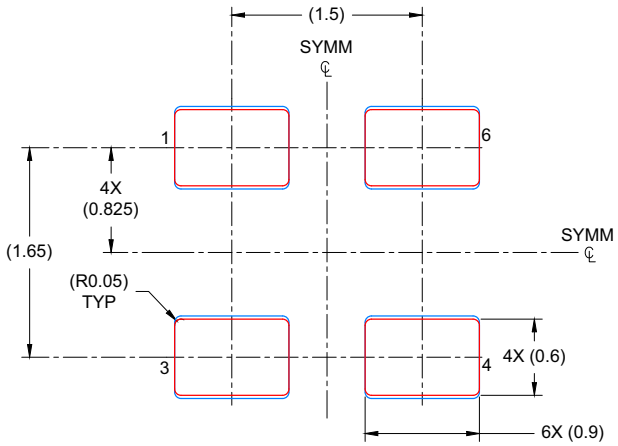
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DLF0004A — **VSON - 1 mm max height**

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 1,3,4 & 6: 92%
SCALE: 20X

4225946/B 10/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

14.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(4)	MSL Peak Temp (3)	Frequency (MHz)	Op Temp (°C)	Device Marking(5) (6)
PLMK6CE02400CDLFT	ACTIVE	VSON	DLF	4	Call TI	Call TI	Call TI	Call TI	24	-40C° to 105C°	P6C5
PLMK6CE02500CDLFT	ACTIVE	VSON	DLF	4	Call TI	Call TI	Call TI	Call TI	25	-40C° to 105C°	P6C6
PLMK6CE15625CDLFT	ACTIVE	VSON	DLF	4	Call TI	Call TI	Call TI	Call TI	156.25	-40C° to 105C°	P6C4
PLMK6CE05000CDLFT	ACTIVE	VSON	DLF	4	Call TI	Call TI	Call TI	Call TI	50	-40C° to 105C°	P6C1
PLMK6CE02400CDLET	ACTIVE	VSON	DLE	4	Call TI	Call TI	Call TI	Call TI	24	-40C° to 105C°	P6C2
PLMK6CE02500CDLET	ACTIVE	VSON	DLE	4	Call TI	Call TI	Call TI	Call TI	25	-40C° to 105C°	P6C3
PLMK6CE15625DDLFT	ACTIVE	VSON	DLF	4	Call TI	Call TI	Call TI	Call TI	156.25	-40C° to 105C°	P6C8
PLMK6CE01920CDLFT	ACTIVE	VSON	DLF	4	Call TI	Call TI	Call TI	Call TI	19.2	-40C° to 105C°	P6C9

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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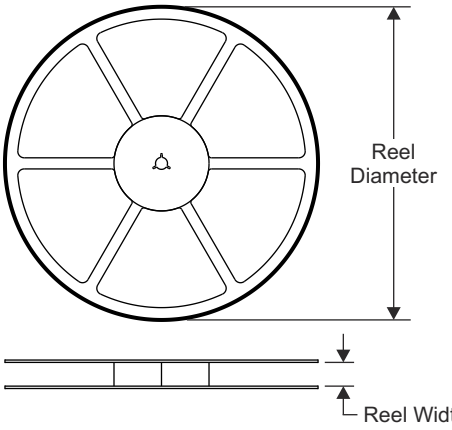
ADVANCE INFORMATION

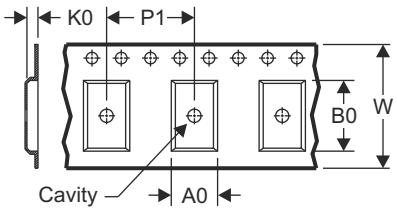
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

14.2 Tape and Reel Information

REEL DIMENSIONS

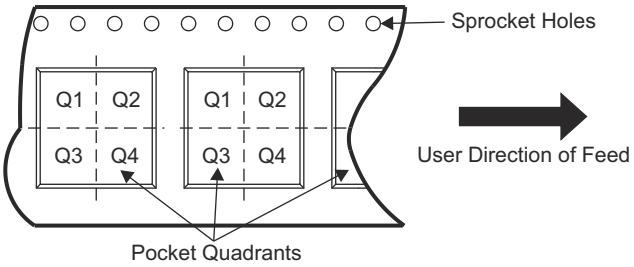


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

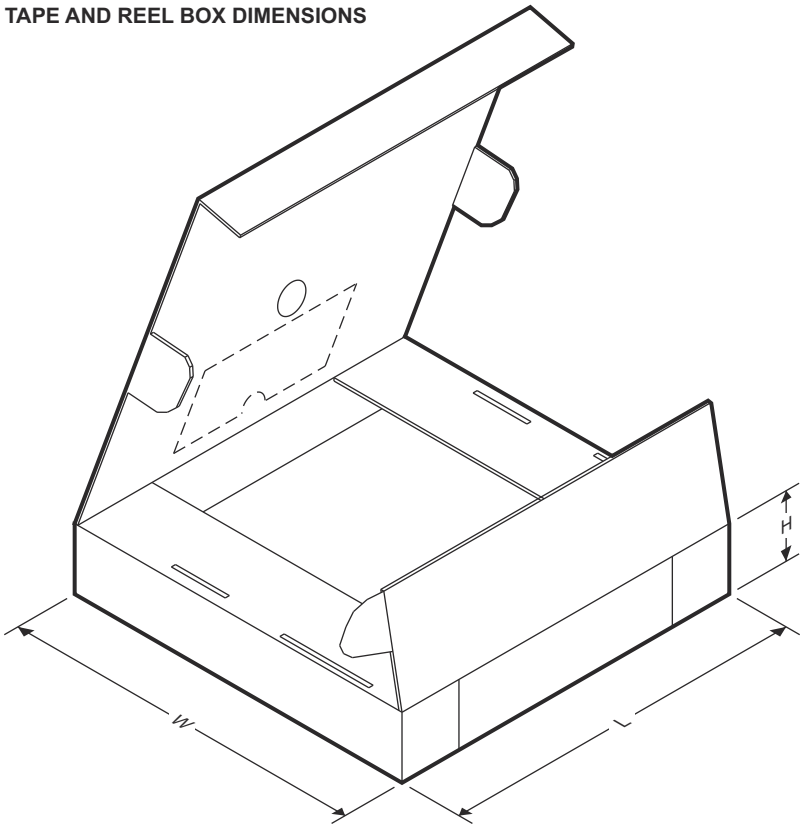


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PLMK6CE02400CDLFT	VSON	DLF	4	250	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI
PLMK6CE02500CDLFT	VSON	DLF	4	250	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI
PLMK6CE15625CDLFT	VSON	DLF	4	250	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI
PLMK6CE05000CDLFT	VSON	DLF	4	250	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI
PLMK6CE02400CDLET	VSON	DLE	4	250	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI
PLMK6CE02500CDLET	VSON	DLE	4	250	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI
PLMK6CE15625DDLFT	VSON	DLF	4	250	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI
PLMK6CE01920CDLFT	VSON	DLF	4	250	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI	Call TI

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PLMK6CE02400CDLFT	VSON	DLF	4	250	Call TI	Call TI	Call TI
PLMK6CE02500CDLFT	VSON	DLF	4	250	Call TI	Call TI	Call TI
PLMK6CE15625CDLFT	VSON	DLF	4	250	Call TI	Call TI	Call TI
PLMK6CE05000CDLFT	VSON	DLF	4	250	Call TI	Call TI	Call TI
PLMK6CE02400CDLET	VSON	DLE	4	250	Call TI	Call TI	Call TI
PLMK6CE02500CDLET	VSON	DLE	4	250	Call TI	Call TI	Call TI
PLMK6CE15625DDLFT	VSON	DLF	4	250	Call TI	Call TI	Call TI
PLMK6CE01920CDLFT	VSON	DLF	4	250	Call TI	Call TI	Call TI

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PLMK6CE01920CDLFT	ACTIVE	VSON	DLF	4	250	TBD	Call TI	Call TI	-40 to 105		Samples
PLMK6CE02400CDLET	ACTIVE	VSON	DLE	4	250	TBD	Call TI	Call TI	-40 to 105		Samples
PLMK6CE02400CDLFT	ACTIVE	VSON	DLF	4	250	TBD	Call TI	Call TI	-40 to 105		Samples
PLMK6CE02500CDLET	ACTIVE	VSON	DLE	4	250	TBD	Call TI	Call TI	-40 to 105		Samples
PLMK6CE02500CDLFT	ACTIVE	VSON	DLF	4	250	TBD	Call TI	Call TI	-40 to 105		Samples
PLMK6CE04000CDLFT	ACTIVE	VSON	DLF	4	250	TBD	Call TI	Call TI	-40 to 105		Samples
PLMK6CE05000CDLFT	ACTIVE	VSON	DLF	4	250	TBD	Call TI	Call TI	-40 to 105		Samples
PLMK6CE15625CDLFT	ACTIVE	VSON	DLF	4	250	TBD	Call TI	Call TI	-40 to 105	PCEC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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