# LMX1204 Low-Noise, High-Frequency JESD Buffer/Multiplier/Divider

## 1 Features

- 300-MHz to 12.8-GHz output frequency
- Ultra-low noise
  - Noise floor of –161 dBc/Hz at 6-GHz output
  - 1/f Noise of –154 dBc/Hz at 6-GHz output, 10-kHz offset
  - Under 30-fs additive jitter (DC to $f_{CLK}$ integration range)
- 4 high-frequency clocks with corresponding SYSREF outputs
  - Shared divider that supports ÷1 (buffer mode), ÷2,3,4,5,6,7, and 8
  - Shared PLL-based multiplier that supports x1 (filter mode), x2, x3, and x4
- LOGICLK output with corresponding SYSREF output
  - On separate divide bank
  - ÷1, 2, 4 pre-divider
  - ÷1 (bypass), 2, …, 1023 post divider
- 8 programmable output power levels
- Synchronized SYSREF clock outputs
  - 508 delay step adjustments of less than 2.5 ps each at 12.8 GHz
  - Generator and repeater modes
  - Windowing feature for SYSREFREQ pins to optimize timing
- SYNC feature to all divides and multiple devices
- 2.5-V operating voltage
- –40ºC to +85ºC operating temperature

## 2 Applications

- General purpose:
  - Data converter clocking
  - Clock distribution/multiplication/division
- Test equipment:
  - Oscilloscopes
  - Wideband digitizers
  - Wireless equipment testers
- Aerospace and defense:
  - Radar
  - Electronic warfare
  - Seeker front end
  - Munitions
  - Phased array antenna/beam forming

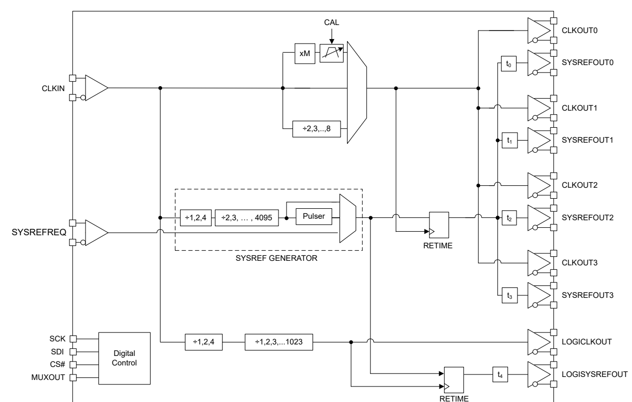
## 3 Description

The high-frequency capability and extremely low jitter of this device, makes a great solution to clock precision, high-frequency data converters without degradation to the signal-to-noise ratio. Each of the four high-frequency clock outputs, and additional LOGICLK output with larger divider range, is paired with a SYSREF output clock signal. The SYSREF signal for JESD interfaces can either be internally generated or passed in as an input and re-clocked to the device clocks. For data converter clocking applications, it is critical to have the jitter of the clock be less than the aperture jitter of the data converter. In applications where more than four data converters must be clocked, a variety of cascading architectures can be developed using multiple devices to distribute all the high-frequency clocks and SYSREF signals required. With low jitter and noise floor, this device combined with an ultra-low noise reference clock source is an exemplary solution for clocking data converters, especially when sampling above 3 GHz.

**Package Information**[(1)]

| PART NUMBER | PACKAGE | BODY SIZE |
|---|---|---|
| LMX1204 | VQFN (40) | 6.00 mm × 6.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.




**Block Diagram**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision * (July 2021) to Revision A (August 2022)** **Page**

- Changed data sheet status from Advanced Information to Production Data......1
- Added filter mode information to the data sheet......1
- Added descriptions for POR, multiplier, filter mode, common mode voltage, and other topics in the *Detailed Description* section......15
- Changed Table 8-1 ......28
- Moved the *Power Supply Recommendations* and *Layout* sections to the *Application and Implementation* section......31


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## 5 Pin Configuration and Functions

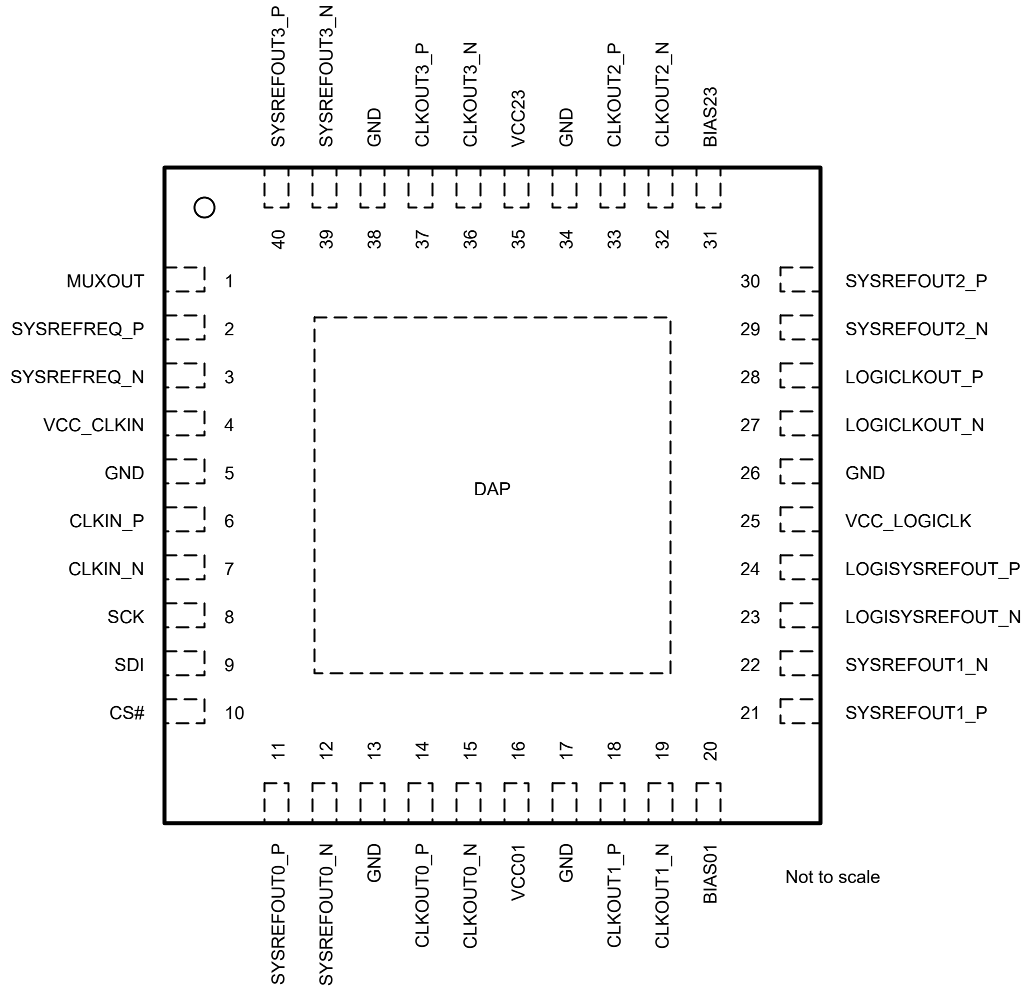


**Figure 5-1. RHA Package 40-Pin VQFN Top View**

**Table 5-1. Pin Functions**

| NAME | NO. | TYPE | DESCRIPTION |
|---|---|---|---|
| BIAS01 | 20 | BYP | If not using the multiplier, this pin may be left open. If using the multiplier, bypass this pin to GND with a 10-nF capacitor for optimal noise performance. |
| BIAS23 | 31 | BYP | If not using the multiplier, this pin may be left open. If using the multiplier, bypass this pin to GND with a 10-µF and 0.1-µF capacitor for optimal noise performance. |
| CLKIN_N | 7 | I | Differential reference input clock. Internal 50-Ω termination. AC-couple with a capacitor appropriate to the input frequency (typically 0.1 µF or smaller). If using single-ended, terminate unused side with a series AC-coupling capacitor 50-Ω resistor to GND. |
| CLKIN_P | 6 | | |
| CLKOUT0_N | 15 | O | Differential clock output pairs. Each pin is an open-collector output with internally integrated 50-Ω resistor with programmable output swing. AC coupling required. |
| CLKOUT0_P | 14 | | |
| CLKOUT1_N | 19 | | |
| CLKOUT1_P | 18 | | |
| CLKOUT2_N | 32 | | |
| CLKOUT2_P | 33 | | |
| CLKOUT3_N | 36 | | |
| CLKOUT3_P | 37 | | |
| CS# | 10 | I | SPI chip select. High impedance CMOS input. Accepts up to 3.3 V. |
| DAP | DAP | GND | Ground these pins. |
| GND | 5,13,17,26,34,38 | | |
| LOGICLKOUT_N | 27 | O | Differential clock output pair. Selectable CML, LVDS, or LVPECL format. Programmable common-mode voltage. |
| LOGICLKOUT_P | 28 | | |
| LOGISYSREFOUT_N | 23 | O | Differential clock output pair. Selectable CML, LVDS, or LVPECL format. Programmable common-mode voltage. |
| LOGISYSREFOUT_P | 24 | | |
| MUXOUT | 1 | O | Multiplexed pin serial data readback and lock status of the multiplier. |
| SCK | 8 | I | SPI clock. High impedance CMOS input. Accepts up to 3.3 V. |
| SDI | 9 | I | SPI data input. High impedance CMOS input. Accepts up to 3.3 V. |
| SYSREFREQ_N | 3 | I | Differential SYSREF request input for JESD204B support. Internal 50-Ω AC coupled to internal common-mode voltage or capacitor to GND. Supports AC and DC coupling which can directly accept a common mode voltage of 1.2 to 2 V. |
| SYSREFREQ_P | 2 | | |
| SYSREFOUT0_N | 12 | O | Differential SYSREF CML output pairs for JESD204B support. Supports AC and DC coupling with programmable common-mode voltage of 0.6 to 2 volts. |
| SYSREFOUT0_P | 11 | | |
| SYSREFOUT1_N | 22 | | |
| SYSREFOUT1_P | 21 | | |
| SYSREFOUT2_N | 29 | | |
| SYSREFOUT2_P | 30 | | |
| SYSREFOUT3_N | 39 | | |
| SYSREFOUT3_P | 40 | | |
| VCC_CLKIN | 4 | PWR | Connect to a 2.5-V supply. Recommend a shunt high frequency capacitor (typically 0.1 µF or smaller) close to the pin in parallel with larger capacitors (typically 1 µF and 10 µF) farther away. |
| VCC_LOGICLK | 25 | | |
| VCC01 | 16 | | |
| VCC23 | 35 | | |


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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | Power supply voltage | –0.3 | 2.75 | V |
| $V_{IN}$ | DC Input Voltage (SCK, SDI, CSB) | GND | 3.6 | V |
| $V_{IN}$ | DC Input Voltage (SYSREFREQ) | GND | $V_{DD}$ + 0.3 | V |
| $V_{IN}$ | AC Input Voltage (CLKIN) | | $V_{DD}$ | Vpp |
| $T_J$ | Junction temperature | | 150 | °C |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Recommended Operating Conditions*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1] | ±2500 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins[2] | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 2.4 | 2.5 | 2.6 | V |
| $T_A$ | Ambient temperature | –40 | | 85 | °C |
| $T_J$ | Junction temperature | | | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC[1] | | RHA (VQFN) | UNIT |
|---|---|---|---|
| | | 40 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 24.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 13.0 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 6.9 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 0.1 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 6.9 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 0.5 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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## 6.5 Electrical Characteristics

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **Current Consumption** | | | | | | | |
| $I_{CC}$ | Supply Current [1] | Powered up, all outputs and SYSREF on | | | 1050 | | mA |
| | | Powered up, all outputs on, all SYSREF off | | | 600 | | mA |
| | | Powered up, all outputs and SYSREF off | | | 265 | | mA |
| | | Powered down[2] | | | 11 | | mA |
| **SYSREF** | | | | | | | |
| $f_{SYSREF}$ | SYSREF output frequency | Generator mode | | | | 200 | MHz |
| | | Repeater mode | | | | 100 | MHz |
| Δt | SYSREF delay step size | $f_{CLKIN}$ = 12.8 GHz | | | 3 | | ps |
| $t_{RISE}$ | Rise time (20% to 80%) | SYSREFOUT | | | 45 | | ps |
| | | LOGISYSREFOUT | CML | | 120 | | ps |
| | | | LVDS | | 120 | | ps |
| | | | LVPECL | | 230 | | ps |
| $t_{FALL}$ | Fall time (20% to 80%) | SYSREFOUT | | | 45 | | ps |
| | | LOGISYSREFOUT | CML | | 120 | | ps |
| | | | LVDS | | 120 | | ps |
| | | | LVPECL | | 170 | | ps |
| $V_{OD}$ | Differential output voltage | SYSREFOUT | | | 0.85 | | Vpp |
| | | LOGISYSREFOUT | CML | | 0.4 | | Vp |
| | | | LVDS | | 0.4 | | Vp |
| | | | LVPECL | | 0.8 | | Vp |
| $V_{SYSREFCM}$ | Common mode voltage | SYSREFOUT | CML<br>SYSREFOUTx_PWR=4<br>100 Ω Differential Load | | 0.8 | | V |
| **SYSREFREQ Pins** | | | | | | | |
| $V_{SYSREFIN}$ | Voltage input range | AC differential voltage | | 0.8 | | 2 | Vpp |
| $V_{CM}$ | Input common mode | Differential 100 Ω Termination, DC coupled<br>Set externally | | 1.2 | 1.3 | 2 | V |
| **Clock Input** | | | | | | | |
| $f_{IN}$ | Input frequency | | | 0.3 | | 12.8 | GHz |
| $P_{IN}$ | Input power | Single-ended power at CLKIN_P or CLKIN_N | | 0 | | 10 | dBm |
| **Clock Outputs** | | | | | | | |
| $f_{OUT}$ | Output frequency | Divide-by-2 | | 0.15 | | 6.4 | GHz |
| $f_{OUT}$ | Output frequency | Buffer Mode | | 0.3 | | 12.8 | GHz |
| $f_{OUT}$ | Output frequency | x1 (filter mode) , x2, x3, x4 | | 3.2 | | 6.4 | GHz |
| $f_{OUT}$ | Output frequency | LOGICLK output | | 1 | | 800 | MHz |
| $t_{CAL}$ | Calibration-time | Multiplier calibration time | $f_{IN}$ = 3.2 GHz; x2<br>$f_{SMCLK}$ = 28 MHz | | 750 | | µs |
| $p_{OUT}$ | Output power | Single-Ended | $f_{CLKLOUT}$= 6 GHz<br>OUTx_PWR = 7 | | 4 | | dBm |
| $t_{RISE}$ | Rise time (20% to 80%) | $f_{CLKOUT}$ = 300 MHz | | | 45 | | ps |
| $t_{FALL}$ | Fall time (20% to 80%) | $f_{CLKOUT}$ = 300 MHz | | | 45 | | ps |
| **Propagation Delay and Skew** | | | | | | | |
| $\lvert t_{SKEW} \rvert$ | Magnitude of skew between outputs | CLKOUTx to CLKOUTy, not LOGICLK | | | 1 | 15 | ps |


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| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **Noise, Jitter, and Spurs** | | | | | | | |
| $J_{CKx}$ | Additive jitter | Additive Jitter. 12k to 100 MHz integration bandwidth. | Buffer Mode | | 5 | | fs, rms |
| | | | Filter Mode | | 12 | | fs, rms |
| | | | x2 Multiplier | | 16 | | fs, rms |
| | | | x3 Multiplier | | 21 | | fs, rms |
| | | | x4 Multiplier | | 26 | | fs, rms |
| Flicker | 1/f flicker noise | Slew Rate > 8 V/ns, $f_{CLK}$=6 GHz | Buffer Mode | | -154 | | dBc/Hz |
| NF | Noise Floor | $f_{OUT}$ = 6 GHz; $f_{Offset}$ ≥ 100 MHz | Buffer Mode | | -161 | | dBc/Hz |
| NF | | | Divide-by-2 | | -160.5 | | dBc/Hz |
| NF | | | Multiplier (x1, x2,x3,x4) | | –161.5 | | dBc/Hz |
| NFL | Noise Floor | LOGICLK output, 300 MHz | CML | | -150.5 | | dBc/Hz |
| NFL | | | LVDS | | -151.5 | | dBc/Hz |
| NFL | | | LVPECL | | -153.5 | | dBc/Hz |
| H2 | Second harmonic | $f_{OUT}$ = 6 GHz (differential), Buffer Mode | | | -25 | | dBc |
| | | $f_{OUT}$ = 6 GHz (single-ended), Buffer Mode | | | -13 | | dBc |
| | | $f_{OUT}$ = 6 GHz, single-ended, Divide by 2 | | | -16 | | dBc |
| H1/2 | Input clock leakage spur | $f_{OUT}$ = 6 GHz (single-ended) | x2 ($f_{SPUR}$ = 3 GHz) | | -40 | | dBc |
| H1/3 | | | x3 ($f_{SPUR}$ = 2 GHz) | | –50 | | dBc |
| H1/4 | | | x4 ($f_{SPUR}$ = 1.5 GHz) | | -54 | | dBc |
| $I_{SPUR}$ | LOGICLK to CLKOUT | $f_{SPUR}$ = 300 MHz (differential) | | | –70 | | dBc |
| **Digital Interface (SCK, SDI, CS#, MUXOUT)** | | | | | | | |
| $V_{IH}$ | High-level input voltage | SCK, SDI, CS# | | 1.4 | | 3.3 | V |
| $V_{IL}$ | Low-level input voltage | | | 0 | | 0.4 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = 5 mA | | 1.4 | | Vcc | V |
| | | $I_{OH}$ = 0.1 mA | | 2.2 | | Vcc | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 5 mA | | | | 0.45 | V |
| $I_{IH}$ | High-level input current | | | -42 | | 42 | uA |
| $I_{IL}$ | Low-level input current | | | –25 | | 25 | uA |

(1) Unless Otherwise Stated, $f_{CLKIN}$=6 GHz, CLK_MUX=Buffer, All clocks on with OUTx_PWR=7, SYSREFREQ_MODE=1
(2) For powered down mode, if the LOGISYSREFOUT field is set to LVPECL mode AND the LVPECL resistors are placed, this powerdown current increases to about 40 mA.

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## 6.6 Timing Requirements

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Timing Requirements** | | | | | | |
| $f_{SPI}$ | SPI Read/Write Speed | | | | 2 | MHz |
| $t_{CE}$ | Clock to enable low time | | | | 20 | ns |
| $t_{CS}$ | Clock to data wait time | | | | 20 | ns |
| $t_{CH}$ | Clock to data hold time | | | | 20 | ns |
| $t_{CWH}$ | Clock pulse width high | | | | 100 | ns |
| $t_{CWL}$ | Clock pulse width low | | | | 100 | ns |
| $t_{CES}$ | Enable to clock setup time | | | | 20 | ns |
| $t_{EWH}$ | Enable pulse width high | | | | 50 | ns |
| $t_{CD}$ | Falling clock edge to data wait time | | | | 100 | ns |

## 6.7 Timing Requirements

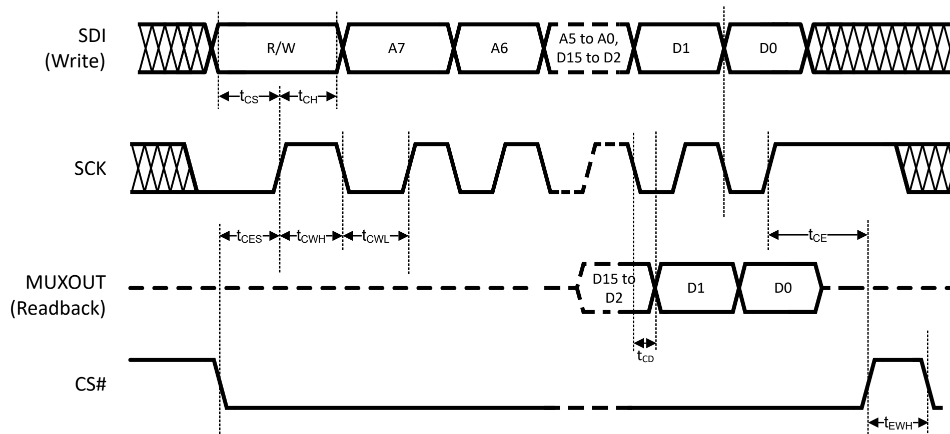


**Figure 6-1. Serial Data Input Timing Diagram**

There are several other considerations for writing on the SPI:

- The R/W bit must be set to 0.
- The data on SDI pin is clocked into a shift register on each rising edge on the SCK pin.
- The CS# must be held low for data to be clocked. Device will ignore clock pulses if CS# is held high.
- Recommended SPI settings for this device are CPOL=0 and CPHA=0.
- When SCK and SDI lines are shared between devices, TI recommends to hold the CS# line high on the device that is not to be clocked.

There are several other considerations for SPI readback:

- The R/W bit must be set to 1.
- The MUXOUT pin will always be low for the address portion of the transaction.
- The data on MUXOUT is clocked out at the falling edge of SCK. In other words, the readback data will be available at the MUXOUT pin $t_{CD}$ after the clock falling edge.
- The data portion of the transition on the SDI line is always ignored.
- The MUXOUT pin does not automatically tri-state after a readback transaction completes. When sharing the SPI bus readback pin with other devices, set MUXOUT_EN=0 after all readback transactions from device are complete to manually tri-state the MUXOUT pin, permitting other devices to control the readback line.


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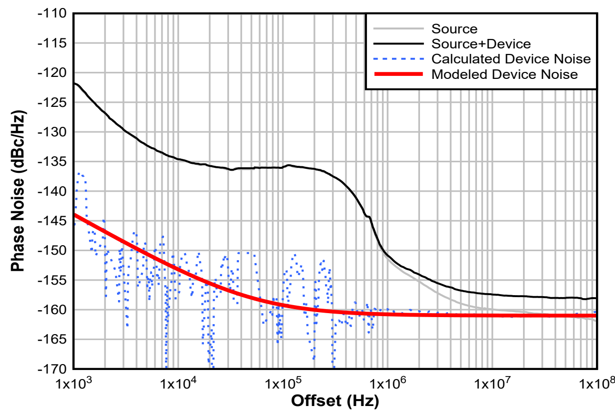
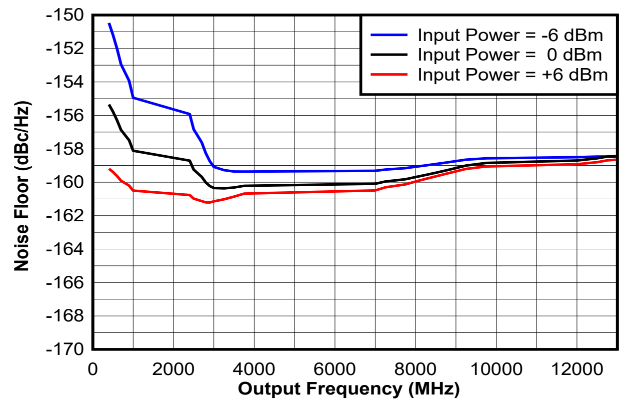
## 6.8 Typical Characteristics

If not otherwise, the following conditions can be assumed: Temperature = 25°C, Vcc = 2.5 V, OUTx_PWR=5, CLKIN driven differentially with 8 dBm at each pin. Signal source used was SMA100B with ultra-low noise option B711.



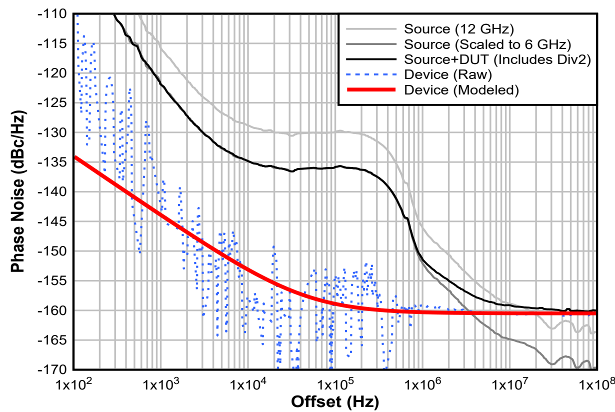

Noise Floor = –161 dBc/Hz, 1/f Noise = –154 dBc/Hz @ 10 kHz, Integrates to 28 fs jitter from 100 Hz to 6 GHz offset

**Figure 6-2. Buffer Phase Noise Plot at 6 GHz Output**



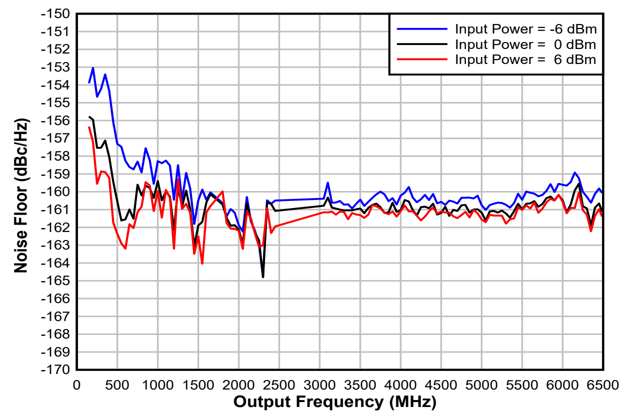

Stated input power is applied at each pin.

**Figure 6-3. Noise Floor in Buffer Mode**




Noise Floor = –160.5 dBc/Hz, 1/f Noise = –154 dBc/Hz @ 10 kHz, Integrates to 30 fs jitter from 100 Hz to 6 GHz offset

**Figure 6-4. Divide by 2 Phase Noise Plot at 6 GHz Output**




Stated input power is applied at each pin.

**Figure 6-5. Noise Floor with Divide by 2**

## 6.8 Typical Characteristics (continued)

If not otherwise, the following conditions can be assumed: Temperature = 25°C, Vcc = 2.5 V, OUTx_PWR=5, CLKIN driven differentially with 8 dBm at each pin. Signal source used was SMA100B with ultra-low noise option B711.

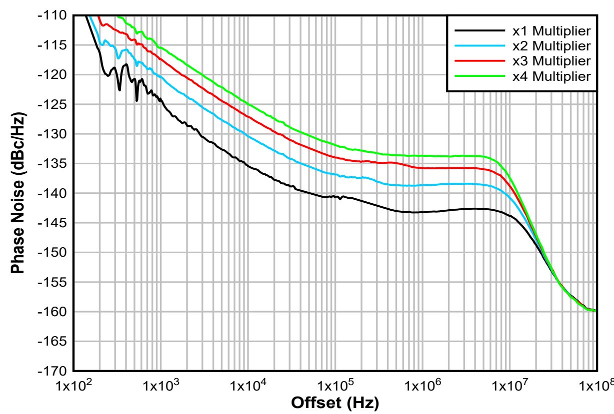
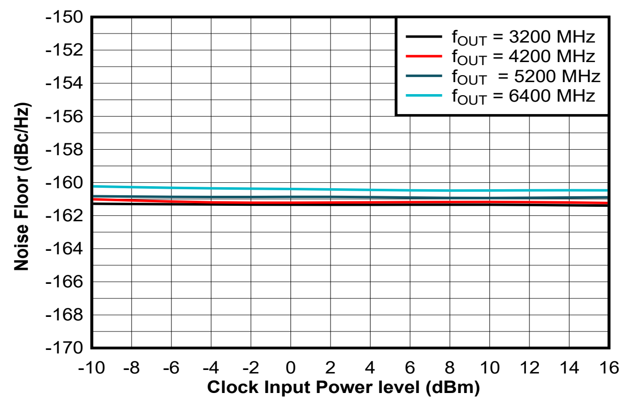



Figure 6-6. Multiplier Phase Noise Plot at 6 GHz Output




**Note**

Input power in graph is differential.

Figure 6-7. Noise Floor in Multiply x2 Mode

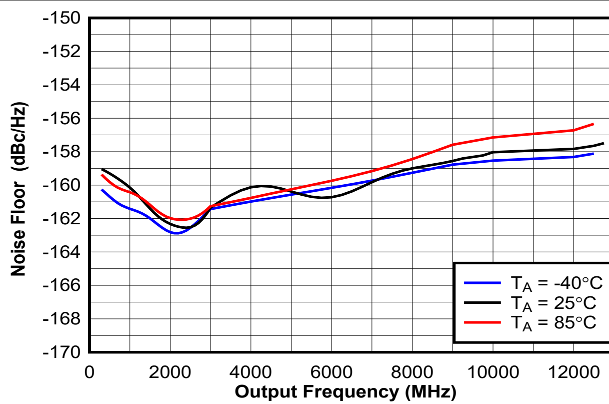



Figure 6-8. Noise Floor in Buffer Mode

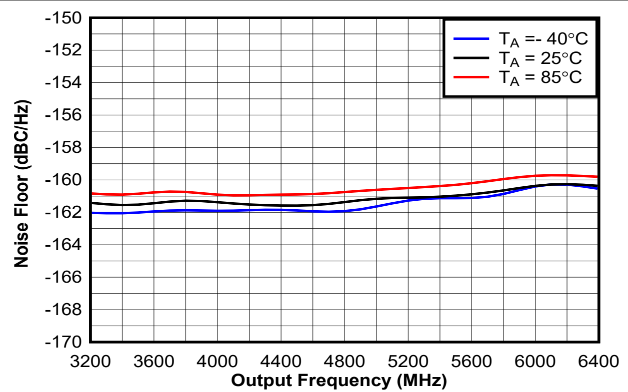



Figure 6-9. Noise Floor in x2 Multiplier Mode

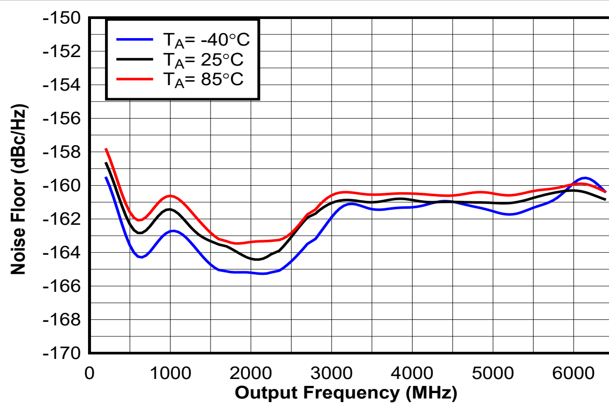



Figure 6-10. Noise Floor in Divide by 2 Mode

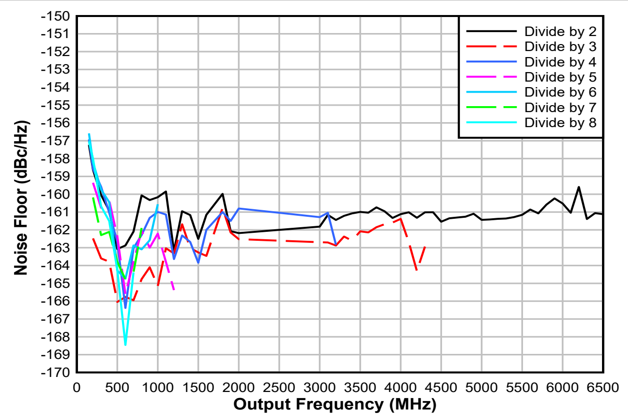



Figure 6-11. Noise Floor in Divider Mode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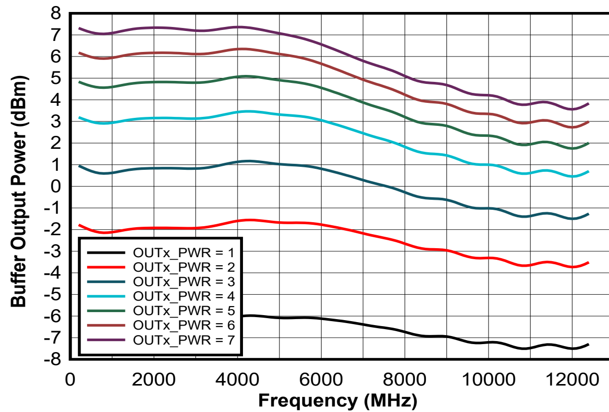
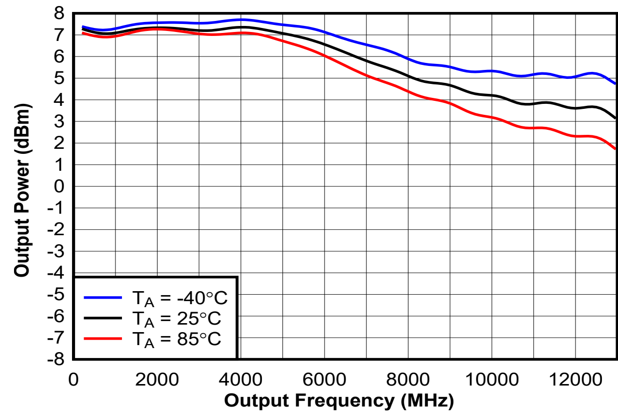
## 6.8 Typical Characteristics (continued)

If not otherwise, the following conditions can be assumed: Temperature = 25°C, Vcc = 2.5 V, OUTx_PWR=5, CLKIN driven differentially with 8 dBm at each pin. Signal source used was SMA100B with ultra-low noise option B711.



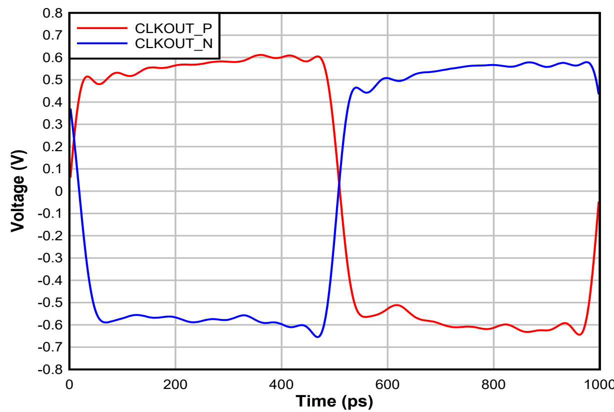

Applies to all modes except divider mode with odd divide (which will have slightly lower power).

**Figure 6-12. Single-Ended Output Power**




CLKOUTx_PWR = 7

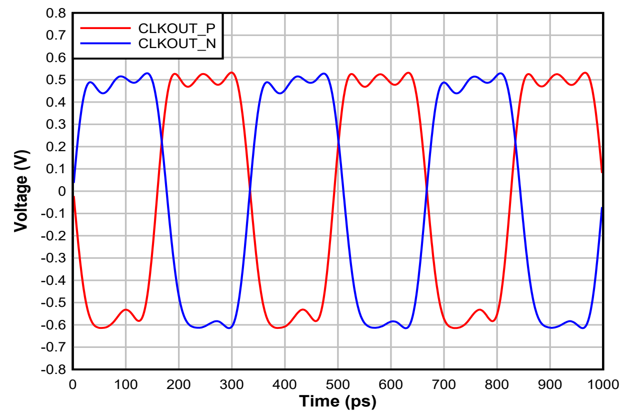
**Figure 6-13. Single-Ended Output Power**




**Note**

CLKOUTx_PWR=7

**Figure 6-14. CLKOUT Waveform at 1 GHz**




**Note**

CLKOUTx_PWR=7

**Figure 6-15. CLKOUT Waveform at 3 GHz**

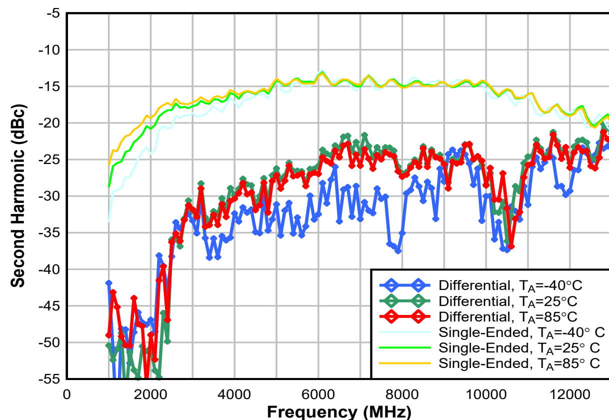



**Figure 6-16. Second Harmonic in Buffer Mode**

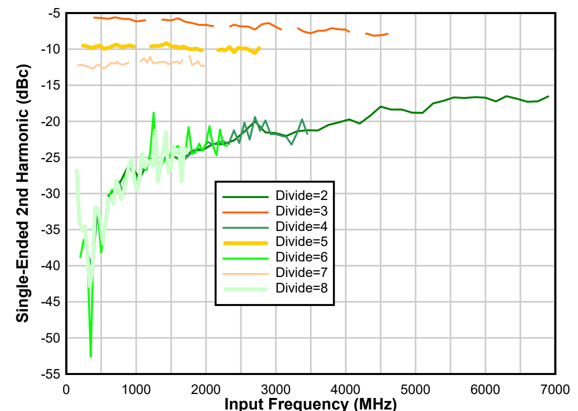



**Figure 6-17. Second Harmonic in Divide Mode (Single-Ended)**

## 6.8 Typical Characteristics (continued)

If not otherwise, the following conditions can be assumed: Temperature = 25°C, Vcc = 2.5 V, OUTx_PWR=5, CLKIN driven differentially with 8 dBm at each pin. Signal source used was SMA100B with ultra-low noise option B711.

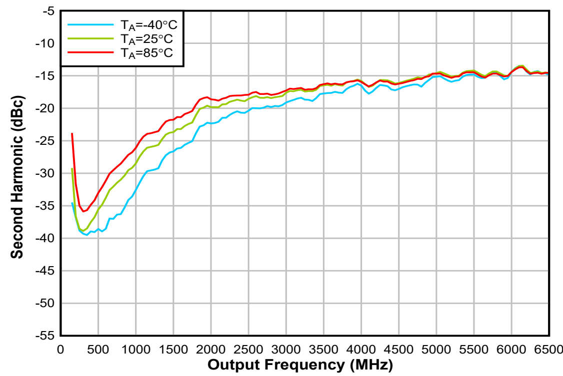



Figure 6-18. Second Harmonic in Divide by 2 Mode (Single-Ended)

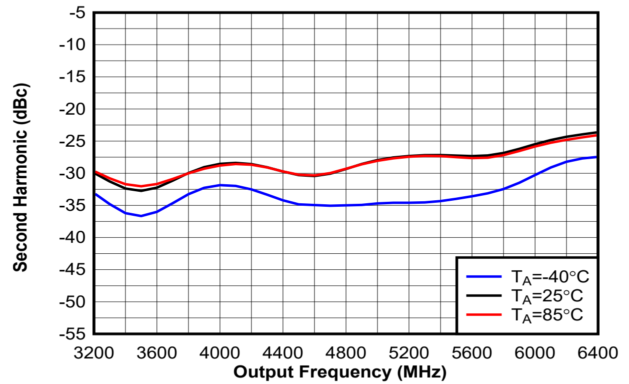
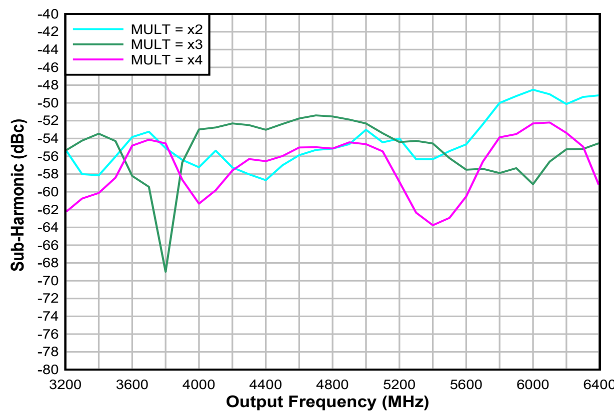



Figure 6-19. Second Harmonic in Multiply X2 Mode (Differential)




**Note**

Output is differential.

Figure 6-20. Multiplier Sub-Harmonics (Harmonic Frequency = Output Frequency / M )

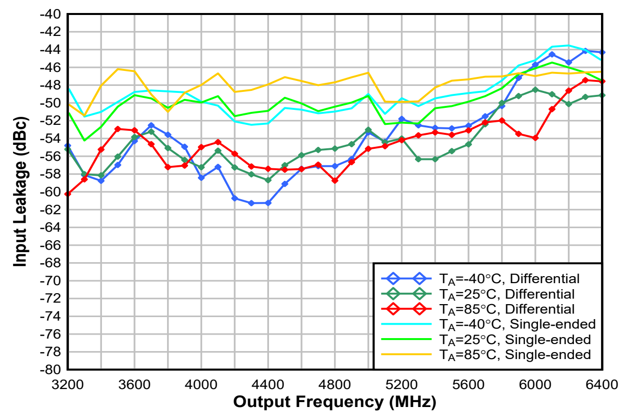



Figure 6-21. Multiplier 1/2 Sub-Harmonic in X2 Mode

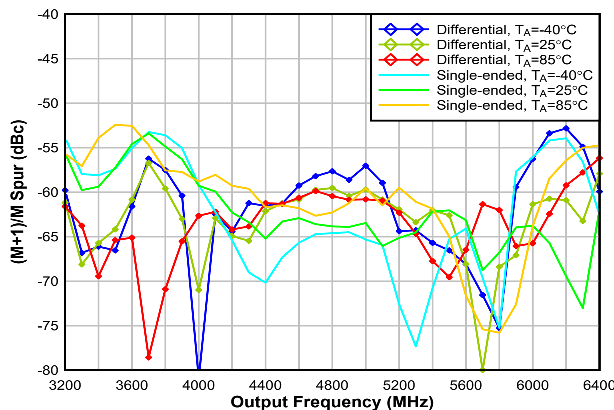



Figure 6-22. Multiplier Intermodulation Spur (MULT=2)

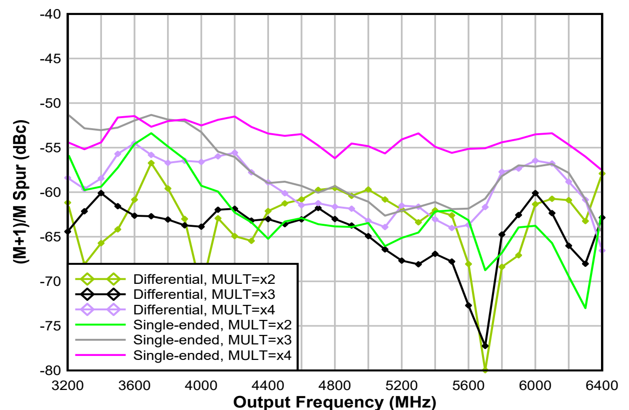



Figure 6-23. Multiplier Intermodulation (M+1)/M Spur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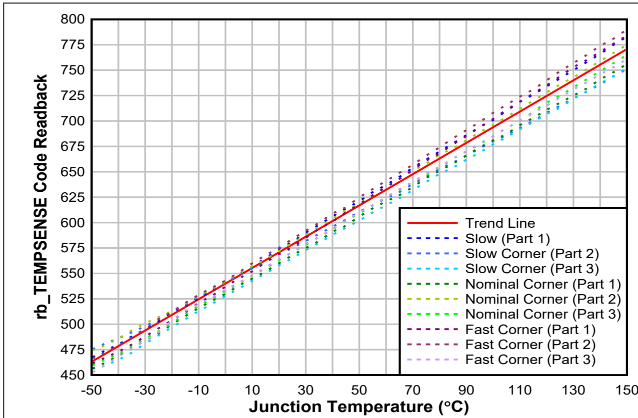
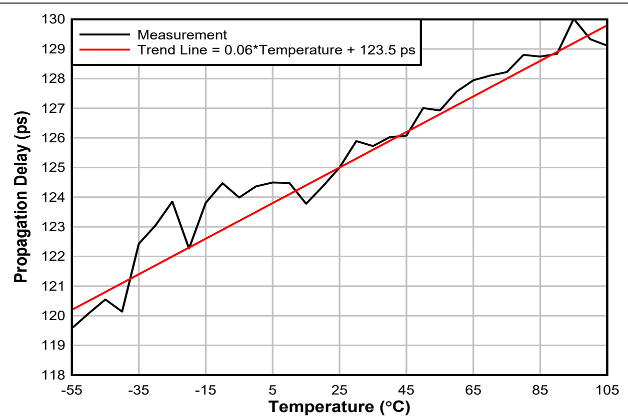
## 6.8 Typical Characteristics (continued)

If not otherwise, the following conditions can be assumed: Temperature = 25°C, Vcc = 2.5 V, OUTx_PWR=5, CLKIN driven differentially with 8 dBm at each pin. Signal source used was SMA100B with ultra-low noise option B711.




Measured in power-down mode to make Junction Temperature = Ambient temperature.

**Figure 6-24. Temperature Sensor Readback**




Over 30 devices and 3 corner lots, propagation delay was found to vary 1.1 ps over process and 7 ps overall when the temperature was held at a constant 25°C.

**Figure 6-25. Propagation Delay**

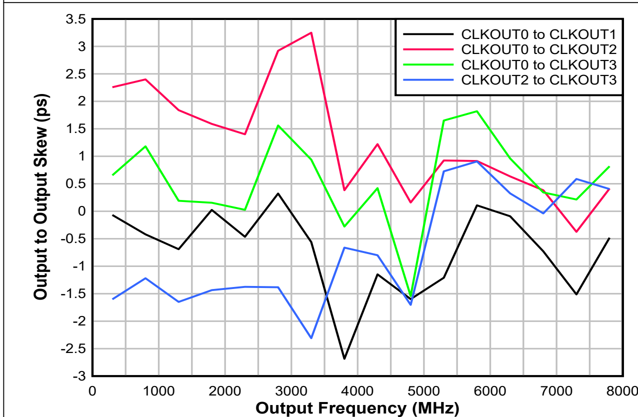
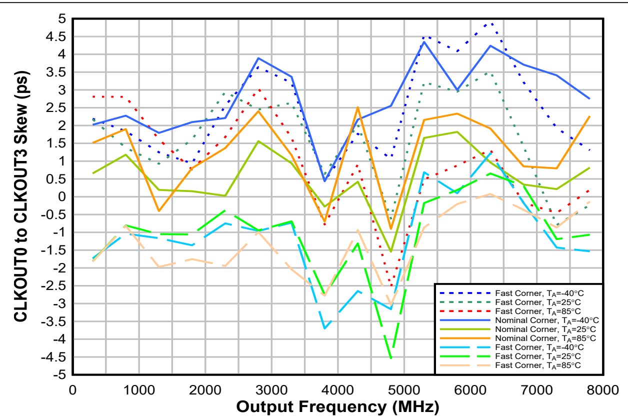



**Figure 6-26. Output to Output Skew**




Main source of skew variation is frequency and measurement error. Other observed sources of variation include about 3 ps over process corners and 1.5 ps over temperature.

**Figure 6-27. Output to Output Skew Variation for CLKOUT0 to CLKout3**

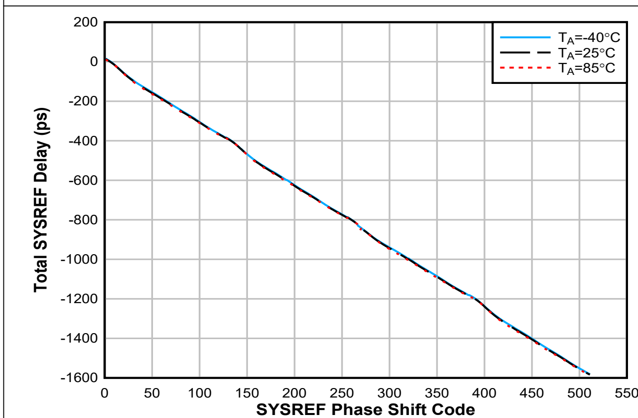



**Figure 6-28. SYSREF Delay vs. Temperature and Code (Fout = 10 GHz)**

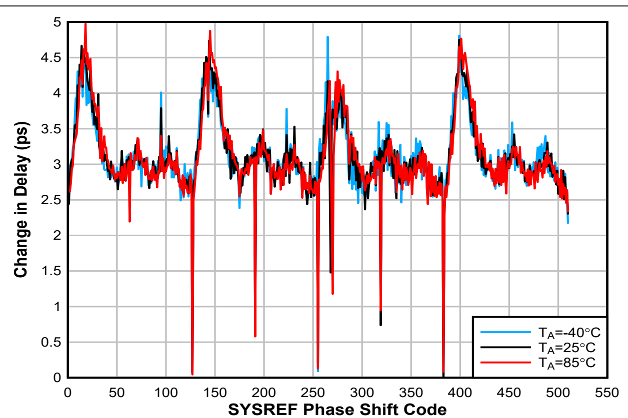



**Figure 6-29. SYSREF Delta Delay vs. Temperature and Code (Fout=10 GHz)**

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## 6.8 Typical Characteristics (continued)

If not otherwise, the following conditions can be assumed: Temperature = 25°C, Vcc = 2.5 V, OUTx_PWR=5, CLKIN driven differentially with 8 dBm at each pin. Signal source used was SMA100B with ultra-low noise option B711.

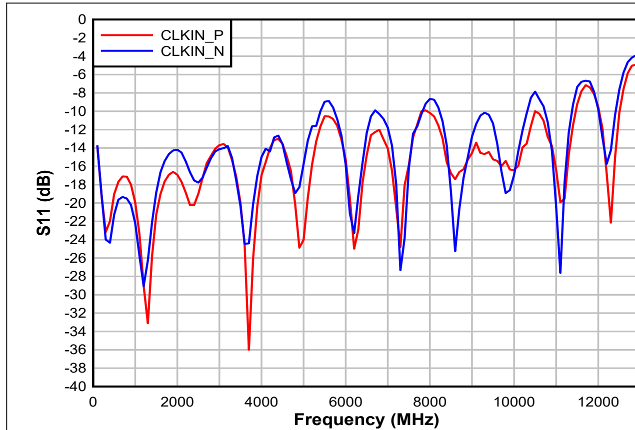


**Figure 6-30. CLKIN S11 Magnitude**

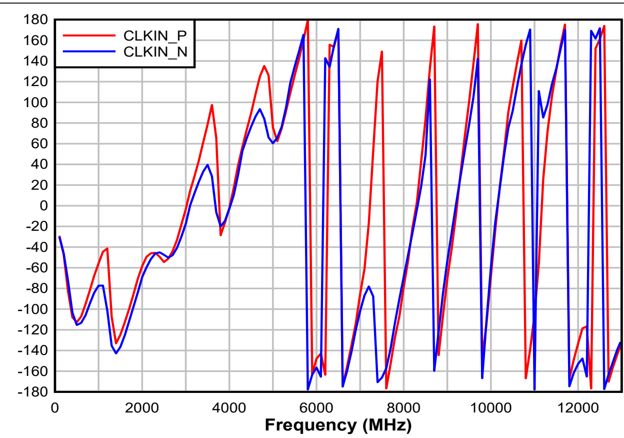


**Figure 6-31. CLKIN S11 Phase**


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# 7 Detailed Description

## 7.1 Overview

The LMX1204 has four main clock outputs and another LOGICLK output. The main clock outputs are all the same frequency. This frequency can be the same, divided, or multiplied relative to the input clock. Each of these clock outputs has programmable power level. The LOGICLK output frequency is independent and typically lower frequency than the other four main clocks and has programmable output format (CML, LVDS, LVPECL) and power level.

The SYSREF can be generated by either repeating the input from the SYSREFREQ pins, or internally generated. There is an internal SYSREF windowing feature that allows the internal timing of the device to be adjusted to optimize setup/hold times of the SYSREFREQ input with respect to the CLKIN input. This feature assumes that the delay between the SYSREF edge and the next rising clock edge is consistent. Each of the five outputs has a corresponding SYSREF output that has individual delays and programmable common mode. For the LOGISYSREF output, the output format is programmable as CML, LVDS, or LVPECL.

### 7.1.1 Range of Dividers and Multiplier

There are dividers that allow the main and LOGICLK outputs to be a divided value of the input clock. The main clock outputs also have a multiplier. In addition to this, dividers are used for SYSREF generation in generator mode as well as generation of the delay block.

**Table 7-1. Range of Dividers and Multiplier**

<table>
<tr><th colspan="3">CATEGORY</th><th>RANGE</th><th>COMMENTS</th></tr>
<tr><td rowspan="3">Main Clocks</td><td colspan="2">Buffer</td><td></td><td></td></tr>
<tr><td colspan="2">Divider</td><td>2, 3, 4, … 8</td><td>Odd divides (except 1) do not have 50% duty cycle</td></tr>
<tr><td colspan="2">Multiplier</td><td>1,2, 3, 4</td><td>x1 Multiplier and Filter mode are the same thing.</td></tr>
<tr><td rowspan="2">LOGICLK</td><td rowspan="2">Divide</td><td>PreDivide</td><td>1, 2, 4</td><td rowspan="2">TotalDivide = PreDivide × Divide<br>Odd divides (except 1) do not have 50% duty cycle</td></tr>
<tr><td>Divide</td><td>1, 2, 3, … 1023</td></tr>
<tr><td rowspan="3">SYSREF</td><td rowspan="2">Divide for frequency generation</td><td>PreDivide</td><td>1,2, 4</td><td rowspan="2">Pre-divides clock for phase interpolator.<br>TotalDivide = PreDivide×Divide<br>Odd divides do not have 50% duty cycle</td></tr>
<tr><td>Divide</td><td>2, 3, 4,… 4095</td></tr>
<tr><td>Divide for delay generation</td><td>Divide</td><td>2, 4, 8, 16</td><td>This divide is set according to the input frequency.</td></tr>
</table>

## 7.2 Functional Block Diagram

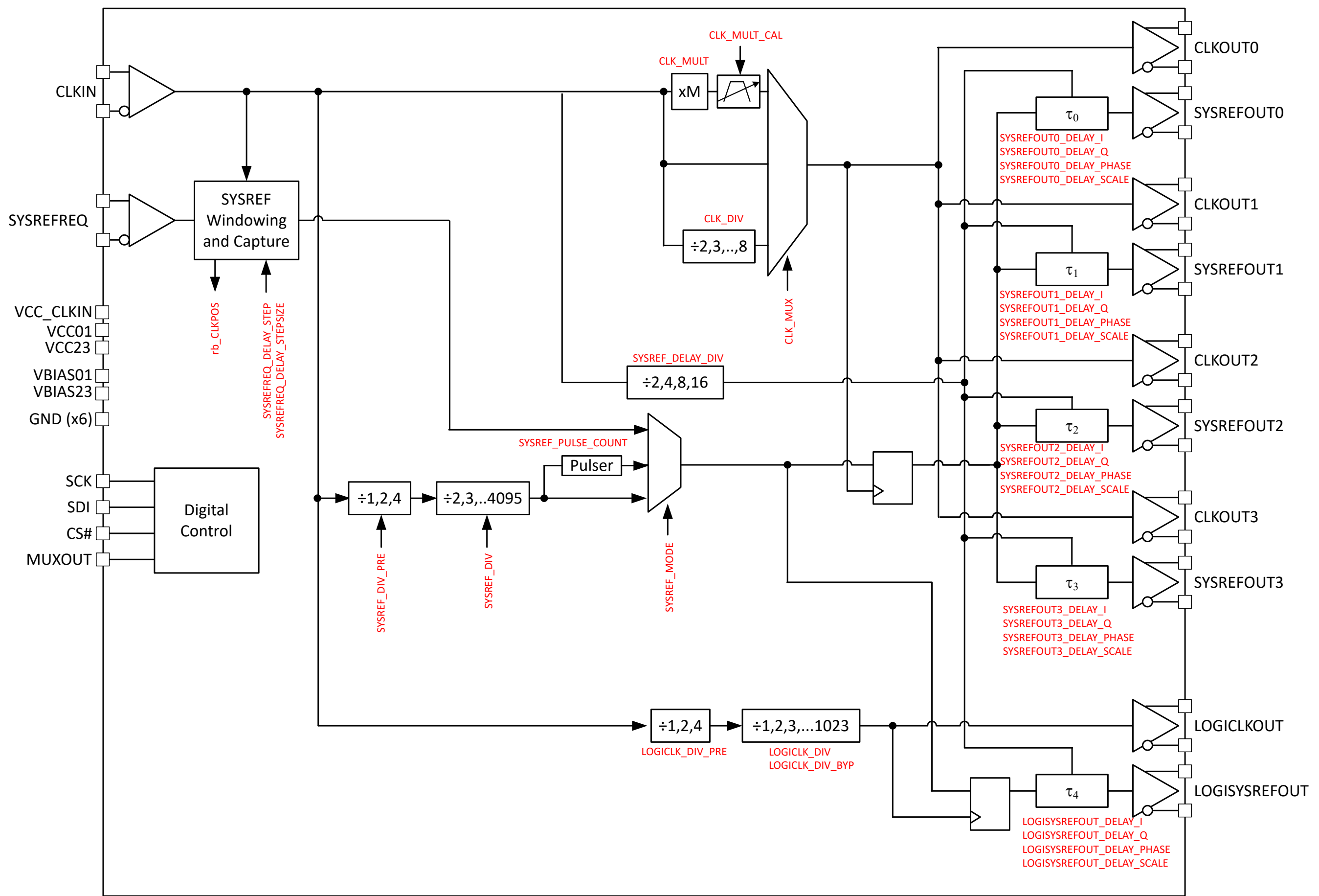


**Figure 7-1. Functional Block Diagram**


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## 7.3 Feature Description

### 7.3.1 Power On Reset

When the device is powered up, the power on reset (POR) resets all registers to a default state as well as resets all state machines and dividers. For the power on reset state, all SYSREF outputs are disabled and all the dividers are bypassed; the device performs as a 4-output buffer. One should wait 100 µs after the power supply rails before programming other registers to ensure that this RESET is finished. If the power on reset happens when there is no device clock present, it will function properly, however, the current will change once an input clock is presented.

It is also possible and generally good practice to do a software power on reset by writing RESET=1 in the SPI bus. The RESET bit will self-clear once any other register is written to. The SPI bus can be used to override these states to the desired settings.

Although the device does have an automatic power on reset, it can be impacted by different ramp rates on the different supply pins, especially in the presence of a strong input clock signal.. It is therefore recommended to do a software reset after POR. This can be done by programming RESET=1. The reset bit can be cleared by programming any other register or setting RESET back to zero. Even at maximum allowed SPI bus speed, the software reset event always completes before the subsequent SPI write.

### 7.3.2 Temperature Sensor

The junction temperature can be read back for purposes such as characterization or to make adjustments based on temperature. Such adjustments might include adjusting CLKOUTx_PWR to make the output power more stable or using external or digital delays to compensate for changes in propagation delay over temperature.

The junction temperature is typically higher than the ambient temperature due to power dissipation from the outputs and other functions on the device. Equation 1 shows the relationship between the code read back and the junction temperature.

$$\text{Temperature} = 0.65 \times \text{Code} - 351 \quad (1)$$

Equation 1 is based on a best-fit line created from three devices from slow, nominal, and fast corner lots (9 parts total),. The worst-case variation of the actual temperature from the temperature predicted by the best-fit line was 13°C, which works out to 20 codes.

### 7.3.3 Clock Outputs

This device has four main output clocks which share a common frequency. This does not include the additional lower frequency LOGICLK output.

#### *7.3.3.1 Clock Output Buffers*

The output buffers have a format that is open collector with an integrated pullup resistor, similar to CML.

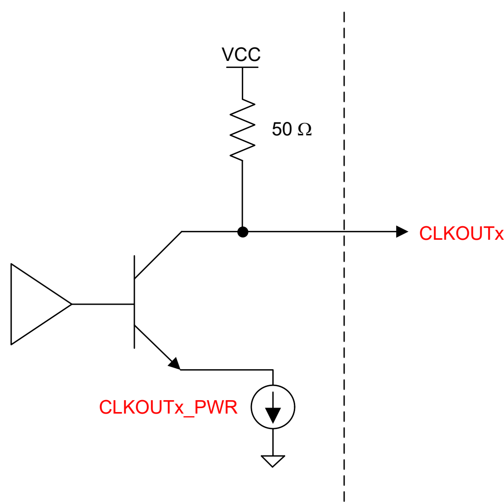


**Figure 7-2. CLKOUT Output Buffer**

The output buffers can be enabled with CLKOUTx_EN bits. In addition to this, their output power can be individually set with the CLKOUTx_PWR field. However, these fields only control the output buffer, not the internal channel path that drives this buffer, the SYSREF generator, or the SYSREF output. To power down the entire path, disable the CHx_EN bit.

**Table 7-2. Clock Output Power**

| CHx_EN | INTERNAL CHANNEL PATH | CLKOUTx_EN | CLKOUTx_PWR | OUTPUT BUFFER |
|---|---|---|---|---|
| 0 | Powered Down | Don't Care | Don't Care | Powered Down |
| 1 | Powered Up | 0 | Don't Care | Powered Down |
| | | 1 | 0 | Minimum |
| | | | 1 | |
| | | | ... | |
| | | | 7 | Maximum |

### 7.3.3.2 Clock MUX

The four main clocks must be the same frequency, but this frequency can be bypassed, multiplied, or divided. This is determined by the CLK_MUX word.

**Table 7-3. Clock MUX**

| CLK_MUX | OPTION | VALUES SUPPORTED |
|---|---|---|
| 0 | Buffer Mode | ÷1 (bypass) |
| 1 | Divider Mode | ÷2, 3, 4, 5, 6, 7, and 8 |
| 2 | Multiplier Mode | x1 (filter mode), x2, x3, x4 |

### 7.3.3.3 Clock Divider

Setting the CLK_MUX to Divided allows a divide value of 2, 3, 4, 5, 6, 7, and 8. This is set by the CLK_DIV word. When using the clock divider, any change to the input frequency requires the CLK_DIV_RST bit to be toggled from 1 to 0.

**Table 7-4. Clock Divider**

| CLK_DIV | DIVIDE | DUTY CYCLE |
|---|---|---|
| 0 | Reserved | n/a |
| 1 | 2 | 50% |
| 2 | 3 | 33% |


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**Table 7-4. Clock Divider (continued)**

| CLK_DIV | DIVIDE | DUTY CYCLE |
|---|---|---|
| 3 | 4 | 50% |
| 4 | 5 | 40% |
| 5 | 6 | 50% |
| 6 | 7 | 43% |
| 7 | 8 | 50% |

#### *7.3.3.4 Clock Multiplier and Filter Modes*

##### General Information about the Clock Multiplier

The clock multiplier is can be used to multiply up the input clock frequency by a factor of x1, x2, x3, or x4. The multiply value is set by the CLK_MULT field. As the multiplier is PLL-based and includes an integrated VCO, it has a state machine clock, requires calibration, has a lock detect feature, and can be used as a tunable filter. Note that if the multiplier is not being used, there is no need for the state machine clock or the lock detect feature.

##### State Machine Clock for the Clock Multiplier

The state machine clock frequency ,$f_{SMCLK}$, is derived by dividing down the input clock frequency by a programmed divider value. The state machine clock is also necessary for the multiplier calibration and lock detect. If there are concerns about the state machine clock creating spurs, then it can be shut off provided that the multiplier calibration is not running and the lock detect feature is not being used.

##### Calibration for the Clock Multiplier

For optimal phase noise, the VCO in the multiplier divides up the frequency range into many different bands and cores and has optimized amplitude settings for each one of these. For this reason, upon initial use, or whenever the frequency is changed, a calibration routine needs to be run in order to determine the correct core, frequency band, and amplitude setting. Calibration is performed by programming the R0 register with a valid input signal. Increasing the speed of the state machine clock speeds up the multiplier calibration time. To ensure reliable multiplier calibration, the state machine clock frequency needs to be at least twice the SPI write speed, but no more than 30 MHz. Whenever the CLK_MUX mode is changed or the multiplier is calibrated for the first time, the calibration time will be substantially longer, on the order of 5 ms.

##### Using the x1 Clock Multiplier as a Filter

As the multiplier is PLL based, it acts as a programmable filter that attenuates noise, spurs, harmonics, and sub-harmonics that are outside the PLL loop bandwidth (about 10 MHz). In some situations, one may want to filter the clock without multiplying this up. Filter mode (x1 multiplier) allows one to use the clock multiplier as a tunable filter with 10 MHz bandwidth that has lower additive noise than the higher multiply values. In this filter mode, spurs of lower offsets tend to get amplified by the multiplier, so it is typically most effective for spurs that are 100 MHz or farther offset from the carrier where the multiplier PLL loop filter is able to roll these spurs off. Note that filter mode is different than buffer mode in that it filters the input frequency, but adds more close in phase noise.

##### Lock Detect for the Clock Multiplier

The lock detect status of the multiplier can be read back through the rb_LD field or from the MUXOUT pin. The state machine clock must be running for the lock detect to work properly. Lock detect is not supported in x1 (filter) mode.

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#### 7.3.3.4.1 State Machine Clock

If not using the clock multiplier, the state machine clock should be disabled by setting SMCLK_EN=0 to minimize crosstalk and spurs. However, when using the clock multiplier, the state machine clock is required to run the calibration engine when the frequency is changed and also used to have the lock detect continuously monitor if the PLL-based clock multiplier is in lock. The state machine clock must be less than 30 MHz. Consult the register map document for more details.

### 7.3.4 LOGICLK Output

The LOGICLK output can be used to drive devices using lower frequency clocks, such as FPGAs. It has programmable output format and a corresponding SYSREF output.

#### *7.3.4.1 LOGICLK Output Format*

The LOGICLK output format can be programmed to LVDS, LVPECL, and CML modes. Depending on the format, the common mode may be programmable or external components may be required (see Table 7-5).

**Table 7-5. LOGICLK Formats and Properties**

| LOGICLKOUT_FMT | FORMAT | EXTERNAL COMPONENTS REQUIRED | OUTPUT LEVEL | COMMON MODE |
|---|---|---|---|---|
| 0 | LVDS | None | Fixed | Programmable through LOGICLKOUT_VCM |
| 1 | LVPECL | Emitter Resistors | Fixed | Not programmable |
| 2 | CML | Pullup Resistors 50 Ω to $V_{CC}$ | Programmable through LOGICLKOUT_PWR | Not programmable |
| 3 | Invalid | | | |

#### *7.3.4.2 LOGICLK_DIV_PRE and LOGICLK_DIV Dividers*

The LOGICLK_DIV_PRE divider and LOGICLK_DIV dividers are used for the LOGICLK output. The LOGICLK_DIV_PRE divider is necessary to divide the frequency down to ensure that the input to the LOGICLK_DIV divider is 3.2 GHz or less. When LOGICLK_DIV is not even and not bypassed, the duty cycle will not be 50%. Both the LOGICLK dividers are synchronized by the SYNC feature, which allows synchronization across multiple devices.

**Table 7-6. Minimum N-Divider Restrictions**

| $f_{CLKIN}$ (MHz) | LOGICLK_DIV_PRE | LOGICLK_DIV | TOTAL DIVIDE RANGE |
|---|---|---|---|
| $f_{CLKIN}$ ≤ 3.2 GHz | ÷1,2,4 | ÷1,2 ,3 ,…1023 | [1, 2, ...1023]<br>[2, 4, ... 2046]<br>[4, 8, 4092] |
| 3.2 GHz < $f_{CLKIN}$≤ 6.4 GHz | ÷2,4 | ÷1, 2 ,3 ,…1023 | [4, ... 2046]<br>[4, 8, 4092] |
| $f_{CLKIN}$ > 6.4 GHz | ÷4 | 1, 2, 3 ,…1023 | [8, 4092] |

### 7.3.5 SYSREF

SYSREF allows a low frequency JESD204B/C compliant signal to be produced that is reclocked to a main or LOGICLK output. The delays between the CLKOUT and SYSREF outputs are adjustable with software. The SYSREF output can be configured as a generator using the internal SYSREF divider, or as a repeater duplicating the signal on the SYSREFREQ pins. The SYSREF generator for both the main clocks and the LOGICLK output are the same.

#### *7.3.5.1 SYSREF Output Buffers*

##### 7.3.5.1.1 SYSREF Output Buffers for Main Clocks (SYSREFOUT)

The SYSREF outputs within the clock output channels have the same output buffer structure as the clock output buffer, with the addition of circuitry to adjust the common-mode voltage. The SYSREF outputs are CML outputs with a common-mode voltage that can be adjusted with the SYSREFOUTx_VCM field, and the output level that can be programmed with the SYSREFOUTx_PWR field. This is to allow DC coupling. Note that the


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CLKOUT outputs do not have adjustable common-mode voltage and must be AC coupled; this is for optimal noise performance.

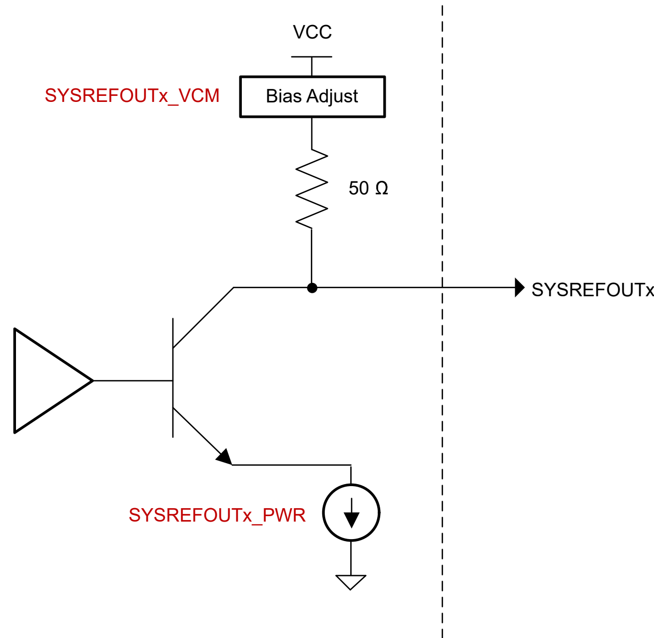


**Figure 7-3. SYSREF Output Buffer**

The common-mode voltage and output power are interrelated and can be simulated assuming a 100-Ω differential load and no DC path to ground. The common mode voltage and output are interrelated as shown in Table 7-7. Realize that for reasons of long-term reliability reasons it is required that $V_{CM}$ - $V_{OD}/2 \geq 0.5$ V.

**Table 7-7. Single-Ended Voltage ($V_{OD}$) and Common Mode Voltage ($V_{CM}$)**

| SYSREFOUT_PWR | Check: $V_{CM}$ - $V_{OL}/2 \geq 0.5$ V. ? | SYSREFOUT_VCM | $V_{OD}$ | $V_{CM}$ |
|---|---|---|---|---|
| 0 | Valid State | 0 | 0.22 | 1.22 |
| | | 1 | 0.22 | 1.34 |
| | | 2 | 0.22 | 1.48 |
| | | 3 | 0.22 | 1.63 |
| | | 4 | 0.22 | 1.77 |
| | | 5 | 0.23 | 1.91 |
| | | 6 | 0.23 | 2.06 |
| | | 7 | 0.23 | 2.20 |
| 1 | | 0 | 0.27 | 0.94 |
| | | 1 | 0.27 | 1.08 |
| | | 2 | 0.27 | 1.25 |
| | | 3 | 0.27 | 1.44 |
| | | 4 | 0.28 | 1.61 |
| | | 5 | 0.28 | 1.78 |
| | | 6 | 0.28 | 1.96 |
| | | 7 | 0.29 | 2.13 |
| 2 | | 0 | 0.32 | 0.70 |
| | | 1 | 0.32 | 0.83 |
| | | 2 | 0.32 | 1.03 |
| | | 3 | 0.33 | 1.25 |
| | | 4 | 0.33 | 1.45 |
| | | 5 | 0.33 | 1.64 |
| | | 6 | 0.34 | 1.86 |
| | | 7 | 0.34 | 2.06 |
| 3 | Invalid State | 0 | 0.36 | 0.55 |
| | | 1 | 0.37 | 0.66 |
| | Valid State | 2 | 0.37 | 0.82 |
| | | 3 | 0.38 | 1.07 |
| | | 4 | 0.38 | 1.30 |
| | | 5 | 0.38 | 1.52 |
| | | 6 | 0.39 | 1.77 |
| | | 7 | 0.39 | 2.00 |
| 4 | Invalid State | 0 | 0.40 | 0.44 |
| | | 1 | 0.41 | 0.53 |
| | | 2 | 0.42 | 0.68 |
| | Valid State | 3 | 0.42 | 0.89 |
| | | 4 | 0.43 | 1.15 |
| | | 5 | 0.44 | 1.39 |
| | | 6 | 0.44 | 1.67 |
| | | 7 | 0.45 | 1.93 |


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**Table 7-7. Single-Ended Voltage ($V_{OD}$) and Common Mode Voltage ($V_{CM}$) (continued)**

| SYSREFOUT_PWR | Check: $V_{CM}$ - $V_{OL}/2 \geq 0.5$ V. ? | SYSREFOUT_VCM | $V_{OD}$ | $V_{CM}$ |
|---|---|---|---|---|
| 5 | Invalid State | 0 | 0.41 | 0.40 |
| | | 1 | 0.44 | 0.45 |
| | | 2 | 0.46 | 0.57 |
| | Valid State | 3 | 0.47 | 0.76 |
| | | 4 | 0.48 | 1.00 |
| | | 5 | 0.49 | 1.27 |
| | | 6 | 0.49 | 1.58 |
| | | 7 | 0.50 | 1.87 |
| 6 | Invalid State | 0 | 0.42 | 0.38 |
| | | 1 | 0.45 | 0.42 |
| | | 2 | 0.50 | 0.49 |
| | | 3 | 0.52 | 0.66 |
| | | 4 | 0.53 | 0.86 |
| | Valid State | 5 | 0.54 | 1.15 |
| | | 6 | 0.54 | 1.49 |
| | | 7 | 0.55 | 1.81 |
| 7 | Invalid State | 0 | 0.42 | 0.36 |
| | | 1 | 0.46 | 0.40 |
| | | 2 | 0.51 | 0.45 |
| | | 3 | 0.56 | 0.58 |
| | | 4 | 0.57 | 0.77 |
| | Valid State | 5 | 0.58 | 1.03 |
| | | 6 | 0.60 | 1.40 |
| | | 7 | 0.61 | 1.75 |

#### 7.3.5.1.2 SYSREF Output Buffer for LOGICLK

The LOGISYSREFOUT output supports the three formats of LVDS, LVPECL, and CML. The LOGISYSREFOUT_EN enables the output buffer and LOGISYSREF_FMT sets the format. LVDS mode allows programmable common mode, LVPECL and CML require external components, and CML allows programmable output power (see Table 7-8).

**Table 7-8. LOGISYSREFOUT Output Buffer Configuration**

| LOGISYSREFOUT_EN | LOGISYSREF_FMT | LOGISYSREF FORMAT | EXTERNAL TERMINIATION REQUIRED | OUTPUT POWER | OUTPUT COMMON MODE |
|---|---|---|---|---|---|
| 0 | Powered Down | | | | |
| 1 | 0 | LVDS | None | Fixed | Programmable with LOGISYSREF_VCM |
| | 1 | LVPECL | Emitter Resistors | Fixed | Fixed |
| | 2 | CML | Pullup resistors 50 Ω to $V_{CC}$ | Controlled by LOGISYSREF_PWR | LOGISYSREF_VCM has no impact, but this changes with LOGISYSREF_PWR. |
| | 3 | Reserved | | | |

### *7.3.5.2 SYSREF Frequency and Delay Generation*

The SYSREF circuitry can produce an output signal that is synchronized to $f_{CLKIN}$. This output can be a single pulse, series of pulses, or a continuous stream of pulses. In generator mode, the SYSREF_DIV_PRE and

SYSREF_DIV values are used to divide the CLKIN frequency to a lower frequency that is reclocked to the output. In repeater mode, this signal is instead input at the SYSREFREQ pins. For each of the outputs, there is an independent delay control.

**Table 7-9. SYSREF Modes**

| SYSREF_MODE | DESCRIPTION |
|---|---|
| 0 | **Generator Mode (Continuous)**<br>Internal generator creates a continuous stream of SYSREF pulses. The SYSREFREQ pins or the SYSREFREQ_SPI field can be used to gate the SYSREF divider from the channels for improved noise isolation without disrupting the synchronization of the SYSREF dividers. The SYSREFREQ pins or the SYSREFREQ_SPI field must be high for a SYSREF output to come out. |
| 1 | **Generator Mode (Pulser)**<br>Internal generator generates a burst of 1 - 16 pulses that is set by SYSREF_PULSE_COUNT that occurs after a rising edge on the SYSREFREQ pins |
| 2 | **Repeater Mode**<br>SYSREFREQ pins are reclocked to clock outputs and then delayed in accordance to the SYSREF_DELAY_BYPASS field before being sent to the SYSREFOUT outputs. |

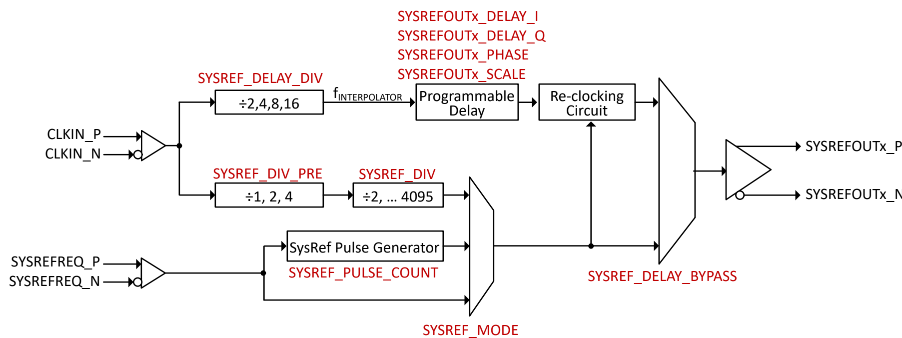


**Figure 7-4. SYSREF Generator Diagram**

For the frequency of the SYSREF output in generator mode, the SYSREF_DIV_PRE divider is necessary to ensure that the input of the SYSREF_DIV divider is not more than 3.2 GHz.

**Table 7-10. SYSREF_DIV_PRE Setup**

| $f_{CLKIN}$ | SYSREF_DIV_PRE | TOTAL SYSREF DIVIDE RANGE |
|---|---|---|
| 3.2 GHz or Less | ÷1, 2, or 4 | ÷2,3,4,...16380 |
| 3.2 GHz < $f_{CLKIN}$ ≤ 6.4 GHz | ÷2 or 4 | ÷4,6,8, … 16380 |
| $f_{CLKIN}$ > 6.4 GHz | ÷4 | ÷8,12,16, … 16380 |

For the delay, the input clock frequency is divided by SYSREF_DELAY_DIV to generate $f_{INTERPOLATOR}$. This has a restricted range as shown in Table 7-11. Note also that when SYSREF_DELAY_BYPASS=0 or 2 (delaygen engaged for generator mode), and SYSREF_MODE = 0 or 1 (a generator mode) the SYSREF output frequency must be a multiple of the phase interpolator frequency.

$f_{INTERPOLATOR} \% f_{SYSREF} = 0$.

**Table 7-11. SYSREF Delay Setup**

| $f_{CLKIN}$ | SYSREF_DELAY_DIV | SYSREFx_DELAY_SCALE | $f_{INTERPOLATOR}$ |
|---|---|---|---|
| 6.4 GHz < $f_{CLKIN}$ ≤ 12.8GHz | 16 | 0 | 0.4 to 0.8 GHz |
| 3.2 GHz < $f_{CLKIN}$ ≤ 6.4 GHz | 8 | 0 | 0.4 to 0.8 GHz |
| 1.6 GHz < $f_{CLKIN}$ ≤ 3.2 GHz | 4 | 0 | 0.4 to 0.8 GHz |
| 0.8 GHz < $f_{CLKIN}$ ≤1.6 GHz | 2 | 0 | 0.4 to 0.8 GHz |
| 0.4 GHz < $f_{CLKIN}$ ≤ 0.8 GHz | 2 | 1 | 0.2 to 0.4 GHz |


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**Table 7-11. SYSREF Delay Setup (continued)**

| $f_{CLKIN}$ | SYSREF_DELAY_DIV | SYSREFx_DELAY_SCALE | $f_{INTERPOLATOR}$ |
|---|---|---|---|
| 0.3 GHz < $f_{CLKIN}$ ≤ 0.4 GHz | 2 | 2 | 0.15 to 0.2 GHz |

The maximum delay is equal to the phase interpolator period and there are 4x127 = 508 different delay steps. Use Equation 2 to calculate the size of each step.

$$DelayStepSize = 1/( f_{INTERPOLATOR} \times 508) = SYSREF_DELAY_DIV/( f_{CLKIN} \times 508) \quad (2)$$

Use Equation 3 to calculate the total delay.

$$TotalDelay=DelayStepSize \times StepNumber \quad (3)$$

Table 7-12 shows the number of steps for each delay.

**Table 7-12. Calculation of StepNumber**

| SYSREFx_DELAY_PHASE | STEPNUMBER |
|---|---|
| 3 | 127 - SYSREFx_DELAY_I |
| 2 | 254 - SYSREFx_DELAY_Q |
| 0 | 381 - SYSREFx_DELAY_I |
| 1 | 508 - SYSREFx_DELAY_Q |

The SYSREF_DELAY_BYPASS field selects between the delay generator output and the repeater mode bypass signal. When SYSREF_MODE is set to continuous or pulser mode, TI recommends to set SYSREF_DELAY_BYPASS to generator mode. If SYSREF_MODE is set to repeater mode, TI recommends to set SYSREF_DELAY_BYPASS to bypass mode.

#### *7.3.5.3 SYSREFREQ pins and SYSREFREQ_SPI Field*

The SYSREFREQ pins are multipurpose and can be used for SYNC, SYSREF requests, and SYSREF Windowing. These pins can be DC or AC coupled and have dual 50-Ω, single-ended termination with programmable common-mode support.

In addition to these pins, the SYSREFREQ_SPI field can be set to 1 to emulate the same effect as forcing these pins high, simplifying hardware in some cases.

##### 7.3.5.3.1 SYSREFREQ Pins Common-Mode Voltage

The SYSREFREQ_P and SYSREFREQ_N pins can be driven either AC or DC coupled. When driven AC coupled, the common-mode voltage can be adjusted with the SRREQ_VCM bit.

**Table 7-13. SYSREFREQ Pin Common-Mode Voltage**

| SRREQ_VCM | COMMON-MODE VOLTAGE |
|---|---|
| 0 | 1.3 V AC-coupled |
| 1 | 1.1 V AC-coupled |
| 2 | 1.5 V AC-coupled |
| 3 | No Bias (DC Coupled) |

##### 7.3.5.3.2 SYSREFREQ Pin Windowing Feature

The SYSREF windowing can be used to internally calibrate the timing between the SYSREFREQ and CLKIN pins in order to optimize setup and hold timing and trim out any mismatches between SYSREFREQ and CLKIN paths. This feature requires that the timing from the SYSREFREQ rising edge to the CLKIN rising edge is consistent. The timing from the SYSREFREQ rising edge to the CLKIN rising edges can be tracked with the rb_CLKPOS field. Once the timing to the rising edge of the CLKIN pin is found, then the SYSREFREQ rising edge can be internally adjusted with the SYSREFREQ_DELAY_STEP and SYSREF_DELAY_STEPSIZE fields to optimize setup/hold times.

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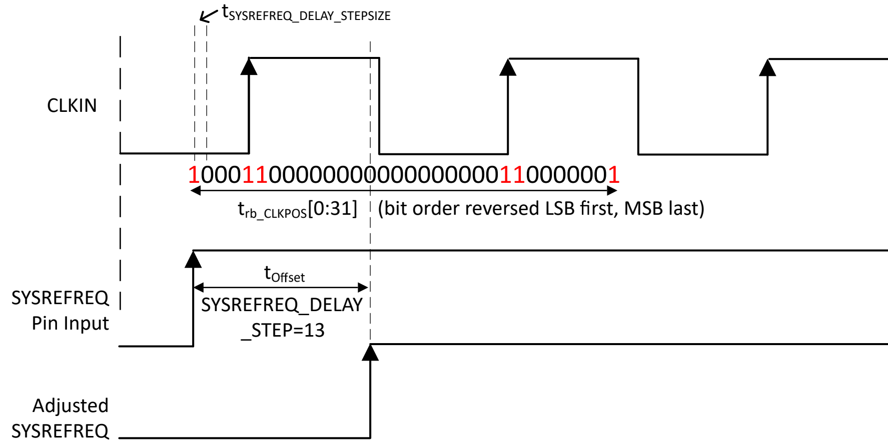


**Figure 7-5. SYSREFREQ Internal Timing Adjustment**

### General Procedure

- While programming the windowing feature for the first time, SYSREFREQ needs to be low.
- Set CLKPOS_CAPTURE_EN=1
- Set SYSREFREQ_DELAY_STEPSIZE according to Table 7-14. If the input frequency is at the boundary of two possible settings, it is recommended to choose the lowest one for optimal temperature stability.
- Program SYSREFREQ_CLR=1 and then SYSREFREQ_CLR=0
- Send a rising edge to the SYSREFREQ pin(s)
- Read back position with rb_CLKPOS field to determine timing from the SYSREFREQ rising edge to the next CLKIN rising edge. The number of 0's between the LSB '1' bit and the first series of '11' can be multiplied by the delay determined by SYSREFREQ_DELAY_STEPSIZE to determine the approximate timing to the first rising clock edge.
- Program SYSREFREQ_DELAY_STEP field in delay steps to maximize margin between left and right rising edges of CLKIN

**Table 7-14. SYSREFREQ_DELAY_STEPSIZE**

| INPUT FREQUENCY | RECOMMENDED SYSREFREQ_DELAY_STEPSIZE | DELAY (ps) |
|---|---|---|
| 1.4GHz < $f_{CLKIN}$ ≤ 2.7 GHz | 0 | 28 |
| 2.4 GHz < $f_{CLKIN}$ ≤ 4.7 GHz | 1 | 15 |
| 3.1 GHz < $f_{CLKIN}$ ≤ 5.7 GHz | 2 | 11 |
| $f_{CLKIN}$ ≥ 4.5 GHz | 3 | 8 |

### For glitch-free output

- Keep the same state for the SYSREFREQ pin when switching from request mode to windowing mode and back to request mode. For example, if the SYSREFREQ pin is high (or low) when windowing mode starts, make sure the pin state is high (or low) again after windowing mode ends before programing CLKPOS_CAPTURE_EN.
- The SYSREFREQ pin must be set low when switching from or to SYNC mode.

### Other pointers with SYSREF windowing

- The SYSREFREQ pins need to be held high for a minimum time of $3/f_{CLKIN}$ + 1.6 ns and only after this time rb_CLKPOS field is valid.
- If the user infers multiple valid SYSREFREQ_DELAY_STEP values from rb_CLKPOS registers to avoid setup-hold violations, choosing the lowest valid SYSREFREQ_DELAY_STEP is recommended to minimize variation over temperature.


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**If using SYNC feature**

- Only one SYSREFREQ pin rising edge is permitted per 75 input clock cycles
- SYSREFREQ has to stay high for >6 clock cycles

#### *7.3.5.4 SYNC Feature*

The SYNC feature allows the user to synchronize the CLK_DIV, LOGICLK_DIV, LOGICLK_DIV_PRE, SYSREF_DIV, SYSREF_DIV_PRE, and SYSREF_DELAY_DIV dividers so that the phase offset can be made consistent between power cycles. This allows multiple devices to be synchronized. This synchronization dividers can only be done through the SYSREFREQ pin, not the software.

## 7.4 Device Functional Modes

Table 7-15 shows the different modes for the device. The CLK_MUX field allows the user to configure the device as a buffer, divider, or multiplier. The SYSREF can also be enabled as well for applications that need this feature.

**Table 7-15. Device Configurations**

<table>
<tr><th>CLK_MUX</th><th>CLK_MULT</th><th>SYSREF_EN</th><th>FUNCTIONAL MODE</th></tr>
<tr><td rowspan="2">1</td><td rowspan="2">x</td><td>0</td><td>Buffer</td></tr>
<tr><td>1</td><td>Buffer w/SYSREF</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">x</td><td>0</td><td>Divider</td></tr>
<tr><td>1</td><td>Divider w/SYSREF</td></tr>
<tr><td rowspan="4">3</td><td rowspan="2">1</td><td>0</td><td>Filter</td></tr>
<tr><td>1</td><td>Filter w/SYSREF</td></tr>
<tr><td rowspan="2">2,3,4</td><td>0</td><td>Multiplier</td></tr>
<tr><td>1</td><td>Multiplier w/SYSREF</td></tr>
</table>

# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Applications Information

### 8.1.1 Current Consumption

The current consumption varies as a function of the setup condition. By adding up all the block currents shown in Table 8-1, a reasonable estimate of the current for any setup condition can be obtained.

**Table 8-1. Current Consumption per Block**

| BLOCK | | CONDITION (s) | | CURRENT (mA) |
|---|---|---|---|---|
| Device Core | | CLK_MUX = Buffer Mode | | 294 |
| | | CLK_MUX = Divide Mode | | 260 |
| | | CLK_MUX = Multiply Mode | SMCLK_EN=0 | 540 |
| | | | SMCLK_EN=1 | 560 |
| SYSREF SYNC Windowing | Core | SYSREF_EN=1 | | 80 |
| | Delay Generator | Generator Mode (SYSREF_MODE=0,1) | | 53 |
| | | Repeater Mode (SYSREF_MODE=2) | | 40 |
| | Windowing Circuitry | Windowing Circuitry (CLKPOS_CAPTURE_EN=1) | SYSREF_MODE=0,1 | 113 |
| | | | SYSREF_MODE=2 | 0 |
| | SYSREF Pulser | SYSREF_MODE=1 | | 7 |
| CLKOUT (Per active clock channel) | Core | SYSREF_EN=0 | | 25 |
| | | SYSREF_EN = 1 | Delay Not Used | 30 |
| | | | Delay Used | 40 |
| | Output Buffer | CHx_EN = CLKOUTx_EN=1 | | 4+6*CLKOUTx_PWR |
| SYSREFOUT | Core | SYSREFOUT_EN = CHx_EN = 1 | | 74 + SYSREFOUTx_PWR*5 |
| | Output Buffer | SYSREFOUT_EN = CHx_EN = 1 (SYSREFOUTx_PWR and SYSREFOUTx_VCM can interact which would make the output buffer current lower than the formula predicts in some cases) | | 2*SYSREFOUTx_PWR + 2*SYSREFOUTx_VCM |
| LOGICLKOUT | Core | LOGIC_EN=1 LOGICLKOUT_EN=1 | SYSREF_EN=0 | 49 |
| | | | SYSREF_EN=1 | 59 |
| | Output Buffer | | CML($R_P$=50Ω) | 16+1*LOGICLKOUT_PWR |
| | | | LVDS | 12 |
| | | | LVPECL | 30 |
| LOGISYSREFOUT | Core | LOGIC_EN=1 LOGISYSREFOUT_EN=1 | SYSREF_EN=0 | 0 |
| | | | SYSREF_EN=1 | 55 |
| | Output Buffer | LOGIC_EN=1 LOGISYSREFOUT_EN=1 | CML($R_P$=50Ω) | 16+1*LOGICLKOUT_PWR |
| | | | LVDS | 12 |
| | | | LVPECL | 30 |

If all the output clocks, LOGICLK, multiplier, and multiplier are all enabled, it is possible for this device to consume a significant amount of current. In order to mitigate this, It is recommended to turn off the SYSREF output buffers when not actively sending SYSREF pulses to conserve current.


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### 8.1.2 Treatment of Unused Pins

In many cases, not all pins will be needed. Table 8-2 gives recommendation on handling of these unused pins.

**Table 8-2. Treatment of Unused or Partially Used Pins**

| PIN(S) | TREATMENT |
|---|---|
| All Vcc Pins | These pins must always be connected to the supply. If the block that this powers (as implied by the pin name) is not used, then the bypassing can be minimized or eliminated. |
| SYSREFREQ | If driving single-ended, the complimentary input should have a AC-coupling capacitor and 50 Ω to ground. If using continuous SYSREF Generator mode, these pins can be either used to turn the output buffers on and off or they can be left floating. If left floating, use SRREQ_SPI to control the output gating. If not using SYSREF at all, pins can be left open. |
| CLKIN Complementary Input | If driving single-ended, the complementary input should have a AC-coupling capacitor and 50 Ω to ground. |
| BIAS01 and BIAS23 | These pins can be left open if multiplier is not used. |
| CLKOUT<br>SYSREFOUT<br>LOGICLKOUT<br>LOGISYSREFOUT | These pins can be left open if not used. |

## 8.2 Typical Application

For this application, the additive noise impact of using the LMX1204 as a x2 multiplier is exported when added to the LMX2820 3-GHz output clock. This particular setup used a single-ended clock to drive the LMX1204 for the sake of simplicity of hooking up two EVMs together, but driving it differentially is generally recommended.

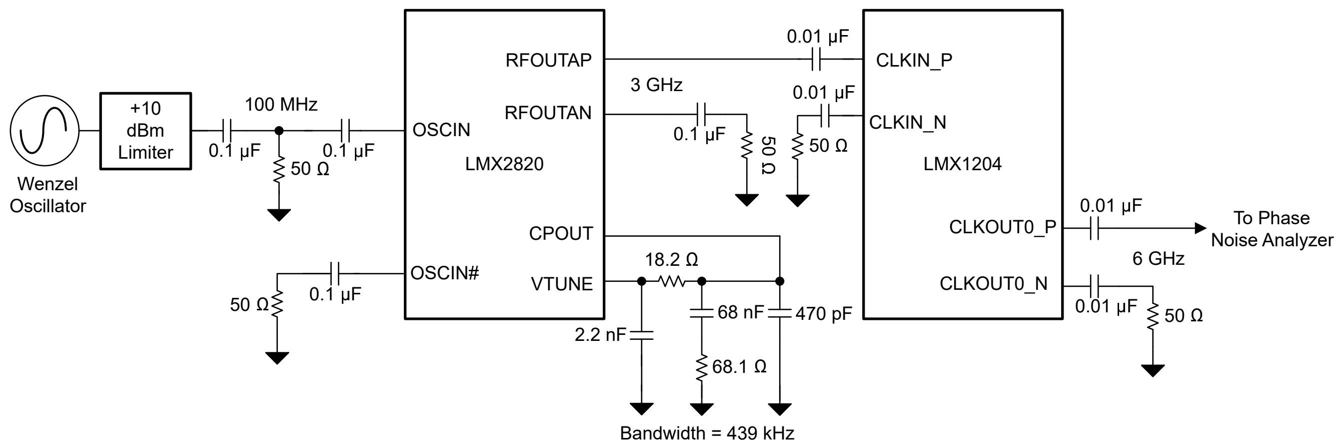


**Figure 8-1. Typical Application Schematic**

### 8.2.1 Design Requirements

Table 8-3 shows the design parameters for this example.

If not all outputs or SYSREF are used, TI recommends to compress the layout to minimize trace lengths, especially that of the input trace.

**Table 8-3. Design Parameters**

| PARAMETER | VALUE |
|---|---|
| LMX2820 Input Frequency | 100 MHz |
| LMX2820 Output Frequency | 3 GHz |
| LMX1204 Input Clock Frequency | 3 GHz |
| LMX1204 Output Clock Frequency | 6 GHz |
| Multiplier Value | x2 |

### 8.2.2 Detailed Design Procedure

In this example, a 3-GHz input clock is being multiplied up to a 6-GHz input clock. The external components do not change that much based on internal configuration. The TICS Pro software is very useful in calculating the necessary register values and configuring the device.

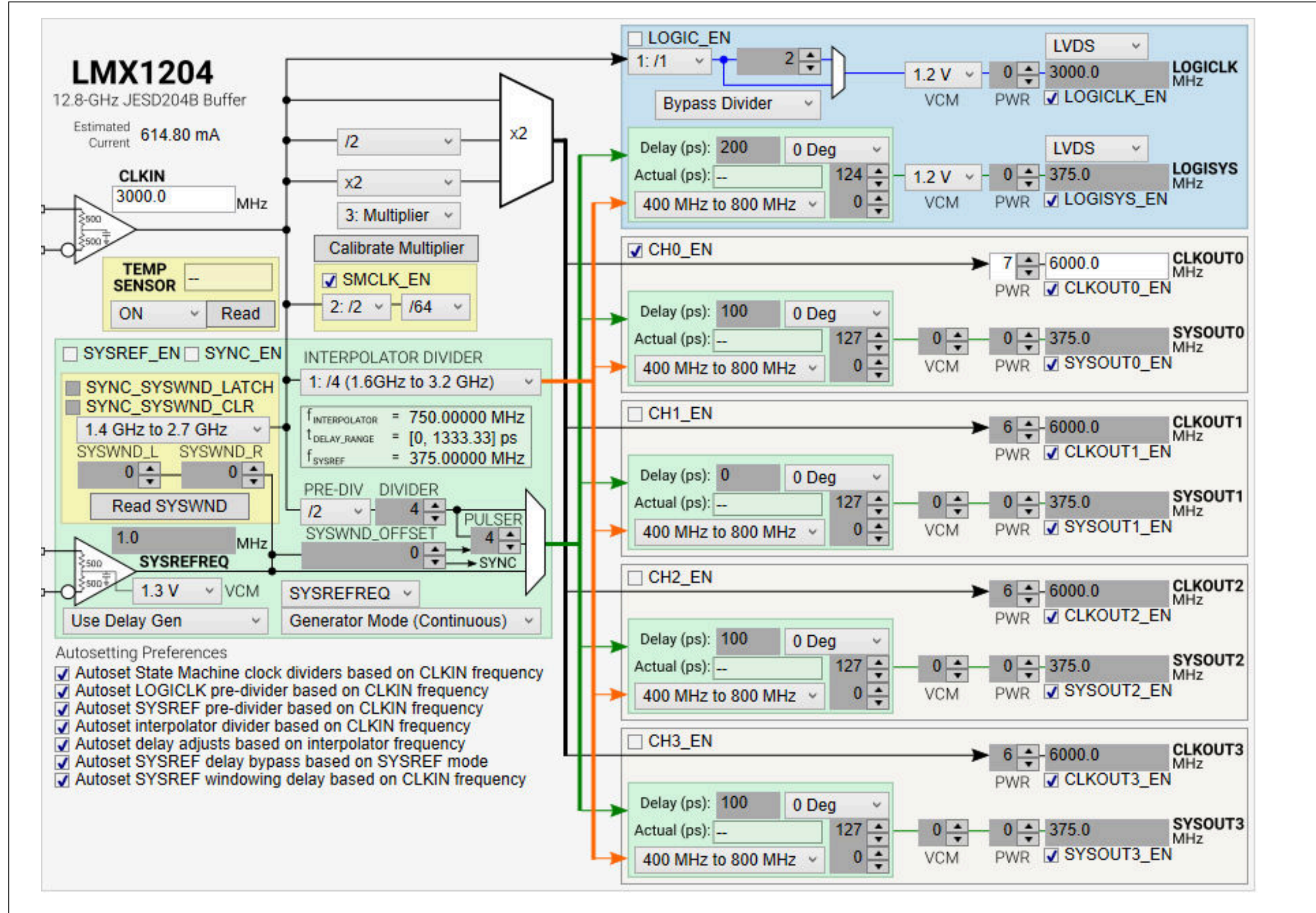


**Figure 8-2. LMX1204 TICS Pro Setup**


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### 8.2.3 Application Curve

In Figure 8-3, the total plot is the sum of the noise of the LMX1204 multiplier noise and the LMX2820 3-GHz output (scaled to 6 GHz by adding 6 dB). Note that the LMX1204 does increase the phase noise in the 1-MHz to 20-MHz range, but beyond 20 MHz, the input multiplier actually filters the output noise floor.

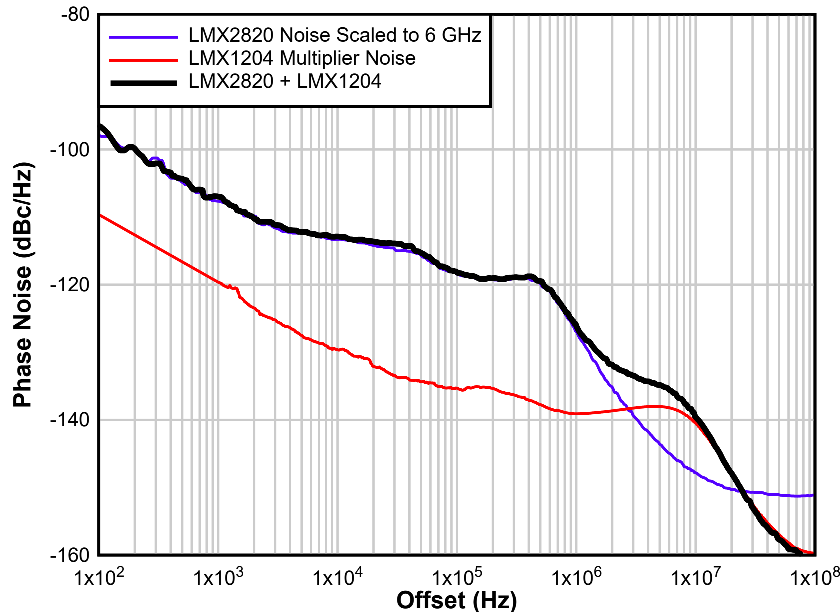


**Figure 8-3. Multiplier Output Frequency**

## 8.3 Power Supply Recommendations

This devices uses a 2.5-V supply for the whole device. A direct connection to a switching power supply will likely result in unwanted spurs at the output. Bypassing can be done individually at all the power pins. TI recommends placing smaller capacitors with higher frequency of minimum impedance on the same layer as the device, as close to the pins as possible. Since the frequencies of nearly all signals in the device are 100 MHz or greater, larger value bypass capacitors with low frequency of minimum impedance are only used for internal LDO stability, and their distance to the device (and the loop inductance of the bypass path) can be larger. The supply pins for the clocks and the LOGICLK should be isolated with a small resistor or ferrite bead if both are being used simultaneously. See the *Pin Configuration and Functions* section for additional recommendations for each pin.

---

**Note**

**This device has minimal PSRR due to the low operating voltage and internal filtering by LDOs; it is important that this device is connected to a low noise supply that does not have excessive spurious noise.**

---

## 8.4 Layout

### 8.4.1 Layout Guidelines

- If using an output single-ended, terminate the complementary side so that the impedance as seen looking out from this is similar to side that is used.
- GND pins on the outer perimeter of the package may be routed on the package back to the DAP.
- Minimize the length of the CLKIN trace for optimal phase noise. Poor matching may degrade the noise floor.
- Ensure the DAP on device is well-grounded with many vias.
- Use a low loss dielectric material, such as Rogers 4350B, for optimal output power.
- Be aware that if all the outputs and SYSREF are operating, the current consumption may be high enough to exceed the recommended internal junction temperature of 125°C; a heat sink may be necessary.

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### 8.4.2 Layout Example

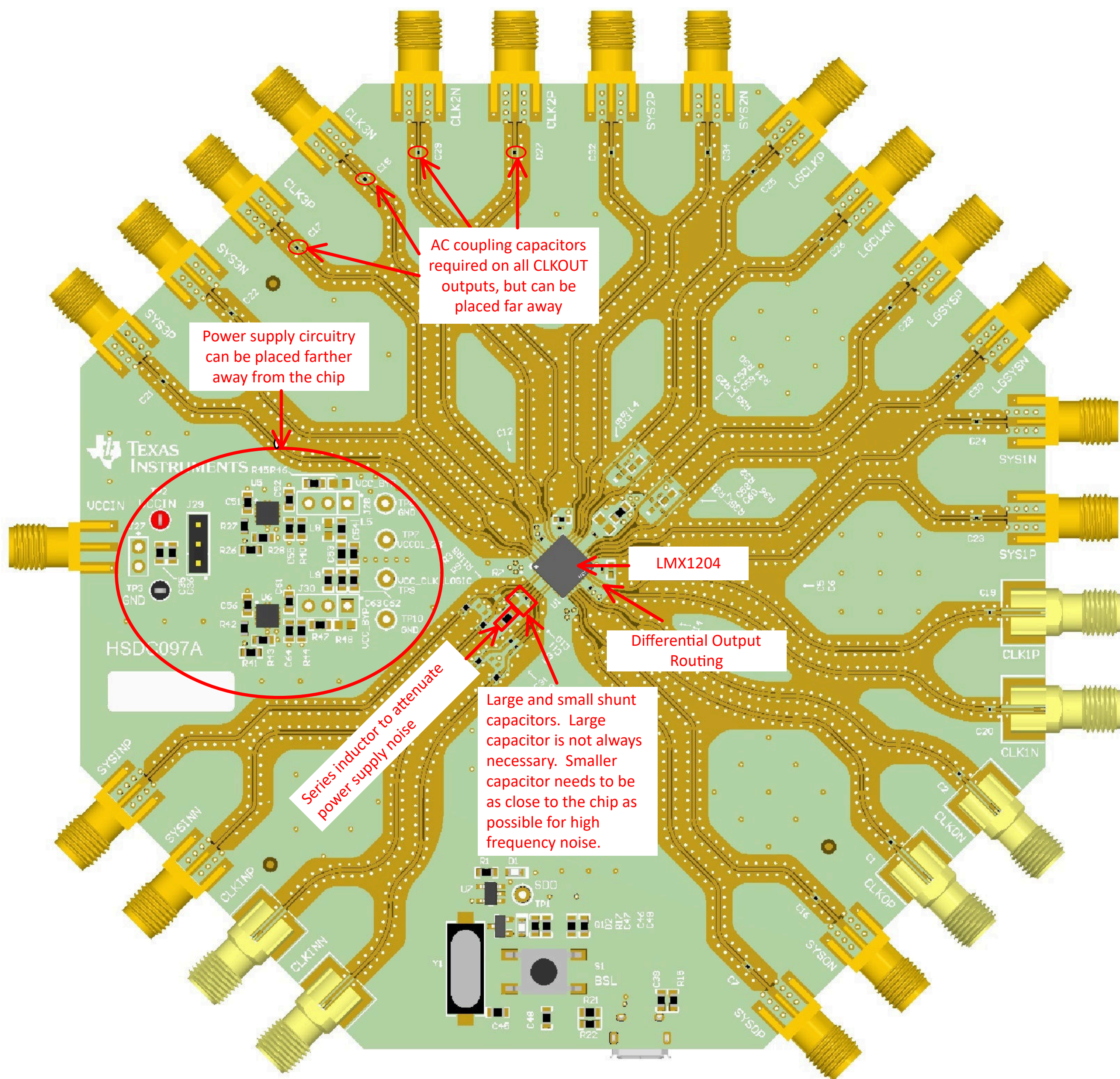


**Figure 8-4. Layout Example**


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# 9 Device and Documentation Support

## 9.1 Device Support

TI offers an extensive line of development tools and software to simulate the device performance and program the device.

**Table 9-1. Development Tools and Software**

| TOOL | TYPE | DESCRIPTION |
|---|---|---|
| PLLatinum™ Sim | Software | Simulates phase noise in all modes and filter transfer function in multiplier mode. |
| TICS Pro | Software | Programs the device with a user-friendly GUI with interactive feedback and hex register export. |
| Register Map Description | Document | Detailed description of all registers. |

## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 9.4 Trademarks

PLLatinum™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

## 9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

# 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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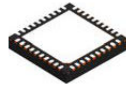
# PACKAGE OUTLINE



## RHA0040C

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD

A
6.1
5.9
B
PIN 1 INDEX AREA
6.1
5.9
0.5
0.3
0.3
0.2
DETAIL
OPTIONAL TERMINAL
TYPICAL
1 MAX
0.05
0.00
C
SEATING PLANE
0.08 C
□4.7±0.1
2X 4.5
(0.2) TYP
36X 0.5
11
20
10
21
EXPOSED
THERMAL PAD
2X
4.5
41
SYMM
SEE TERMINAL
DETAIL
1
30
40X 0.3
0.2
0.1 Ⓜ C A B
0.05 Ⓜ
40
31
PIN 1 ID
(OPTIONAL)
SYMM
40X 0.5
0.3

4219053/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.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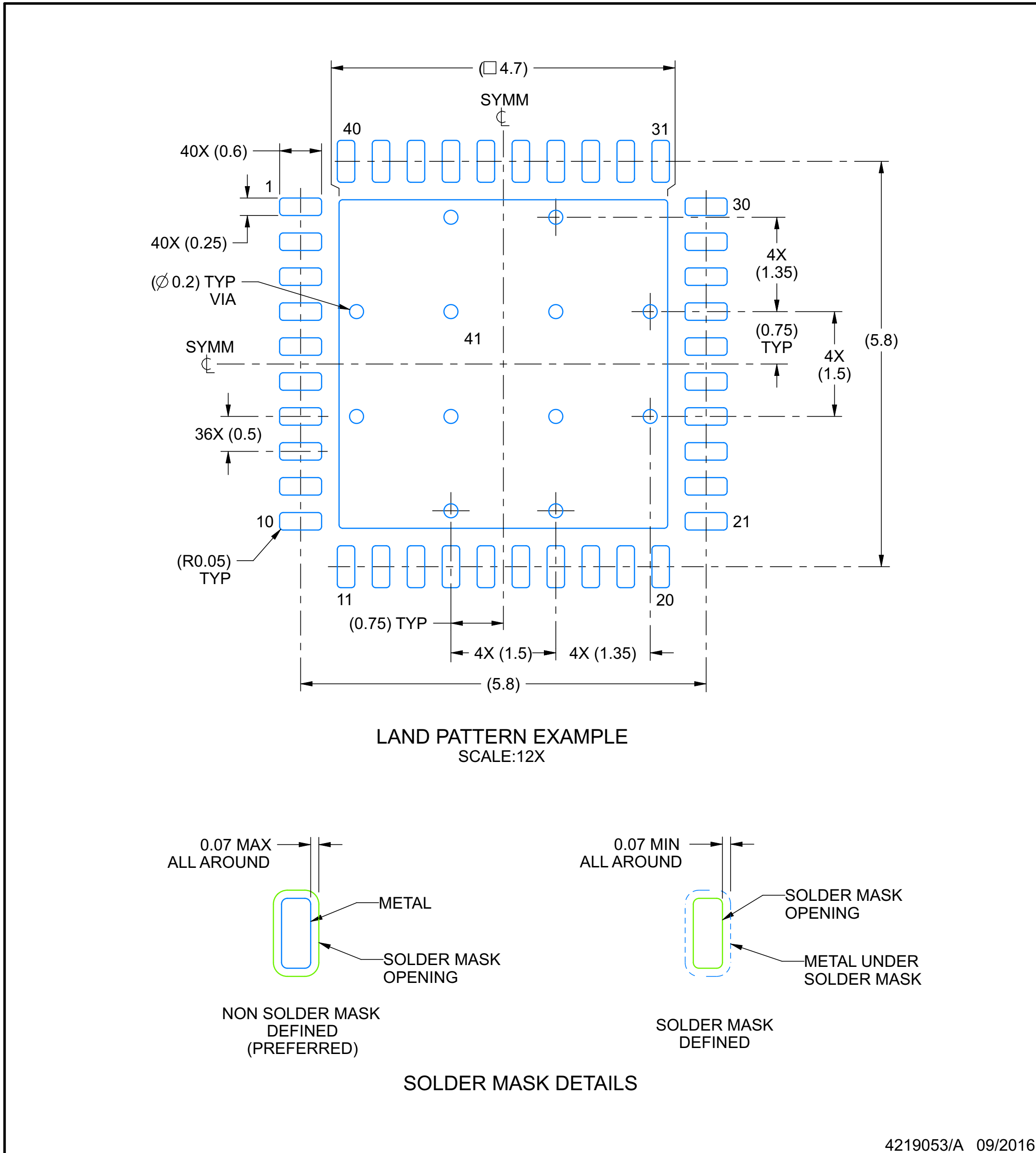
# EXAMPLE BOARD LAYOUT

## RHA0040C

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD




NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



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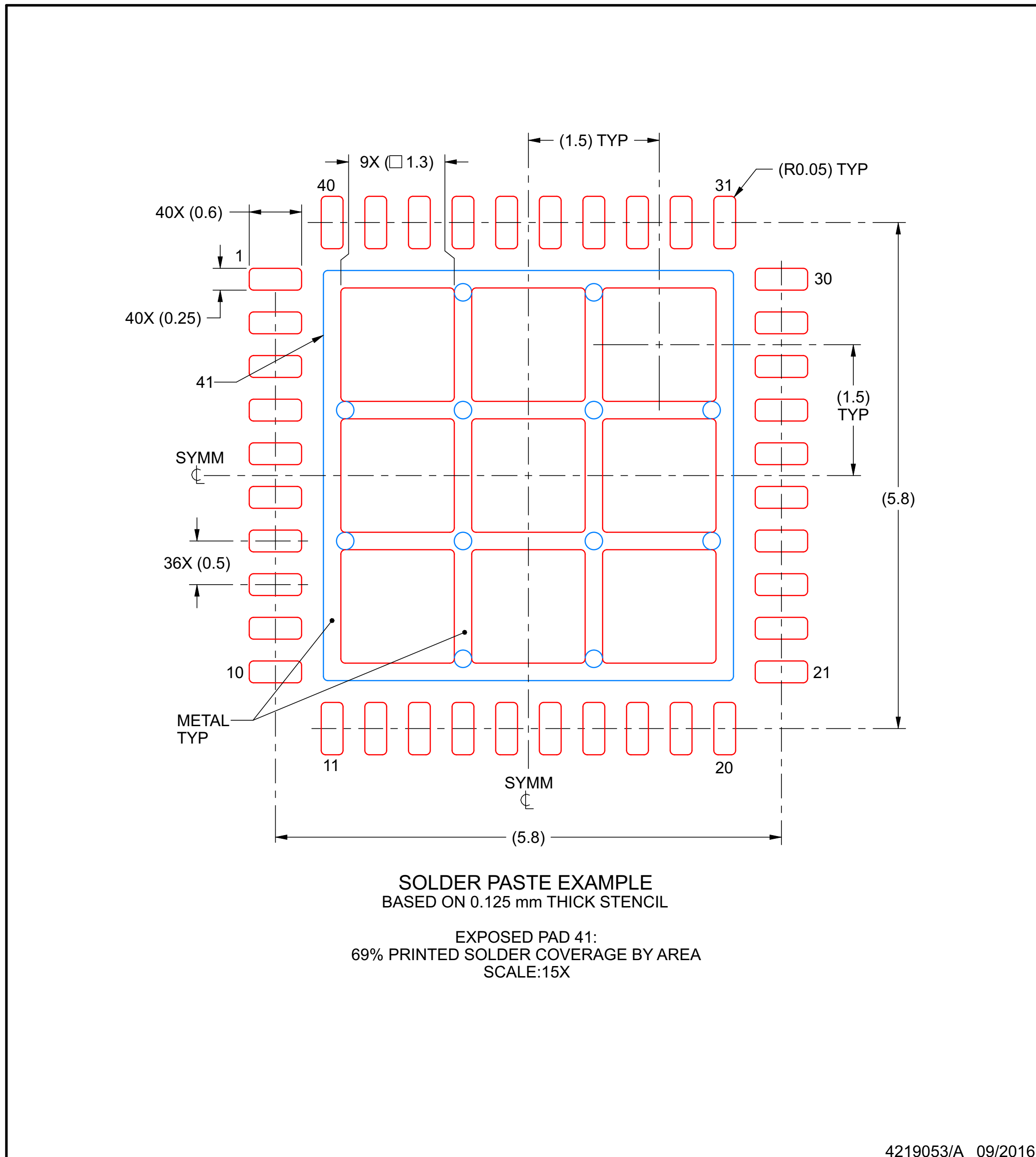
# EXAMPLE STENCIL DESIGN

## RHA0040C

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
69% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

4219053/A 09/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PLMX1204RHAT | ACTIVE | VQFN | RHA | 40 | 250 | TBD | Call TI | Call TI | -40 to 85 | | Samples |

[(1)] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[(2)] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[(3)] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[(4)] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[(5)] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[(6)] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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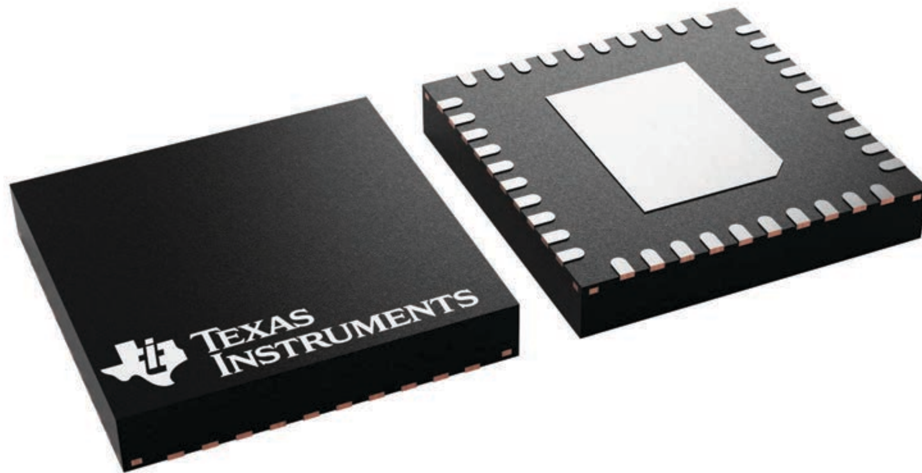
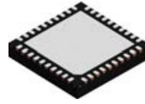
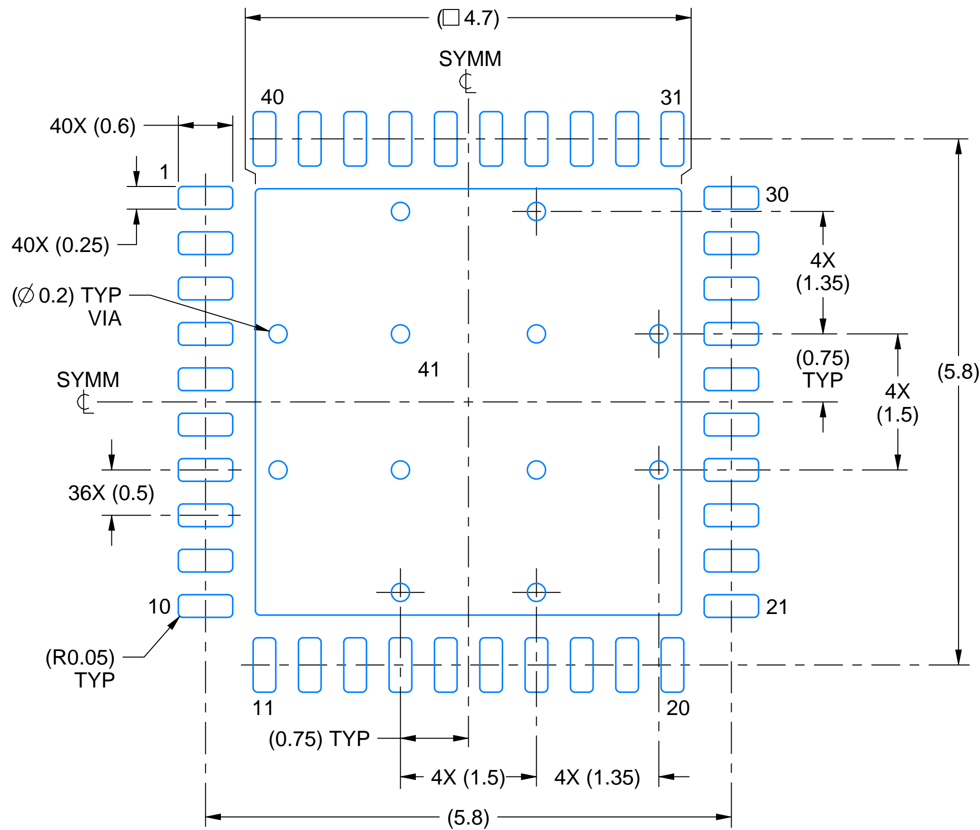
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



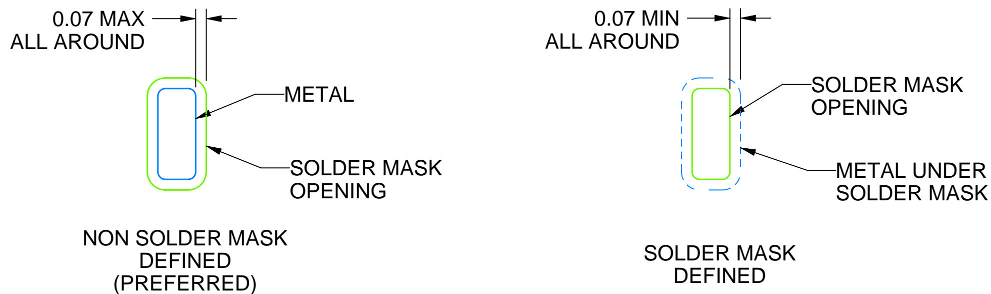


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:12X




SOLDER MASK DETAILS

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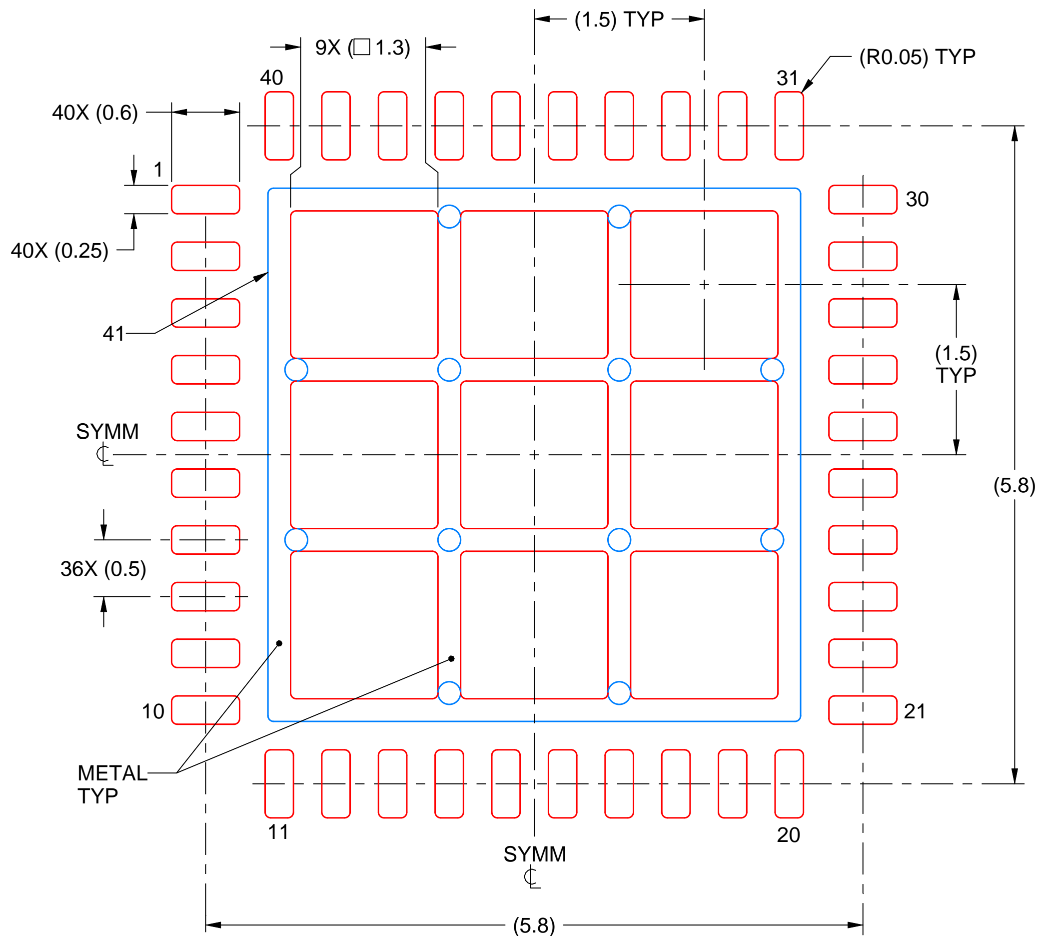
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
69% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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