Programmer's Guide

LMX1204 Register Map

ABSTRACT

The LMX1204 Register Map defines the register set for the LMX1204. Named registers are documented and described in detail, including valid states. Some registers are marked as reserved, but require value updates after device POR or after the RESET bit is toggled. When generating configurations in TICS Pro Software, any exported registers by default will include the required value updates to reserved registers as well. For applications where the register values are defined manually, carefully observe the required updates.

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Trademarks

1 LMX1204 Registers

Table 1-1 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 1-1 should be considered as reserved locations and the register contents should not be modified.

Table 1-1. LMX1204 Registers

Offset	Acronym	Register Name	Section
0x0	R0		Go
0x1	R1	RESERVED	Go
0x2	R2		Go
0x3	R3		Go
0x4	R4		Go
0x5	R5		Go
0x6	R6		Go
0x7	R7		Go
0x8	R8		Go
0x9	R9		Go
0xA	R10		Go
0xB	R11		Go
0xC	R12		Go
0xD	R13		Go
0xE	R14		Go
0xF	R15		Go
0x10	R16		Go
0x11	R17		Go
0x12	R18		Go
0x13	R19		Go
0x14	R20		Go
0x15	R21		Go
0x16	R22		Go
0x17	R23		Go
0x18	R24		Go
0x19	R25		Go
0x1A	R26		Go
0x1B	R27	RESERVED	Go
0x1D	R29		Go
0x1E	R30		Go
0x1F	R31	RESERVED	Go
0x20	R32	RESERVED	Go
0x21	R33	RESERVED	Go
0x22	R34	RESERVED	Go
0x30	R48	RESERVED	Go
0x40	R64		Go
0x47	R71		Go
0x4B	R75	RESERVED	Go
0x4C	R76	RESERVED	Go
0x4D	R77		Go
0x4F	R79	RESERVED	Go
0x58	R88	RESERVED	Go

Complex bit access types are encoded to fit into small table cells. Device Access Type Codes shows the codes that are used for access types in this section.

Table 1-2. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write

1.1 R0 Register (Offset = 0x0) [Reset = 0x0000]

R0 is shown in Table 1-3.

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Table 1-3. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED	R	0x0	Reserved
2	POWERDOWN	R/W	0x0	Sets the device in a low-power state. The states of other registers are maintained.
1	RESERVED	R/W	0x0	Reserved. Set to 0x0.
0	RESET	R/W	0x0	Soft Reset. Resets the entire logic and registers (equivalent to power-on reset)

1.2 R1 Register (Offset = 0x1) [Reset = 0x0000]

R1 is shown in Table 1-4.

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Table 1-4. R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	R	0x0	Reserved

1.3 R2 Register (Offset = 0x2) [Reset = 0x0223]

R2 is shown in Table 1-5.

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Table 1-5. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R	0x0	Reserved
9:6	SMCLK_DIV_PRE	R/W	0x8	Pre-divider for State Machine clock. The state machine clock is divided from the input clock. The output of the pre-divider should be ≤1600MHz. 0x1 = /1 0x2 = /2 0x4 = /4 0x8 = /8
5	SMCLK_EN	R/W	0x1	Enables the state machine clock generator. Must be enabled before programming other registers for LMX1204 to work in any mode, and for multiplier lock detect to work correctly. If multiplier lock detect is not used, the state machine clock generator can be disabled after programming.
4:0	RESERVED	R/W	0x3	Reserved. Set to 0x3.

1.4 R3 Register (Offset = 0x3) [Reset = 0xFF86]

R3 is shown in Table 1-6.

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Table 1-6. R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CH3_EN	R/W	0x1	Enables CH3 (CLKOUT3, SYSOUT3). Setting this bit to 0 will completely disable all CH3 circuitry, overriding the state of other powerdown/enable bits.
14	CH2_EN	R/W	0x1	Enables CH2 (CLKOUT2, SYSOUT2). Setting this bit to 0 will completely disable all CH2 circuitry, overriding the state of other powerdown/enable bits.
13	CH1_EN	R/W	0x1	Enables CH1 (CLKOUT1, SYSOUT1). Setting this bit to 0 will completely disable all CH1 circuitry, overriding the state of other powerdown/enable bits.
12	CH0_EN	R/W	0x1	Enables CH0 (CLKOUT0, SYSOUT0). Setting this bit to 0 will completely disable all CH0 circuitry, overriding the state of other powerdown/enable bits.
11	LOGIC_MUTE_CAL	R/W	0x1	Mute LOGICLK/LOGISYS during multiplier calibration.
10	CH3_MUTE_CAL	R/W	0x1	Mute CLKOUT3/SYSOUT3 during multiplier calibration.
9	CH2_MUTE_CAL	R/W	0x1	Mute CLKOUT2/SYSOUT2 during multiplier calibration.
8	CH1_MUTE_CAL	R/W	0x1	Mute CLKOUT1/SYSOUT1 during multiplier calibration.
7	CH0_MUTE_CAL	R/W	0x1	Mute CLKOUT0/SYSOUT0 during multiplier calibration.
6:3	RESERVED	R/W	0x0	Reserved. Set to 0x0.
2:0	SMCLK_DIV	R/W	0x6	State machine clock divider. Further divides the output of the state machine clock pre-divider. Input frequency must be ≤ 1600MHz. Output frequency must be ≤ 40MHz. Divide value is 2^{SMCLK_DIV}. 0x0 = /1 0x1 = /2 0x2 = /4 0x3 = /8 0x4 = /16 0x5 = /32 0x6 = /64 0x7 = /128

1.5 R4 Register (Offset = 0x4) [Reset = 0x360F]

R4 is shown in Table 1-7.

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Table 1-7. R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R	0x0	Reserved
13:11	CLKOUT1_PWR	R/W	0x6	Controls the output power of CLKOUT1. Larger values correspond to higher output power.
10:8	CLKOUT0_PWR	R/W	0x6	Controls the output power of CLKOUT0. Larger values correspond to higher output power.
7	SYSOUT3_EN	R/W	0x0	Enables SYSREFOUT3 output buffer.
6	SYSOUT2_EN	R/W	0x0	Enables SYSREFOUT2 output buffer.
5	SYSOUT1_EN	R/W	0x0	Enables SYSREFOUT1 output buffer.
4	SYSOUT0_EN	R/W	0x0	Enables SYSREFOUT0 output buffer.
3	CLKOUT3_EN	R/W	0x1	Enables CLKOUT3 output buffer.
2	CLKOUT2_EN	R/W	0x1	Enables CLKOUT2 output buffer.
1	CLKOUT1_EN	R/W	0x1	Enables CLKOUT1 output buffer.
0	CLKOUT0_EN	R/W	0x1	Enables CLKOUT0 output buffer.

1.6 R5 Register (Offset = 0x5) [Reset = 0x0036]

R5 is shown in Table 1-8.

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Table 1-8. R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14:12	SYSOUT2_PWR	R/W	0x0	Controls the output power of SYSREFOUT2. Larger values correspond to higher output power. SYSOUT2_VCM must be set properly to bring the output common-mode voltage within permissible limits.
11:9	SYSOUT1_PWR	R/W	0x0	Controls the output power of SYSREFOUT1. Larger values correspond to higher output power. SYSOUT1_VCM must be set properly to bring the output common-mode voltage within permissible limits.
8:6	SYSOUT0_PWR	R/W	0x0	Controls the output power of SYSREFOUT0. Larger values correspond to higher output power. SYSOUT0_VCM must be set properly to bring the output common-mode voltage within permissible limits.
5:3	CLKOUT3_PWR	R/W	0x6	Controls the output power of CLKOUT3. Larger values correspond to higher output power.
2:0	CLKOUT2_PWR	R/W	0x6	Controls the output power of CLKOUT2. Larger values correspond to higher output power.

1.7 R6 Register (Offset = 0x6) [Reset = 0x0000]

R6 is shown in Table 1-9.

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Table 1-9. R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	LOGICLK_EN	R/W	0x0	Enables the logic clock output buffer.
14:12	SYSOUT3_VCM	R/W	0x0	Sets the output common mode of SYSREFOUT3. SYSOUT3_PWR must be set properly to bring the minimum and maximum output voltage within permissible limits.
11:9	SYSOUT2_VCM	R/W	0x0	Sets the output common mode of SYSREFOUT2. SYSOUT2_PWR must be set properly to bring the minimum and maximum output voltage within permissible limits.
8:6	SYSOUT1_VCM	R/W	0x0	Sets the output common mode of SYSREFOUT1. SYSOUT1_PWR must be set properly to bring the minimum and maximum output voltage within permissible limits.
5:3	SYSOUT0_VCM	R/W	0x0	Sets the output common mode of SYSREFOUT0. SYSOUT0_PWR must be set properly to bring the minimum and maximum output voltage within permissible limits.
2:0	SYSOUT3_PWR	R/W	0x0	Controls the output power of SYSREFOUT3. Larger values correspond to higher output power. SYSOUT3_VCM must be set properly to bring the output common-mode voltage within permissible limits.

1.8 R7 Register (Offset = 0x7) [Reset = 0x0000]

R7 is shown in Table 1-10.

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Table 1-10. R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14:13	LOGISYS_VCM	R/W	0x0	In LVDS mode, sets the output common mode of the logic SYSREF output. 0x0 = 1.2V 0x1 = 1.1V 0x2 = 1.0V 0x3 = 0.9V
12:11	LOGICLK_VCM	R/W	0x0	In LVDS mode, sets the output common mode of the logic clock output. 0x0 = 1.2V 0x1 = 1.1V 0x2 = 1.0V 0x3 = 0.9V
10:9	LOGISYS_PREDRV_PWR	R/W	0x0	Controls the output power of the logic SYSREF pre-driver. Larger values correspond to higher output power. LOGISYS_VCM must be set properly to bring the output common-mode voltage within permissible limits.
8:7	LOGICLK_PREDRV_PWR	R/W	0x0	Controls the output power of the logic clock pre-driver. Larger values correspond to higher output power.
6:4	LOGISYS_PWR	R/W	0x0	Controls the output power of the logic SYSREF output. Larger values correspond to higher output power.
3:1	LOGICLK_PWR	R/W	0x0	Controls the output power of the logic clock output. Larger values correspond to higher output power. LOGICLK_VCM must be set properly to bring the output common-mode voltage within permissible limits.
0	LOGISYS_EN	R/W	0x0	Enables the logic SYSREF output buffer.

1.9 R8 Register (Offset = 0x8) [Reset = 0x0120]

R8 is shown in Table 1-11.

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Table 1-11. R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED	R	0x0	Reserved
8:6	LOGICLK_DIV_PRE	R/W	0x4	Pre-divider for logic clock divider. Output of the pre-divider should be ≤ 3.2GHz. 0x1 = /1 0x2 = /2 0x4 = /4
5	RESERVED	R/W	0x1	Reserved. Set to 0x1.
4	LOGIC_EN	R/W	0x0	Enables the LOGICLK/LOGISYS subsystem. Setting this bit to 0 will completely disable all LOGICLK/LOGISYS circuitry, overriding the state of other powerdown/enable bits.
3:2	LOGISYS_FMT	R/W	0x0	Selects the output driver format of the LOGISYS output. 0x0 = LVDS (w/ Temp Comp) 0x1 = LVPECL 0x2 = CML
1:0	LOGICLK_FMT	R/W	0x0	Selects the output driver format of the LOGICLK output. 0x0 = LVDS (w/ Temp Comp) 0x1 = LVPECL 0x2 = CML

1.10 R9 Register (Offset = 0x9) [Reset = 0x001E]

R9 is shown in Table 1-12.

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Table 1-12. R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	SRREQ_VCM	R/W	0x0	Sets the internal DC Bias for the SYSREFREQ pins. Bias must be enabled for AC-coupled inputs, but can be enabled or disabled for DC-coupled inputs. Minimum SYSREF common-mode voltage with bias disabled is 1.0V. 0x0 = 1.3V 0x1 = 1.1V 0x2 = 1.5V 0x3 = Disabled (DC-coupled only)
13	SYNC_EN	R/W	0x0	Enables synchronization for the dividers. Used for multi-device synchronization. If SYSREF_EN=0, this bit must be set to allow synchronization. Redundant if SYSREF_EN=1.
12	LOGICLK_DIV_PD	R/W	0x0	Disables the LOGICLK divider. Logic clock pre-divider will remain enabled. Used to reduce current consumption when bypassing the LOGICLK divider.
11	LOGICLK_DIV_BYP	R/W	0x0	Bypass the LOGICLK divider, deriving LOGICLK output directly from the pre-divider. Used to achieve divide-by-1 when LOGICLK_DIV_PRE=1. When LOGICLK_DIV_PRE=2 or 4, this bit must be set to 0.
10	RESERVED	R/W	0x0	Reserved. Set to 0x0.
9:0	LOGICLK_DIV	R/W	0x1E	Logic clock divider. 0x0: Reserved 0x1: Reserved 0x2: divide-by-2 0x3: divide-by-3 ... 0x1FF: divide-by-1023

1.11 R10 Register (Offset = 0xA) [Reset = 0x0000]

R10 is shown in Table 1-13.

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Table 1-13. R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED	R	0x0	Reserved
0	SYSWND_EN	R/W	0x0	Enables the SYSREF windowing circuit. When SYSREF_EN=0, the state of SYSWND_EN will be ignored and the SYSREF windowing circuit will be disabled. Redundant if SYSREF_EN=1 or SYNC_EN=1.

1.12 R11 Register (Offset = 0xB) [Reset = 0xFFFF]

R11 is shown in Table 1-14.

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Table 1-14. R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	rb_SYSWND_R	R	0xFFFF	Returns the position of SYSREF with respect to the input clock rising edge.

1.13 R12 Register (Offset = 0xC) [Reset = 0xFFFF]

R12 is shown in Table 1-15.

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Table 1-15. R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	rb_SYSWND_L	R	0xFFFF	Returns the position of SYSREF with respect to the input clock rising edge.

1.14 R13 Register (Offset = 0xD) [Reset = 0x0003]

R13 is shown in Table 1-16.

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Table 1-16. R13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	RESERVED	R	0x0	Reserved
1:0	SYSWND_DLY	R/W	0x3	Controls the step size of the SYSREF Windowing delay element. Set according to CLKIN frequency. 0x0 = 1.4GHz to 2.7GHz 0x1 = 2.4GHz to 4.7GHz 0x2 = 3.1GHz to 5.7GHz 0x3 = 4.5GHz to 12.8GHz

1.15 R14 Register (Offset = 0xE) [Reset = 0x0000]

R14 is shown in Table 1-17.

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Table 1-17. R14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED	R/W	0x0	Reserved. Set to 0x0.
8	SYNC_MUTE_PD	R/W	0x0	When SRREQ_MODE=0, SYSREF generator output is normally muted. Set this bit to unmute SYSREF generator output even when SRREQ_MODE=0.
7:3	RESERVED	R/W	0x0	Reserved. Set to 0x0.
2:1	SRREQ_MODE	R/W	0x0	Selects the function of the SYSREFREQ pins. 0x0 = SYNC Pin 0x1 = SYSREFREQ Pin 0x2 = SYSREF Windowing
0	SYNC_SYSWND_LATCH	R/W	0x0	If enabled, SYNC/Windowing will be performed on the first SYSREFREQ edge only. Successive SYSREFREQ pulses will be ignored until SYNC_SYSWND_CLR is toggled low→high→low.

1.16 R15 Register (Offset = 0xF) [Reset = 0x0901]

R15 is shown in Table 1-18.

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Table 1-18. R15 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0x0	Reserved
11:10	SYSREF_DIV_PRE	R/W	0x2	Sets the SYSREF pre-divider. Maximum output frequency must be ≤ 3.2GHz. 0x0 = /1 0x1 = /2 0x2 = /4 0x3 = Invalid
9	SYSREF_GEN_EN	R/W	0x0	Enables SYSREF generator (divider/pulser). If SYSREF_EN=0, the state of this register is ignored, and this circuit is disabled.
8	RESERVED	R/W	0x1	Reserved. Set to 0x1.
7	SYSREF_EN	R/W	0x0	Enables SYNC/SYSREF subsystem. Setting this bit to 0 will completely disable all SYNC, SYSREF, and windowing circuitry, overriding the state of other powerdown/enable bits.
6:1	SYSWND_OFFSET	R/W	0x0	Selects the delay which will be used to SYNC the dividers. The value for this field must be set based on the rb_SYSWND_L/H value to ensure the internal setup and hold time are satisfied. Refer to the data sheet for detailed description of the SYSREF windowing procedure.
0	SYNC_SYSWND_CLR	R/W	0x1	Clears the SYNC/Windowing subsystems, resetting rb_SYSWND_L/R and the SYNC-to-CLKIN re-timers. This bit should be set and cleared once whenever the SYNC or Windowing operations must be performed.

1.17 R16 Register (Offset = 0x10) [Reset = 0x1003]

R16 is shown in Table 1-19.

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Table 1-19. R16 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	SYSREF_PULSE_COUNT	R/W	0x1	Programs the number of pulses in generator mode. 0x0: Reserved 0x1: 1 pulse 0x2: 2 pulses ... 0xF: 15 pulses
11:0	SYSREF_DIV	R/W	0x3	Sets the SYSREF divider. Maximum output frequency must be ≤ 100MHz. 0x0: Reserved 0x1: Reserved 0x2: divide-by-2 0x3: divide-by-3 ... 0xFFF: divide-by-4095

1.18 R17 Register (Offset = 0x11) [Reset = 0x07F0]

R17 is shown in Table 1-20.

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Table 1-20. R17 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED	R	0x0	Reserved
10:4	SYSOUT0_DLY_I	R/W	0x7F	Selects fine phase for SYSOUT0 delay generator. Must satisfy SYSOUT0_DLY_I + SYSOUT0_DLY_Q = 127.
3:2	SYSOUT0_DLY_QUAD	R/W	0x0	Selects coarse phase (quadrant) for SYSOUT0 delay generator. 0x0 = 180° 0x1 = 270° 0x2 = 90° 0x3 = 0°
1:0	SYSREF_MODE	R/W	0x0	Controls how the SYSREF signal is generated or repeated. 0x0 = Generator (Continuous) 0x1 = Generator (Pulser) 0x2 = Repeater

1.19 R18 Register (Offset = 0x12) [Reset = 0xFE00]

R18 is shown in Table 1-21.

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Table 1-21. R18 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	SYSOUT1_DLY_I	R/W	0x7F	Selects fine phase for SYSOUT1 delay generator. Must satisfy SYSOUT1_DLY_I + SYSOUT1_DLY_Q = 127.
8:7	SYSOUT1_DLY_QUAD	R/W	0x0	Selects coarse phase (quadrant) for SYSOUT1 delay generator. 0x0 = 180° 0x1 = 270° 0x2 = 90° 0x3 = 0°
6:0	SYSOUT0_DLY_Q	R/W	0x0	Selects fine phase for SYSOUT0 delay generator. Must satisfy SYSOUT0_DLY_I + SYSOUT0_DLY_Q = 127.

1.20 R19 Register (Offset = 0x13) [Reset = 0xFE00]

R19 is shown in Table 1-22.

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Table 1-22. R19 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	SYSOUT2_DLY_I	R/W	0x7F	Selects fine phase for SYSOUT2 delay generator. Must satisfy SYSOUT2_DLY_I + SYSOUT2_DLY_Q = 127.
8:7	SYSOUT2_DLY_QUAD	R/W	0x0	Selects coarse phase (quadrant) for SYSOUT2 delay generator. 0x0 = 180° 0x1 = 270° 0x2 = 90° 0x3 = 0°
6:0	SYSOUT1_DLY_Q	R/W	0x0	Selects fine phase for SYSOUT1 delay generator. Must satisfy SYSOUT1_DLY_I + SYSOUT1_DLY_Q = 127.

1.21 R20 Register (Offset = 0x14) [Reset = 0xFE00]

R20 is shown in Table 1-23.

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Table 1-23. R20 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	SYSOUT3_DLY_I	R/W	0x7F	Selects fine phase for SYSOUT3 delay generator. Must satisfy SYSOUT3_DLY_I + SYSOUT3_DLY_Q = 127.
8:7	SYSOUT3_DLY_QUAD	R/W	0x0	Selects coarse phase (quadrant) for SYSOUT3 delay generator. 0x0 = 180° 0x1 = 270° 0x2 = 90° 0x3 = 0°
6:0	SYSOUT2_DLY_Q	R/W	0x0	Selects fine phase for SYSOUT2 delay generator. Must satisfy SYSOUT2_DLY_I + SYSOUT2_DLY_Q = 127.

1.22 R21 Register (Offset = 0x15) [Reset = 0xFE00]

R21 is shown in Table 1-24.

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Table 1-24. R21 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	LOGISYS_DLY_I	R/W	0x7F	Selects fine phase for LOGISYS delay generator. Must satisfy LOGISYS_DLY_I + LOGISYS_DLY_Q = 127.
8:7	LOGISYS_DLY_QUAD	R/W	0x0	Selects coarse phase (quadrant) for LOGISYS delay generator. 0x0 = 180° 0x1 = 270° 0x2 = 90° 0x3 = 0°
6:0	SYSOUT3_DLY_Q	R/W	0x0	Selects fine phase for SYSOUT3 delay generator. Must satisfy SYSOUT3_DLY_I + SYSOUT3_DLY_Q = 127.

1.23 R22 Register (Offset = 0x16) [Reset = 0x8A00]

R22 is shown in Table 1-25.

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Table 1-25. R22 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	SYSREF_DLYGEN_CLKDIV	R/W	0x4	Selects the delay generator clock division, determining $f_{INTERPOLATOR}$ and the delay generator resolution. 0x0 = /2 (≤ 1.6GHz) 0x1 = /4 (1.6GHz to 3.2GHz) 0x2 = /8 (3.2GHz to 6.4GHz) 0x4 = /16 (6.4GHz to 12.8GHz)
12:7	RESERVED	R/W	0x14	Reserved. Set to 0x14.
6:0	LOGISYS_DLY_Q	R/W	0x0	Selects fine phase for LOGISYS delay generator. Must satisfy LOGISYS_DLY_I + LOGISYS_DLY_Q = 127.

1.24 R23 Register (Offset = 0x17) [Reset = 0x0000]

R23 is shown in Table 1-26.

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Table 1-26. R23 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R	0x0	Reserved
9:8	LOGISYS_DLY_ADJ	R/W	0x0	Sets the frequency range of the LOGISYS delay generator. Set according to $f_{INTERPOLATOR}$. 0x0 = 400MHz to 800MHz 0x1 = 200MHz to 400MHz 0x2 = Reserved 0x3 = 150MHz to 200MHz
7:6	SYSOUT3_DLY_ADJ	R/W	0x0	Sets the frequency range of the SYSOUT3 delay generator. Set according to $f_{INTERPOLATOR}$. 0x0 = 400MHz to 800MHz 0x1 = 200MHz to 400MHz 0x2 = Reserved 0x3 = 150MHz to 200MHz
5:4	SYSOUT2_DLY_ADJ	R/W	0x0	Sets the frequency range of the SYSOUT2 delay generator. Set according to $f_{INTERPOLATOR}$. 0x0 = 400MHz to 800MHz 0x1 = 200MHz to 400MHz 0x2 = Reserved 0x3 = 150MHz to 200MHz
3:2	SYSOUT1_DLY_ADJ	R/W	0x0	Sets the frequency range of the SYSOUT1 delay generator. Set according to $f_{INTERPOLATOR}$. 0x0 = 400MHz to 800MHz 0x1 = 200MHz to 400MHz 0x2 = Reserved 0x3 = 150MHz to 200MHz
1:0	SYSOUT0_DLY_ADJ	R/W	0x0	Sets the frequency range of the SYSOUT0 delay generator. Set according to $f_{INTERPOLATOR}$. 0x0 = 400MHz to 800MHz 0x1 = 200MHz to 400MHz 0x2 = Reserved 0x3 = 150MHz to 200MHz

1.25 R24 Register (Offset = 0x18) [Reset = 0x0100]

R24 is shown in Table 1-27.

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Table 1-27. R24 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED	R	0x0	Reserved
10:9	TEMPSENSE_EN	R/W	0x0	Enables on-die temperature sensor. 0x0 = OFF 0x1 = Reserved 0x2 = Reserved 0x3 = ON
8	RESERVED	R/W	0x1	Reserved. Set to 0x1.
7	MUXOUT_EN	R/W	0x0	Enables or tri-states MUXOUT pin. 0x0 = Tri-State 0x1 = Push-Pull
6:1	RESERVED	R/W	0x0	Reserved. Set to 0x0.
0	MUXOUT_SEL	R/W	0x0	Selects MUXOUT function. 0x0 = Lock Detect 0x1 = SDO

1.26 R25 Register (Offset = 0x19) [Reset = 0x27FF]

R25 is shown in Table 1-28.

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Table 1-28. R25 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	CLK_MUX	R/W	0x1	Selects buffer behavior. 0x1 = Buffer 0x2 = Divider 0x3 = Multiplier
12:11	RESERVED	R/W	0x0	Reserved. Set to 0x0.
10:0	rb_TEMPSENSE	R	0x7FF	Output of on-die temperature sensor. Valid only when TEMPSENSE_EN=1. Valid during powerdown. To convert to °C, use the following equation: T_J = (rb_TEMPSENSE - 535.47) / 1.35

1.27 R26 Register (Offset = 0x1A) [Reset = 0x0040]

R26 is shown in Table 1-29.

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Table 1-29. R26 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED	R/W	0x8	Reserved. Set to 0x4.
2:0	CLK_DIV	R/W	0x0	When CLK_MUX=2 (divider mode), sets the clock divider equal to 1 + field value. When CLK_MUX=3 (multiplier mode), sets the multiplier equal to 1 + field value. If this field is set to 0, or to an unsupported multiplier mode value, the device will be placed in buffer mode. 0x0 = Reserved 0x1 = /2 or x2 0x2 = /3 or x3 0x3 = /4 or x4 0x4 = /5 or Reserved 0x5 = /6 or Reserved 0x6 = /7 or Reserved 0x7 = /8 or Reserved

1.28 R27 Register (Offset = 0x1B) [Reset = 0x1000]

R27 is shown in Table 1-30.

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Table 1-30. R27 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R	0x0	Reserved
12:0	RESERVED	R/W	0x1000	Reserved. Set to 0x1800.

1.29 R29 Register (Offset = 0x1D) [Reset = 0x0A08]

R29 is shown in Table 1-31.

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Table 1-31. R29 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R	0x0	Reserved
12	FORCE_VCO	R/W	0x0	Forces the multiplier PLL's VCO to the value selected by VCO_SEL.
11:9	VCO_SEL	R/W	0x5	User specified start VCO for multiplier PLL. Calibration starts from the VCO set by this field.
8:0	RESERVED	R/W	0x8	Reserved. Set to 0x8.

1.30 R30 Register (Offset = 0x1E) [Reset = 0x1200]

R30 is shown in Table 1-32.

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Table 1-32. R30 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R	0x0	Reserved
12:8	RESERVED	R/W	0x12	Reserved. Set to 0x06.
7:0	CAPCTRL	R/W	0x0	Selects the starting value for the VCO tuning capacitance during multiplier PLL calibration. Used to speed up multiplier calibration.

1.31 R31 Register (Offset = 0x1F) [Reset = 0x4A52]

R31 is shown in Table 1-33.

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Table 1-33. R31 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14:0	RESERVED	R/W	0x4A52	Reserved. Set to 0x1CC6.

1.32 R32 Register (Offset = 0x20) [Reset = 0x0192]

R32 is shown in Table 1-34.

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Table 1-34. R32 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R	0x0	Reserved
12:0	RESERVED	R/W	0x192	Reserved. Set to 0x607.

1.33 R33 Register (Offset = 0x21) [Reset = 0x0240]

R33 is shown in Table 1-35.

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Table 1-35. R33 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R	0x0	Reserved
13:0	RESERVED	R/W	0x240	Reserved. Set to 0x00C1.

1.34 R34 Register (Offset = 0x22) [Reset = 0x0000]

R34 is shown in Table 1-36.

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Table 1-36. R34 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0x0	Reserved
11:0	RESERVED	R/W	0x0	Reserved. Set to 0xF13.

1.35 R48 Register (Offset = 0x30) [Reset = 0x2AB9]

R48 is shown in Table 1-37.

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Table 1-37. R48 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	R/W	0x2AB9	Reserved. Set to 0x2C79.

1.36 R64 Register (Offset = 0x40) [Reset = 0x45F0]

R64 is shown in Table 1-38.

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Table 1-38. R64 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED	R/W	0x22	Reserved. Set to 0x32.
8:4	rb_VCO_SEL	R/W	0x1F	Readback multiplier PLL's VCO core selection. The readback is inverted, such that the low bit in the readback designates the VCO core. 0xF = VCO5 0x17 = VCO4 0x1B = VCO3 0x1D = VCO2 0x1E = VCO1
3:0	RESERVED	R/W	0x0	Reserved. Set to 0x0.

1.37 R71 Register (Offset = 0x47) [Reset = 0x0000]

R71 is shown in Table 1-39.

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Table 1-39. R71 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	RESERVED	R	0x0	Reserved
1:0	SYSREF_DLYGEN_BYP	R/W	0x0	Bypass delay generator retiming. Must be set to 0x2 for repeater mode. 0x0 = Use Delay Gen 0x1 = Bypass (Generator Mode) 0x2 = Bypass (Repeater Mode)

1.38 R75 Register (Offset = 0x4B) [Reset = 0x0000]

R75 is shown in Table 1-40.

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Table 1-40. R75 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	R/W	0x0	Reserved. Set to 0x0002.

1.39 R76 Register (Offset = 0x4C) [Reset = 0x1100]

R76 is shown in Table 1-41.

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Table 1-41. R76 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0x1	Reserved
11:0	RESERVED	R/W	0x100	Reserved. Set to 0x600.

1.40 R77 Register (Offset = 0x4D) [Reset = 0x21E7]

R77 is shown in Table 1-42.

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Table 1-42. R77 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	RESERVED	R	0x879	Reserved
1:0	rb_LD	R	0x3	0x0 = Multiplier Unlocked (VTUNE low) 0x1 = Reserved 0x2 = Multiplier Locked 0x3 = Multiplier Unlocked (VTUNE high)

1.41 R79 Register (Offset = 0x4F) [Reset = 0x8080]

R79 is shown in Table 1-43.

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Table 1-43. R79 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R	0x2	Reserved
13:0	RESERVED	R/W	0x80	Reserved. Set to 0x98.

1.42 R88 Register (Offset = 0x58) [Reset = 0x0000]

R88 is shown in Table 1-44.

Return to the Summary Table.

Table 1-44. R88 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	R/W	0x0	Reserved. Set to 0x0004.

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