Application Report
SNVA800B–December 2017–Revised October 2018

Inverting Application for the LMZM33602/3

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ABSTRACT

The LMZM33603 is a 3-A rated synchronous step-down power module from Texas Instruments that features a wide operating input range from 4 V to 36 V with adjustable output voltage options from 1 V to 18 V. Furthermore, the LMZM33603 can be configured in an inverting buck-boost (IBB) topology with the output voltage inverted or negative with respect to ground. This application report shows how the conventional non-inverting evaluation board for the LMZM33603 can be configured for an inverting application without the need to spin the PCB if EN and PGOOD pins are not required. If EN and PGOOD pins are required, additional level-shifter circuitry must be taken into account during for PCB spin. Note that the LMZM33602 is rated for 2 A and pin-to-pin compatible with the LMZM33603.

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Trademarks

1 Inverting Buck-Boost Topology

1.1 Concept

In a standard buck configuration the positive connection (V_{OUT}) is connected to the inductor, and the return connection is connected to the device ground.

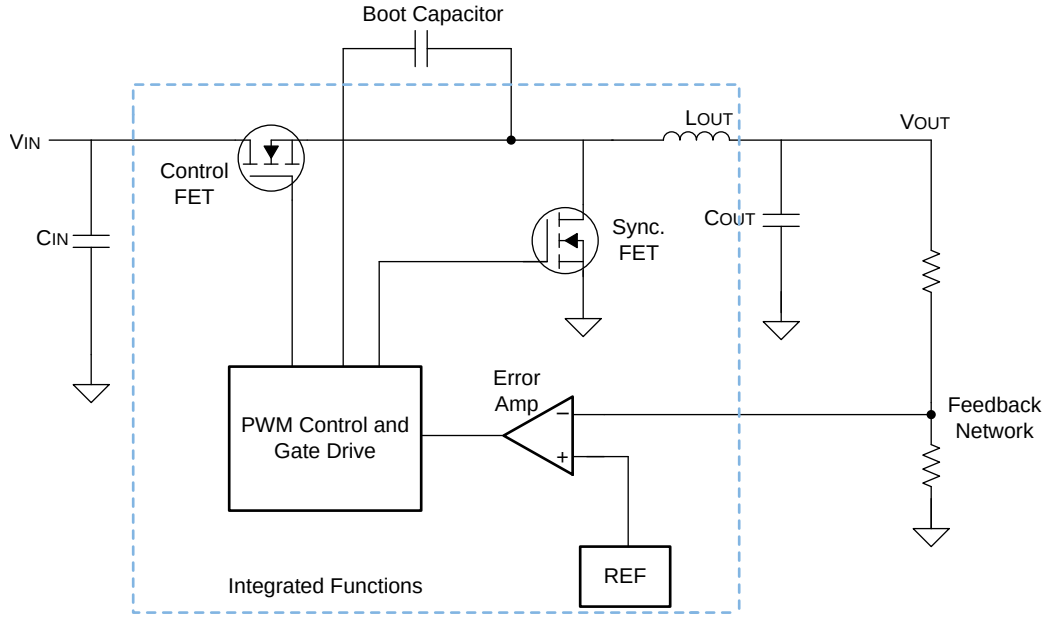


Figure 1. Buck Topology

In the IBB configuration, the device return is used as the negative output voltage pin (labeled as V_{OUT}). The positive output in the buck configuration that was previously V_{OUT} is now referenced as ground (GND). This shift in topology allows the output voltage to be inverted with respect to the input voltage.

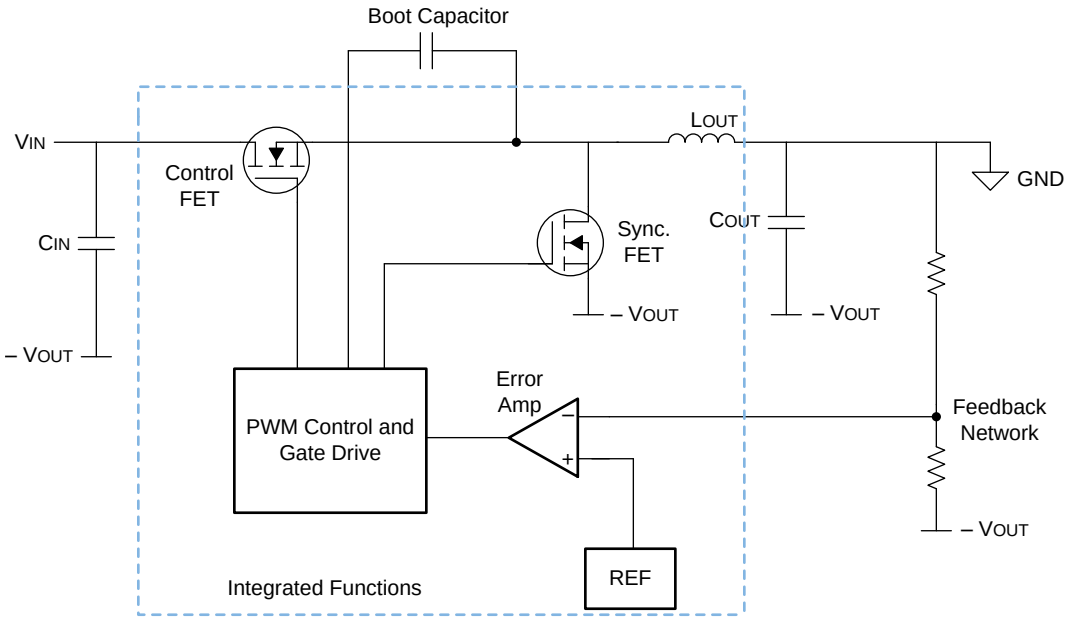


Figure 2. Inverting Buck Boost Topology

Though the components in an IBB topology are connected in the same way as with a buck topology, the output voltage terminals are reversed, as shown in (a) of Figure 3. During the *on* time of the control MOSFET, as shown in (b) of Figure 3, the inductor is energized with current, while the output capacitor supplies the load current. In this state, the inductor does not provide current to the load. During the *off* time of the control MOSFET and the *on* time of the synchronous MOSFET, as shown in (c) of **Figure 3** , the inductor provides current to the load and the output capacitor. These changes affect many parameters, as discussed in the *Design Considerations* section.

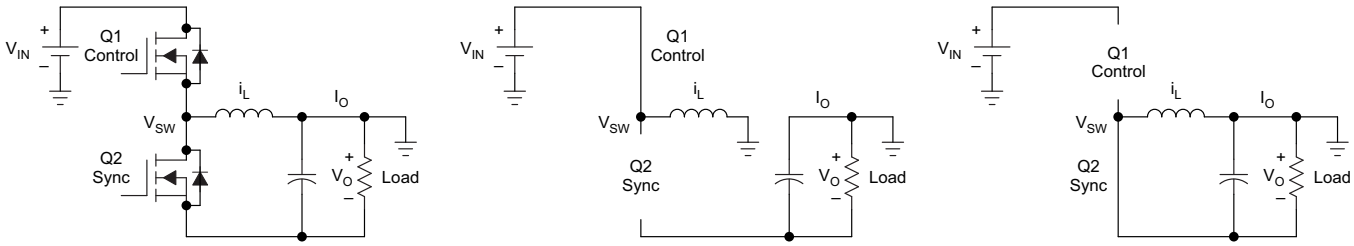


Figure 3. Buck-Boost Configuration

1.2 Output Current Calculations

By changing the buck configuration into an IBB configuration, the average inductor current is affected. In the buck configuration, the average inductor current equates to the average output current because the inductor is always supplying current to the load in both the *on* and *off* times of the high and low side FETs. In the inverting buck-boost configuration the output capacitor is completely disconnected from the inductor during the *on* time of the high-side FET and the inductor supplies current to both the output capacitor and the load during the *off* time.

The operating duty cycle for an inverting buck-boost converter can be found with Equation 1:

$$D = \frac{Vout}{Vout - Vin * \eta} \tag{1}$$

NOTE: V_{OUT} in Equation 1 is represented with a negative value.

The efficiency term in Equation 1 adjusts the equations in this section for power conversion losses and yields a more accurate maximum output current result. Given that the IBB configuration yields an efficiency range of 70% to 85%, the conservative value of 70% is used for calculating the duty cycle. For example, given a –12-V output voltage, 24-V input voltage, and 3-A maximum current rating, Equation 2 and Equation 3 calculate the recommended maximum output current.

$$D = \frac{-12}{-12V - 24 * 0.7} = 0.4166 \tag{2}$$

The result of Equation 2 is then used to calculate the maximum achievable output current:

I_{OUT} (IBB) = 3 × (1 – 0.4166) =1.75 A (3)

It is expected that the maximum output current for the LMZM33603 in the IBB topology will be lower than the typical buck topology due to the fact that the average inductor current is higher. Table 1 provides a general idea of what to expect from the modified LMZM33603. Given that the switching frequency is set at 450 kHz, Table 1 and Figure 4 show the maximum output current for the LMZM33603 IBB configuration. Table 2 and Figure 5 show the maximum output current for the LMZM33602 IBB configuration.

Table 1. Maximum Output Current Calculation for LMZM33603

V_{OUT} (V)	V_{IN} (V)	I_{L_max} (A)	η	D	I_{OUT} (A)
–2.5	24	3	0.7	0.129	2.6
–3.3	24	3	0.7	0.164	2.5
–5	24	3	0.7	0.229	2.3
–12	24	3	0.7	0.416	1.75

Figure 4 is a visual interpretation of the maximum output current table.

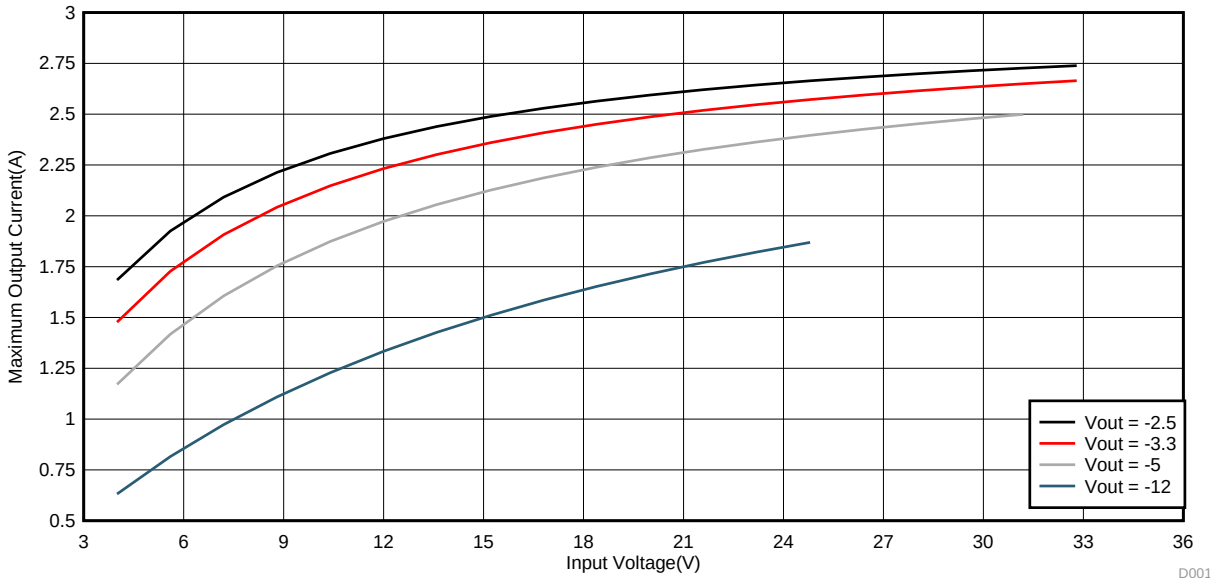


Figure 4. Recommended Maximum Output Current for LMZM33603

Table 2. Maximum Output Current Calculation for LMZM33602

V_{OUT} (V)	V_{IN} (V)	I_{L_max} (A)	η	D	I_{OUT} (A)
–2.5	24	2	0.7	0.119	1.74
–3.3	24	2	0.7	0.151	1.67
–5	24	2	0.7	0.205	1.54
–12	24	2	0.7	0.392	1.16

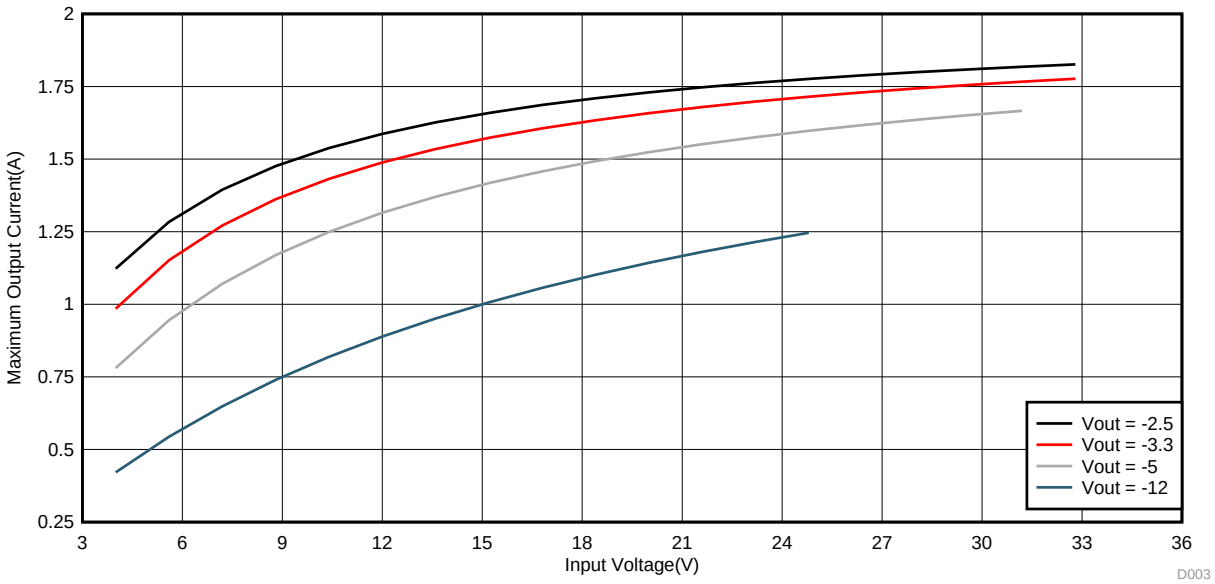


Figure 5. Recommended Maximum Output Current for LMZM33602

1.3 V_{IN} and V_{OUT} Ranges

When configured in an IBB topology, the input voltage across the module is V_{IN} to V_{OUT}, not V_{IN} to ground. To illustrate this, the modified LMZM33603 has an input voltage range from 4 V to 36 + V_{OUT}, where V_{OUT} is a negative value. The output voltage range in this topology is –1 V to –18V because the expected output is now negative. Also consider that most DC-DC converter circuits have undervoltage lockout (UVLO) circuitry and that the minimum voltage to maintain operational start-up must be above the UVLO limit even with the modified topology.

2 Design Considerations

2.1 Additional Bypass Capacitor and Schottky Diode

Add a ceramic bypass capacitor, C_{BYP}, with a minimum capacitance of 10 µF, as shown in Figure 6. The voltage rating must be taken into consideration because this capacitor will experience stress equal to the full voltage difference between V_{IN} and V_{OUT}.

Consider that the inclusion of the C_{BYP} capacitor introduces an AC path from V_{IN} to V_{OUT} and might worsen the line transient response. When V_{IN} is initially applied, this dV/dt across the bypass capacitor creates a current that must return to ground to complete the loop. This current might flow through the internal low-side body diode of the MOSFET and the inductor to return to ground. For this case, TI recommends adding a Schottky diode between V_{OUT} and GND. If large line transients are expected, increase the output capacitance to keep the output voltage within acceptable levels.

Also note that in order for the system to be stable, there must be an input power supply capacitor to help dampen the high-frequency noise that can couple onto the circuit. When using the LMZM33603EVM, the C_{BULK} capacitor connection must be modified because the IC return is no longer ground.

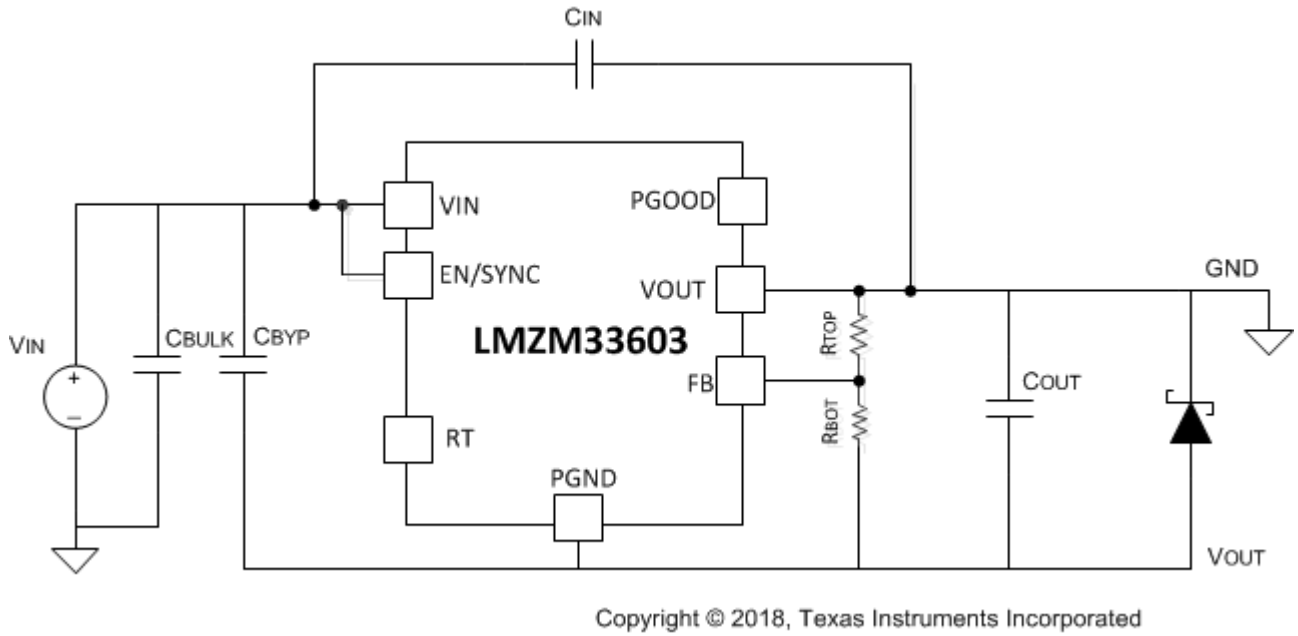


Figure 6. LMZM33603 Inverting Buck-Boost Schematic With Schottky Diode

2.2 Bode Plot Stability

Output capacitance is an important factor when considering stability of the system. For stability the phase margin(PM) of at least 45 is typically desired. Below is a table that shows the measured PM data configured IBB LMZM33603 for both 12-V and 24-V inputs under maximum load for the given output voltages. Note that this dataset is valid for switching frequency of 450 kHz and output capacitance (4 × 22 µF) of the original LMZM33603EVM.

Table 3. Measured Phase Margin of IBB Default EVM

V_{IN} (V)	V_{OUT} (V)	I_{OUT} (A)	F_{CROSS} (kHz)	PM (º)
24	-2.5	2.6	58.15	46.1
24	-3.3	2.5	43.39	62.2
24	-5	2.35	28.02	73.7
24	-12	1.8	12.05	49.2

For the 24-V input voltage application, Table 4shows that using the output capacitance of the LMZM33603EVM will satisfy PM 45º for all negative output voltage selection. LMZM33603 features hiccup mode and will fault during a maintained over current condition on the output. During hiccup mode, the LMZM33603 shuts off both the high-side and low-side MOSFET and waits for a time interval before the LMZM33603 is turned back on. If the output capacitance is too high, the output voltage takes longer to stabilize to the regulated voltage and can trip hiccup. The table below shows the maximum output capacitance recommended for the IBB converted LMZM33603. Note that the output capacitance listed takes into account DC bias effects at each specific output voltage.

Table 4. Recommended Output Capacitance For V_{IN} = 24 V

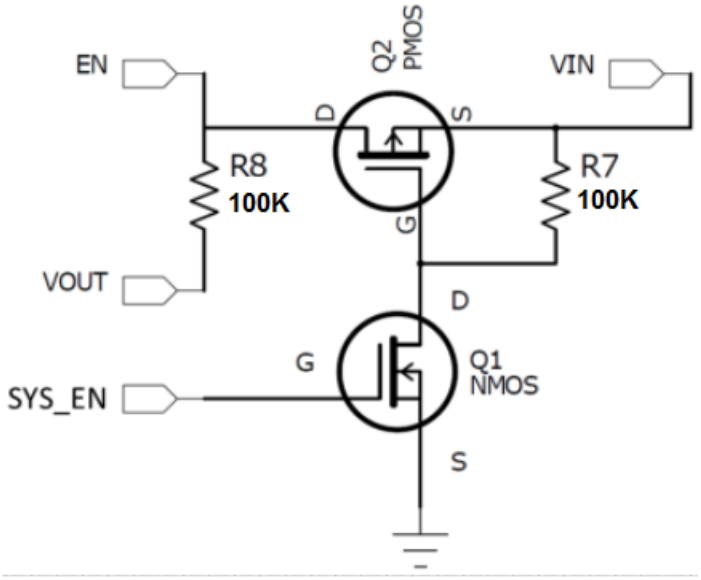
V_{IN} (V)	V_{OUT} (V)	I_{OUT} (A)	C_{OUT_MIN} (µF)	C_{OUT_MAX} ($_u$F)
24	-2.5	2.6	135	660
24	-3.3	2.5	97	530
24	-5	2.35	56	450
24	-12	1.8	22	70

2.3 Digital Pin Configurations

2.3.1 Digital Input Pin (EN)

Because V_{OUT} is the IC return in this configuration, the EN pin must be referenced to V_{OUT} instead of 0 V. In a buck configuration, the specified typical threshold voltage for the EN pin to be considered high is 1.55 V and 1.15 V is considered low. In the inverting buck-boost configuration, however, the V_{OUT} voltage is the reference; therefore, the high threshold is 1.55 V + V_{OUT}, and the low threshold is 1.15 V + V_{OUT}. For example, if V_{OUT} = –12 V, V_{EN} is considered a high for voltages above –10.45 V and a low for voltages below –10.85 V.

This behavior can cause difficulties enabling or disabling the part, becuase in some applications the IC providing the EN signal may not be able to produce negative voltages. The level shifter alleviates any problems associated with the offset EN threshold voltages by eliminating the need for negative EN signals.



VOUT is the negative output voltage of the inverting buck-boost converter

Figure 7. EN Pin Level Shifter

The positive signal that originally drove EN is instead tied to the gate of Q1 (SYS_EN). When Q1 is off (SYS_EN grounded), Q2 detects 0 V across its V_{GS} and also remains off. In this state, the EN pin detects V_{OUT}, which is below the low level threshold and disables the device.

When SYS_EN provides enough positive voltage to turn Q1 on (minimum V_{GS} as specified in the data sheet of the MOSFET), the gate of Q2 is pulled low through Q1. This drives the V_{GS} of Q2 negative and turns Q2 on. As a consequence, V_{IN} ties to EN through Q2, and the pin is above the high level threshold, causing the device to turn on. Ensure that the V_{GD} of Q2 remains within theratings of the MOSFET ratings during both enabled and disabled states. Also ensure that V_{GS} and V_{DS} ratings are not exceeded. Failing to adhere to these constraint can result in damaged MOSFETs.

The SYS_EN signal activates the enable circuit, and the G/D NODE signal represents the shared node between Q1 and Q2. The EN signal is the output of the circuit and goes from VIN to –VOUT properly enabling and disabling the device.

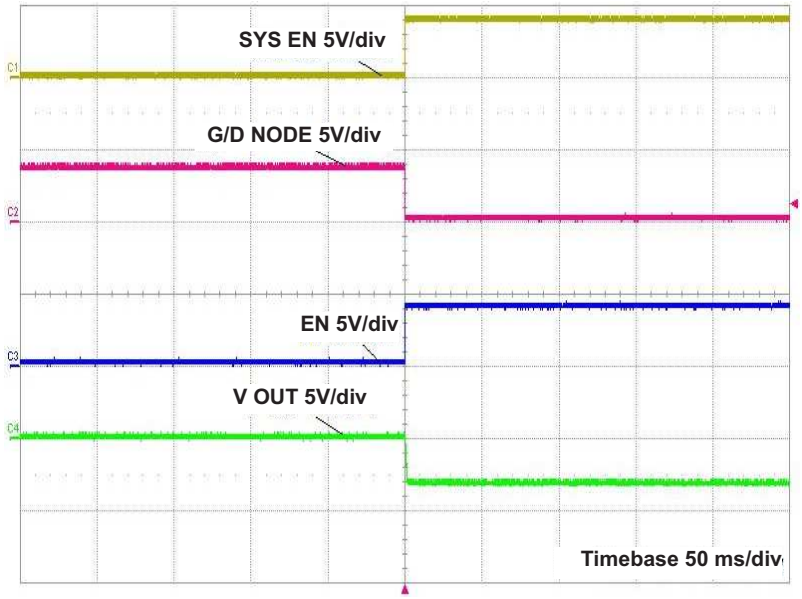


Figure 8. EN Pin Level Shifter on Start-Up

Figure 9. EN Pin Level Shifter on Shutdown

2.3.2 Power-Good Pin

The LMZM33603 has a built-in power-good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG pin is an open-drain output that requires a pullup resistor. Because V_{OUT} is the IC return in this configuration, the PG pin is referenced to V_{OUT} instead of ground, which means that the device pulls PG to V_{OUT} when it is low.

This behavior can cause difficulties in reading the state of the PG pin, because in some applications the IC detecting the polarity of the PG pin may not be able to withstand negative voltages. The level shifter circuit alleviates any difficulties associated with the offset PG pin voltages by eliminating the negative output signals of the PG pin. If the PG pin functionality is not needed, it may be left floating or connected to V_{OUT} without this circuit. Note that to avoid violating its absolute maximum rating, the PG pin must not be driven more than 12 V above the negative output voltage (IC return).

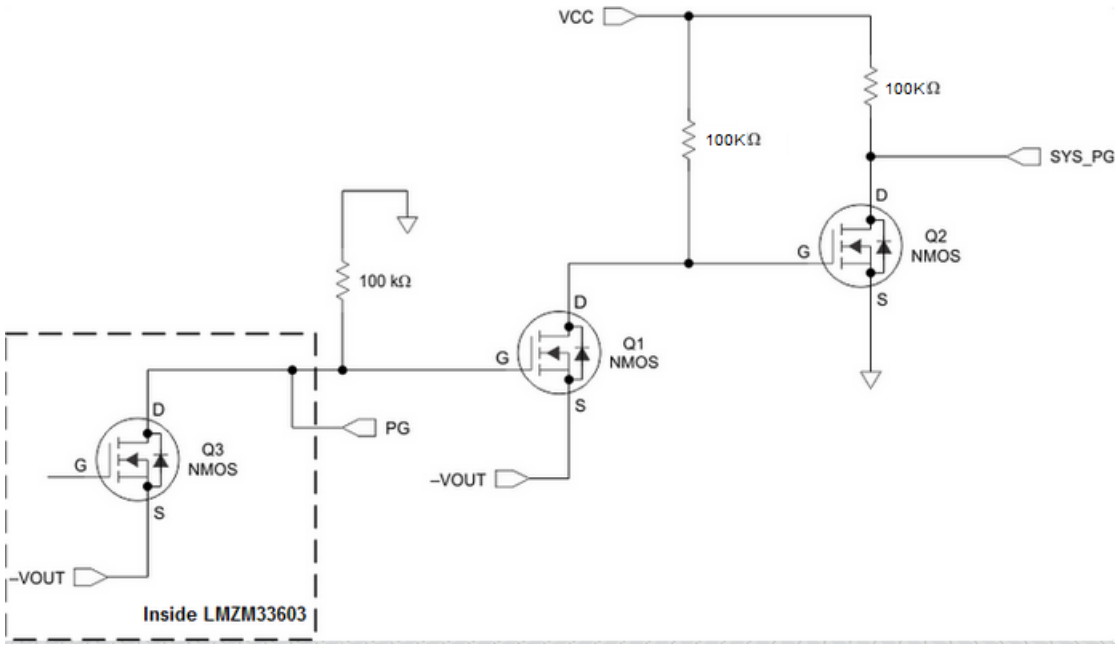
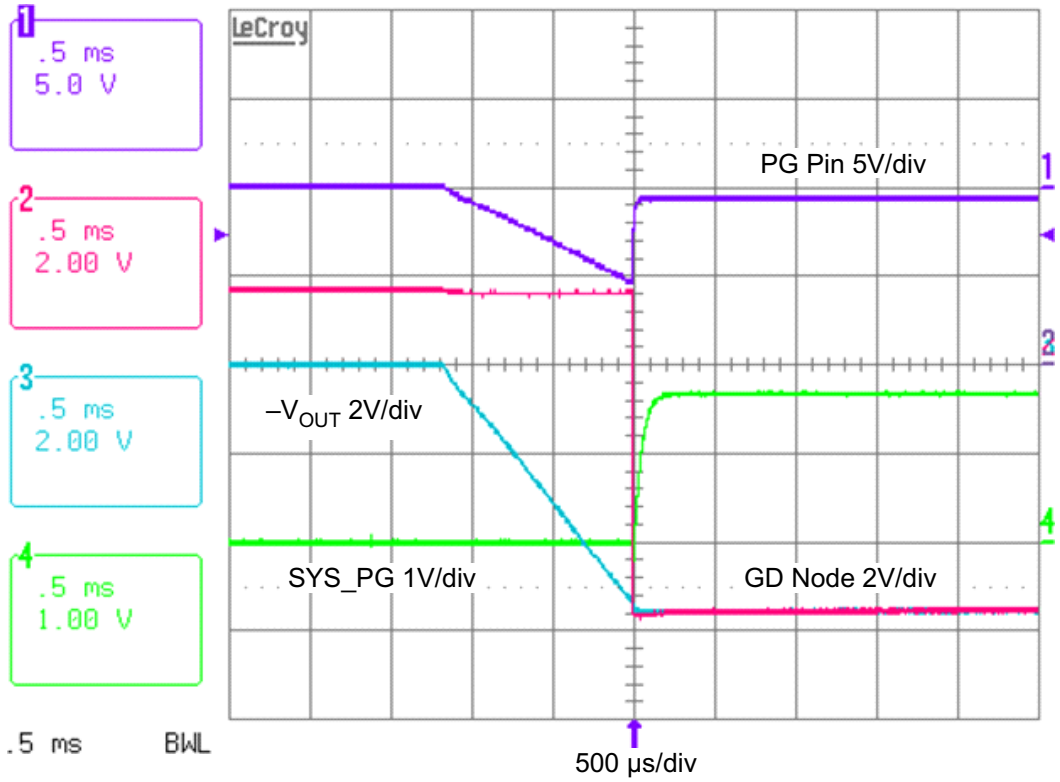


Figure 10. PG Pin Level Shifter

Inside these devices, the PG pin is connected to an N-channel MOSFET (Q3). By tying the PG pin to the gate of Q1, when the PG pin is pulled low, Q1 is off and Q2 is on because its V_{GS} detects V_{CC}. SYS_PG is then pulled to ground.

When Q3 turns off, the gate of Q1 is pulled to ground potential turning it on. This pulls the gate of Q2 below ground, turning it off. SYS_PG is then pulled up to the V_{CC} voltage. Note that the V_{CC} voltage must be at an appropriate logic level for the circuitry connected to the SYS_PG net.

This PG pin level shifter sequence is illustrated in Figure 11 and Figure 12. The PG signal activates the PG pin level shifter circuit, and the GD Node signal represents the shared node between Q1 and Q2. This circuit was tested with a V_{CC} of 1.8 V and FemtoFET CSD15830F3. The SYS_PG net is the output of the circuit that transitions between ground and 1.8 V and is easily read by a separate device.



Note that the PG pin is with respect to system return.

Figure 11. PG Pin Level Shifter on Start-Up

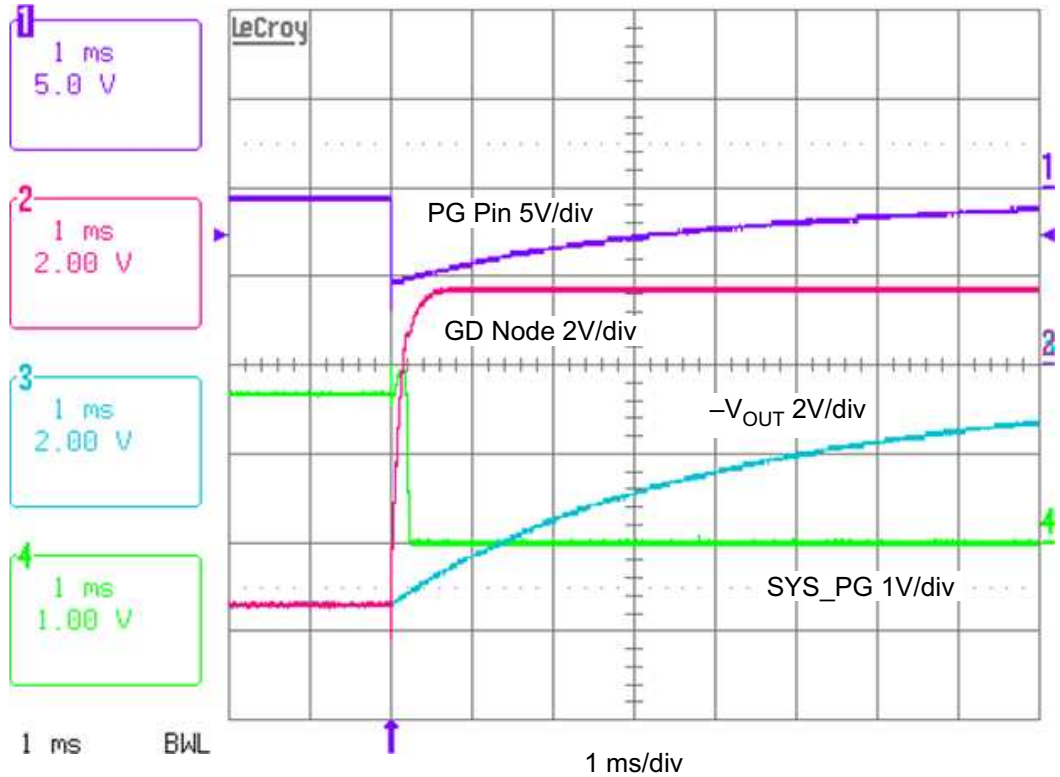


Figure 12. PG Pin Level Shifter on Shutdown

2.4 Start-up Behavior and Switching Node Consideration

The voltage on the SW pin switches from V_{IN} to V_{OUT} in an inverting topology instead of from V_{IN} to GND in a buck topology. When the high-side MOSFET is on, the SW node sees the input voltage. When low-side MOSFET is on, the SW node detects the device return, which is the output voltage. During start-up, V_{IN} rises to achieve the desired input voltage. V_{OUT} starts ramping down after the EN pin voltage exceeds its threshold level and V_{IN} exceeds its UVLO threshold. As V_{OUT} continues to ramp down, the SW node low level follows it down. Figure 13 shows the resulting normal and smooth start-up of the output voltage.

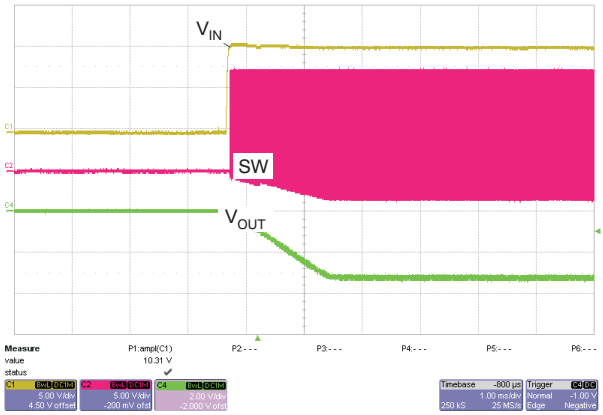


Figure 13. SW Node Voltage During Start-Up

3 External Components

The LMZM33603 power module integrates power MOSFETs and shielded inductor. As a result, this application only requires as few as four external components. TI recommends performing a load-transient test and frequency sweep to evaluate stability.

3.1 Capacitor Selection

TI recommends ceramic capacitors for low equivalent series resistance (ESR) to achieve low output voltage ripple criteria. X5R- or X7R-type dielectrics are recommended for the stable capacitance versus temperature characteristics and DC bias. The higher the DC voltage applied to the ceramic capacitor, the less the effective capacitance. TI recommends a minimum of 10-µF capacitance for both C_{BYP} and C_{IN}. For the output capacitor, see *Table 1 - Required Component Values* in the LMZM33603 data sheet. Making this capacitor value too great can prevent proper start-up operations. Evaluating the Bode plot can provide insight on the stability of the system.

4 Typical Performance

The reference design shown in Figure 14 was used to generate the typical characteristic graphs presented in this section.

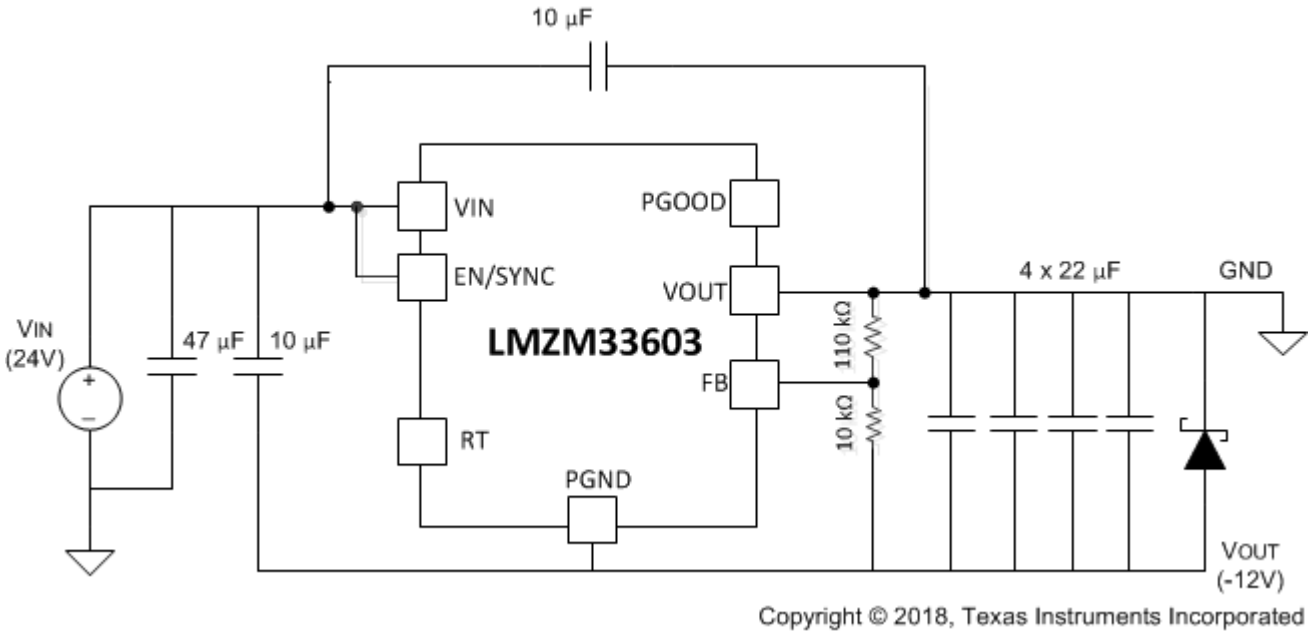


Figure 14. Schematic of Tested Circuit

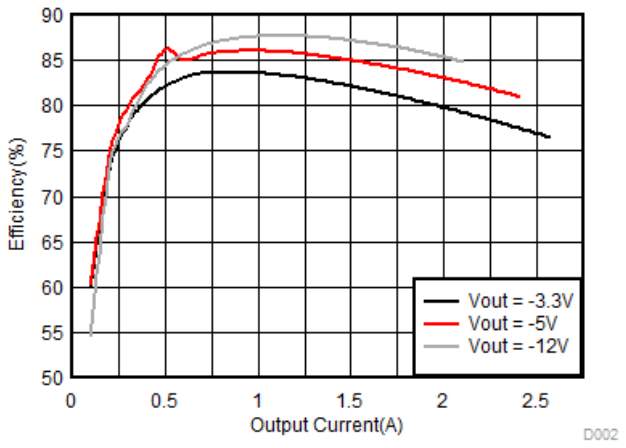


Figure 15. Efficiency vs Load Current With V_{IN} = 24 V

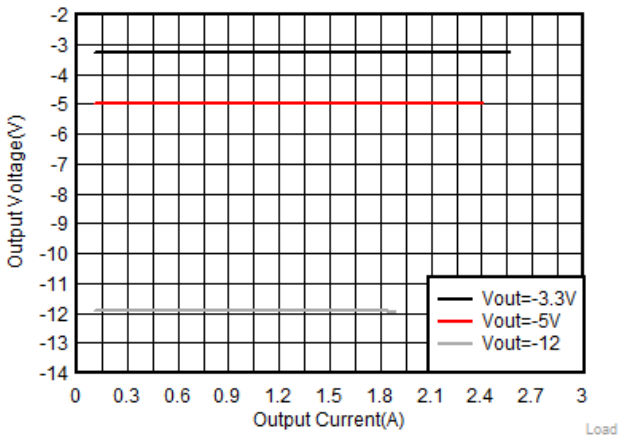


Figure 16. Load Range With V_{IN} = 24 V

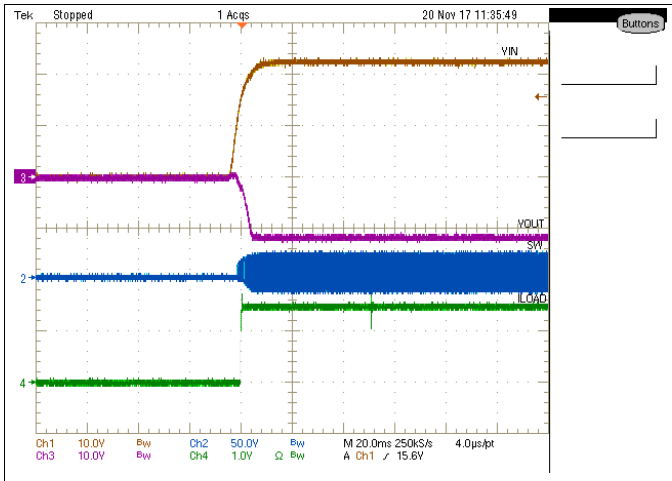


Figure 17. Start-Up on V_{IN} With 1.5-A Load

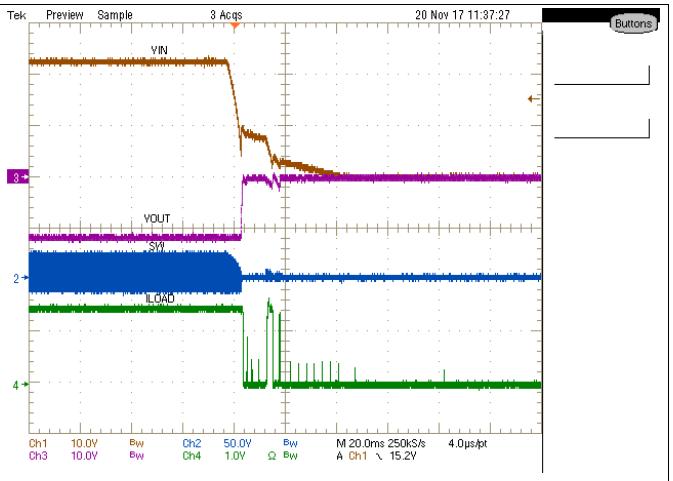


Figure 18. Shutdown on V_{IN} With 1.5-A Load

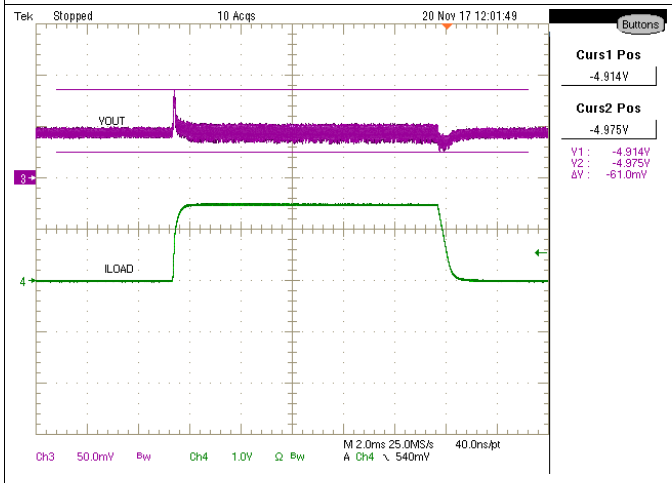


Figure 19. Load Transient Response, 0 mA to 1.5 A With V_{IN} = 12 V

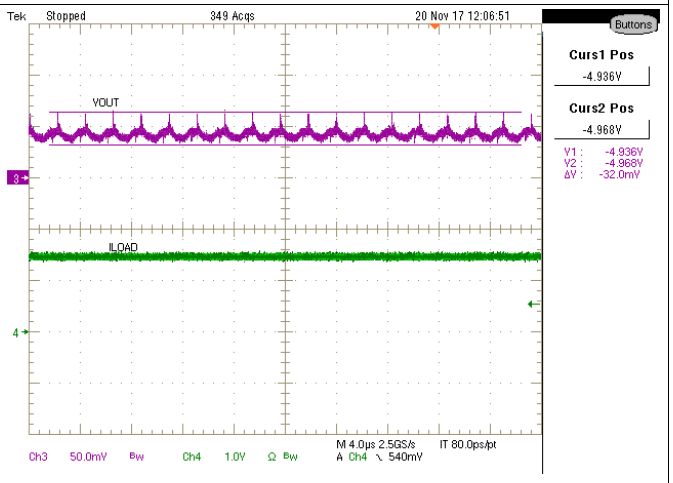


Figure 20. Output Voltage Ripple, V_{IN} = 12 V, V_{OUT} = 5 V, and I_{OUT} = 1.5 A

5 Conclusion

The LMZM33603 step-down power module can be configured in an IBB topology to generate a negative output voltage. This limits the system's input voltage range and maximum output current. The input voltage range is lowered because the device now has a reference point at negative output voltage rather than ground. Additionally, the inductor peak current is much higher effectively lowering the recommended maximum output current operating range. A spin of the PCB with additional level shifter circuitry is required if the EN and PG features are used.

6 References

The following documents are available for download from the TI web site:

1. *Create an Inverting Power Supply From a Step-Down Regulator* .
2. *LMZM33603 4-V to 36-V Input, 3-A Step-Down DC-DC Power Module in QFN Package*
3. *Using a buck converter in an inverting buck-boost topology*
4. *Using the TPS5430 as an Inverting Buck-Boost Converter*

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (February 2018) to B Revision **Page**

- Changed duty cycle equation 3
- Changed duty cycle calculation 3
- Updated values in Table 1 4
- Updated values in Table 2 4

Changes from Original (December 2017) to A Revision **Page**

- Added content to end of first paragraph 1
- Updated Figure 1 and Figure 2 2
- Updated Figure 3 3
- Changed efficiency from "0.87" to "0.85" 3
- Updated values in Table 1 3
- Changed titles of Table 1 and Figure 3; added and Figure 4 4
- Changed diode symbol in Figure 6 to Schottky diode 5
- Deleted last sentence in *Section 3* - information now elsewhere in app note; condensed *Section 3.1* 11
- Changed diode symbol in Figure 14 to Schottky diode 12
- Deleted reference no. 5 14

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