LM2633,LM2657,LM2717,LM3370,LP3906

Implementing Single-Chip FPGA Power Solutions

Literature Number: SNVA597

POWER designer

Expert tips, tricks, and techniques for powerful designs

No. 115

Implementing Single-Chip FPGA Power Solutions

— *By Hector F. Arroyo, Sr. Field Applications Engineer*

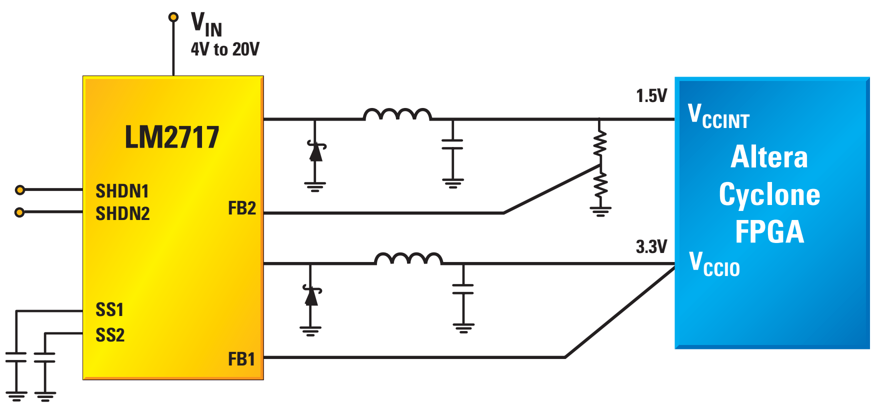

Figure 1.
LM2717 Dual Integrated Switching Supply for 1.5V Core and 3.3V I/O Medium-power FPGA

FPGA-based systems are becoming increasingly common. While many designers favor FPGA-based architectures for the flexibility of adding features or making modifications through code, designing an adequate power supply involves some challenges. First is the multiple power rail issue. FPGAs require, as a minimum, one voltage for powering the core and one (or more) voltages to power the I/O banks. However, FPGA-based systems may require additional rails to power double data rate (DDR) memory, transceivers, Ethernet Physical Layer ICs (PHYs), ADCs or small microcontrollers. Additionally, these voltage rails need to have specific characteristics: sub-1.25V outputs, monotonic ramp-up, sequencing, and controlled rise time etc.

While design engineers and semiconductor manufacturers make continuous efforts to provide integrated, easy-to-use alternatives, many times it is still up to the designer to leverage available features and go beyond the typical datasheet circuit to implement an optimal solution. Through this article, we

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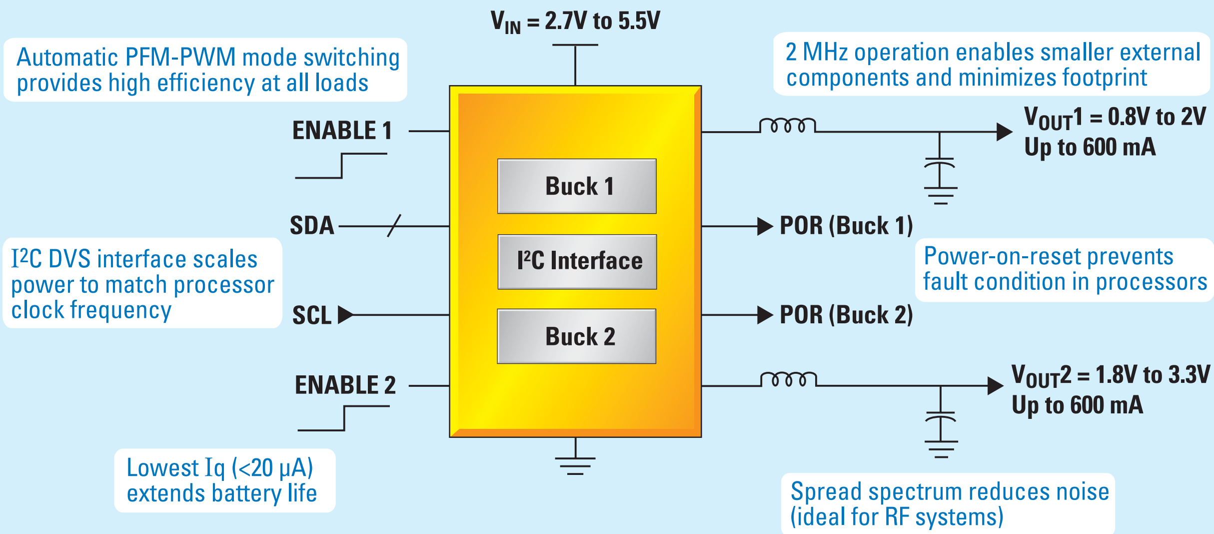
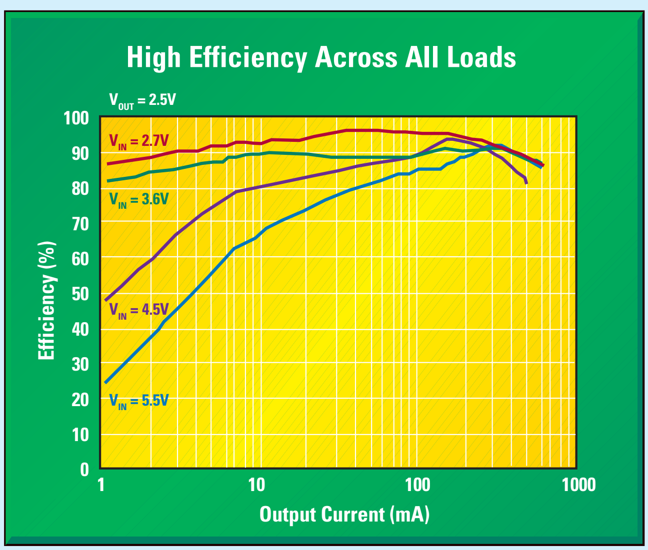
Enhance Digital Processor Power Management with Dynamic Voltage Scaling (DVS)

LM3370 Dual Buck Regulator Provides Highest Efficiency for FPGAs and Multimedia Processors



Ideal for low-power FPGAs, CPLDs, and application processors



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Implementing Single-Chip FPGA Power Solutions

will explore some available multi-output regulators that can be used as single-chip FPGA power supplies and techniques on how to implement sub-1.25V outputs from readily available bandgap regulators.

Figure 1 shows a simplified diagram of a typical application to power an FPGA (like a Cyclone device from Altera) with a single-chip power supply. National's LM2717, an integrated dual-output switching regulator IC, is set to provide 1.5V at 2A (3.2A peak) to the core and 3.3V at 1.5A (2.2A peak) to the I/Os.

The LM2717 is medium-power, single-chip solution with the simplicity and flexibility needed to implement a compact, greater than 90 percent efficient, supply matching the specifications for many digital multi-rail systems, including FPGAs, from a variety of sources: 5V, 12V or wall warts in the 4V to 20V range. The LM2717 comes with one adjustable output and one fixed output at 3.3V, a very common rail, which helps save space and increase output voltage accuracy by implementing internal output-voltage-setting resistors on this output. The LM2717-ADJ is a variation of the original LM2717 IC that allows both outputs to be adjustable, which is very useful if a different I/O voltage is needed.

Altera's literature on Cyclone and Cyclone II, as well as many other latest generation FPGAs such as Xilinx Spartan 3E, state that those FPGAs do not require any specific sequencing on their voltage rails during power-up. However, individual enable pins (SHDN1 & SHDN2) are still present on the LM2717 to turn on each output at a specific time or in a specific order should this be necessary for the system or when powering other FPGAs. In the same fashion, individual soft-start pins (SS1 and SS2) allow the LM2717 to set different ramp-up times for each output voltage to meet manufacturer specifications for individual FPGAs and other digital cores.

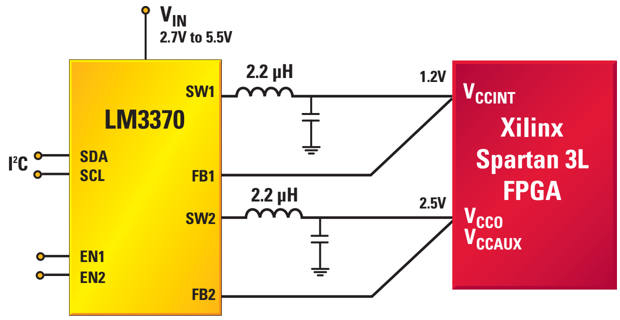

Figure 2.
LM3370 Dual Integrated Synchronous Switching Supply for 1.2V Core and 2.5V I/O and V_{CCAUX} Low-power FPGA

Figure 2 shows a low-power 1.2V, 90 nm FPGA (Spartan 3L from Xilinx) powered by the LM3370, a dual 600 mA per channel integrated synchronous buck regulator.

Voltage for one channel can be adjusted from 1V to 2V in 50 mV steps (ideal for core power) while the other channel can be programmed for an output of 1.8V to 3.3V in 100 mV steps (ideal for I/O power). Individual enable pins, internal soft-start, fast transient response, and power-on-reset flags for each output make this IC a single-chip minimum-external-components solution optimized to power low-power FPGAs and other multi-rail digital cores.

While the LM3370 can be used off-the-shelf because pre-programmed output voltages and individual enable pins are available. An on-board I²C-compatible interface allows the user to optionally modify various parameters of the IC, even dynamically, for added flexibility. These parameters include output voltage setting (per channel), output enable (per channel), switching mode selection (auto PWM-PFM for high efficiency under light-loads or fixed PWM for fixed frequency operation), spread spectrum feature enable, and spread spectrum frequency range selection.

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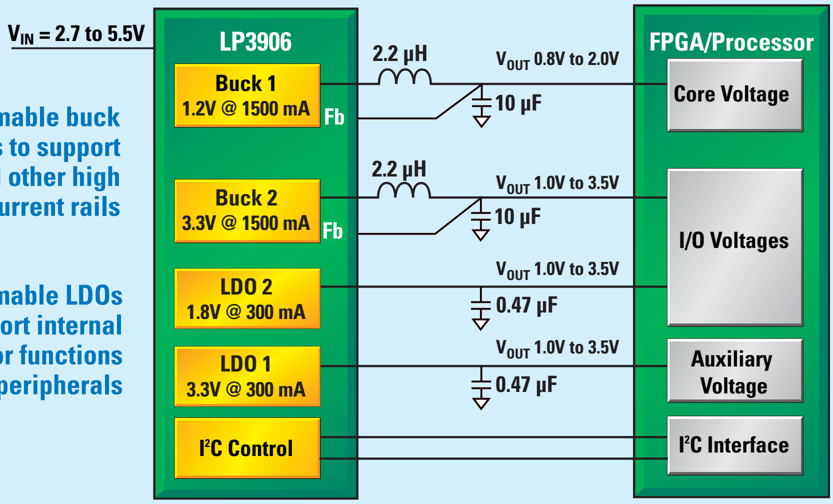
96% Efficient LP3906 Provides Flexibility with Digital Programmability



2 Programmable buck regulators to support core and other high current rails

2 Programmable LDOs to support internal processor functions and peripherals

I²C for independent control of LP3906 and peripherals

AVAILABLE LEAD-FREE

Product ID	Digitally Programmable	Efficiency	Regulator Output Current	LDO Output Current	Packaging	Solution Size
LP3906	I²C	Up to 96%	1.5 A	300 mA	LLP-24	20 mm x 20 mm
LP3905	N/A	Up to 90%	600 mA	150 mA (low noise)	LLP-14	15 mm x 10 mm

Ideal for powering application processors, FPGAs, and DSPs where size and efficiency are important

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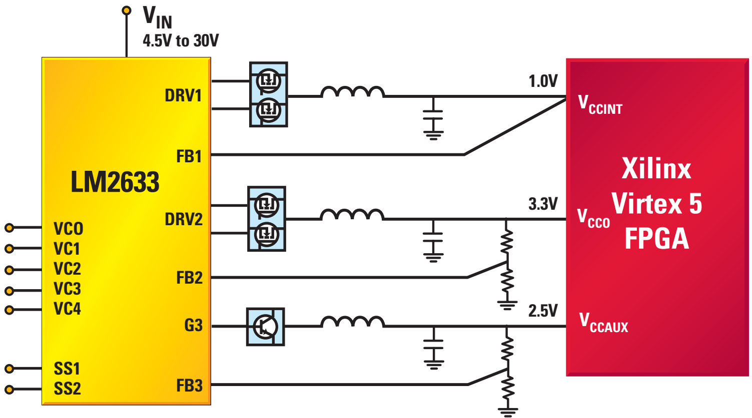


Figure 3.
LM2633 Triple Switching/Linear Controller Supply for 1.0V Core, 3.3V I/O and 2.5V V_{CCAUX} High-power FPGAs

The simplified diagram in ***Figure 3*** shows the implementation of a three-rail, higher power FPGA supply. In this case, an LM2633 controller is providing 1.0V to a Xilinx Virtex 5 core, 3.3V to the I/Os and 2.5V for V_{CCAUX}. The LM2633 is a triple output IC, and is a perfect example of how existing technology can be leveraged for new purposes, taking it out of its original context. Two of the three LM2633 outputs utilize a synchronous rectification buck architecture to provide maximum efficiency to medium and high current loads (5A to 15A per channel) while it also integrates an LDO controller for a third low-power output. One of the switching outputs has a voltage range between 0.900 and 2.000, making it a perfect fit for powering the core of digital devices. The second switching output has a range of 1.25V to 6V, adequate for I/Os, memory, and other loads. For higher accuracy and flexibility, the low voltage output is programmable through a 5-bit parallel digital word that can be either hard-wired or tied to a processor for dynamic voltage scaling if desired.

For applications where only a dual synchronous buck controller with sub-1.25V outputs is needed, the LM2657 provides a good alternative in a fewer pin-count package. For lower power applications where three or four rails are needed, the LP3906 is also an excellent alternative, providing two fully integrated 1.5A synchronous switching outputs and two 300 mA LDO outputs, all in a single package.

As seen from the previous examples, most of today's FPGAs require 1.50V, 1.20V and sometimes even a lower core voltage (as Xilinx's newest Virtex 5 series of FPGAs which have a 1.0V 65 nm core). Many regulators in the market have a regular 1.25V bandgap reference. ***Figures 4*** and ***5*** show simplified diagram examples of how to use regular bandgap ICs (like the LM2717) to power such sub-bandgap digital loads. Fundamental operation of the voltage converter remains the same, but the way in which the resistive voltage divider is referenced to program the regulator's output voltage is different.

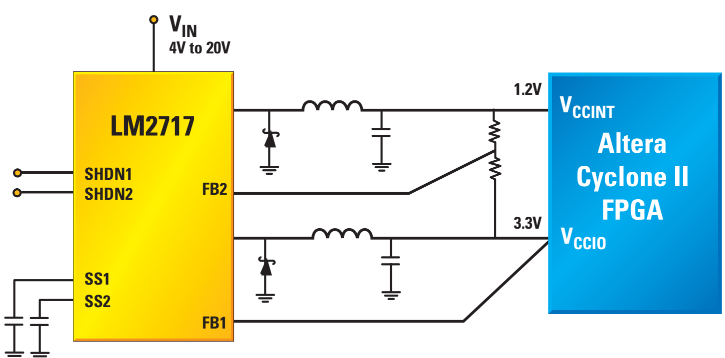
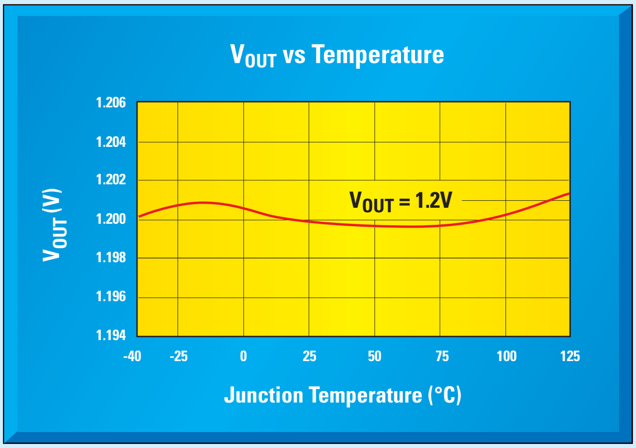
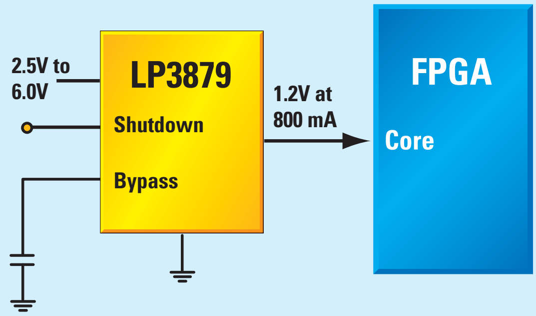


Figure 4.
LM2717 1.2V Core, 3.3V I/O Dual Integrated Switching FPGA Supply Using the 3.3V Rail as Auxiliary Voltage for Sub-1.25V Core Voltage Generation

1.2V Output LDO Enables Powering of Latest Generation Digital Cores

LP3879 800 mA LDO Provides ± 1% Initial Output Accuracy





LP3879 Features

- 1% initial output accuracy
- Input voltage: 2.5V to 6.0V
- Custom voltages available from 1.0V to 1.2V
- <10 µA quiescent current in shutdown
- Low 18 µV output noise reduces noise
- Available in PSOP-8 and LLP-8 surface mount packages

LDOs for Powering FPGAs

Product ID	V_{OUT} Range	V_{IN} Range	I_{OUT}	Features
LP38856	0.8V to 1.2V	1.3V to 5.5V*	3A	Enable Pin
LP38859	0.8V to 1.2V	1.3V to 5.5V*	3A	Soft Start Pin
LP3879	1V to 2V	2.5V to 6V	800 mA	Shutdown Pin
LP3878	1V to 5.5V	2.5V to 16V	800 mA	Adjustable Output
LP5951	1.3v to 3.3V	1.8V to 5.5V	150 mA	Low 29 µA quiescent current

* 3V to 5.5V input bias rail required

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In any closed-loop regulator circuit, the output voltage, after being scaled down by a resistor divider, is compared to an internal reference. If this reference is 1.25V, then the scaled-down sample of the output voltage, which is injected to the regulator IC through the FB pin, needs to be set to match this value to maintain regulation. In a typical system, this FB voltage divider is placed between the output (highest potential) and ground (lowest potential) since the FB voltage (1.25V) falls within this range. In a system that requires the output voltage to be below the internal reference value, we still need to provide a matching voltage (1.25V) to the FB pin, however this value won't fall now between V_{OUT} (which is now lower) and ground. The way to achieve it is by placing the voltage divider between V_{OUT} (now becoming the lowest potential and the lower end of the divider) and any auxiliary voltage above 1.25V (to serve as the higher potential).

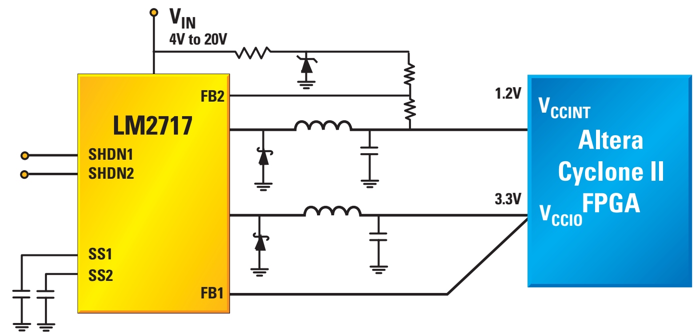


Figure 5.
LM2717 1.2V Core, 3.3V I/O Dual Integrated Switching FPGA Supply Using an LM4040 Shunt Reference for Sub-1.25V Core Voltage Generation

The example in ***Figure 4*** uses Altera's Cyclone II 1.20V FPGA and National's LM2717 to show the simplest implementation for this configuration, with the higher voltage being the 3.3V rail itself. Adequate filtering and layout for this rail is important (a decoupling ceramic capacitor close to where the resistive divider lower end meets the 3.3V rail is recommended) because regulation on the sub-bandgap output will depend on the stability of this rail. Sequencing is also important, because 3.3V rail needs to be present for proper regulation before the core voltage output is turned on.

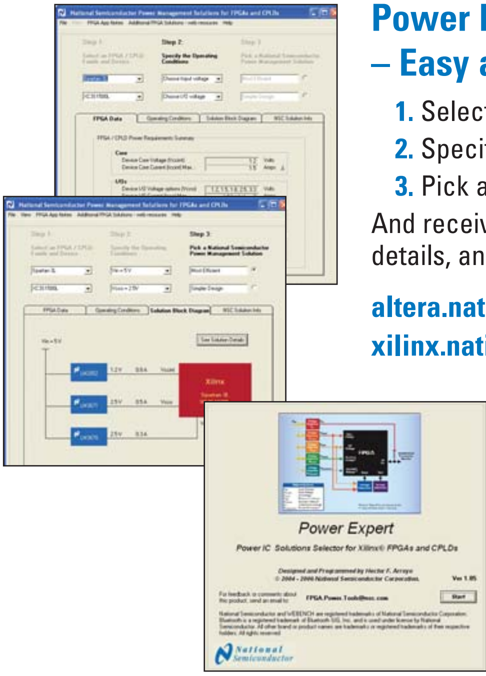
In most FPGAs, the nominal 1.20V or 1.0V core supply voltage needs to be stable within ±50 mV or ±60 mV, so all transients, ripple and tolerance variations need to be kept within that limit.

Figure 5 shows an alternate method for achieving a sub-bandgap output using an independent source for the auxiliary rail, in this case a small, low-cost shunt reference (precision Zener), such as National's LM4040CIM3-2.5 (0.5%) or LM4040DIM3-2.5 (1%). This approach allows potential transients seen in the 3.3V output not to be cross-coupled to the regulation of the 1.20V output. It also allows the 3.3V rail to be powered up after the 1.2V rail, or be turned off at any time without disturbing the 1.2V output regulation. Accuracy of this output is dependent on the line regulation of the selected voltage reference. Because core voltage accuracy is important in the application, selection of the right voltage reference is key.

Multiple resources are available today to assist designers craft the optimal power supply for their application. For example, National's Power Expert software tool, easily guides the user through selecting the FPGA of their choice, picking up the supply rails and operating conditions and finally recommending the power IC solution that matches the designers top requirements, whether these are maximum efficiency or design simplicity. It also connects to National's WEBENCH® design environment for component selection around the selected regulator IC and circuit simulation (if these features are available for the selected regulator). ■

For additional information on these tools, visit **altera.national.com** and **xilinx.national.com.**

Power Design Tools



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3. Pick a National Semiconductor power management solution

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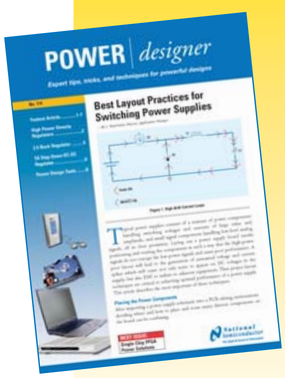

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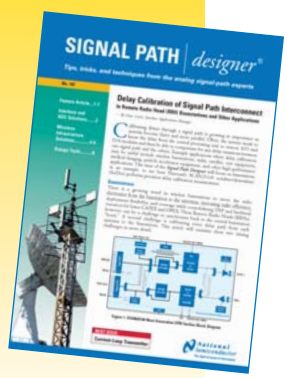

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