Parasitics can Hinder Switcher Regulator and LDO Designs

Application Report

Literature Number: SNVA689A
MAY 2013–Revised JULY 2014

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ABSTRACT

Finding solutions for the demand for point-of-load (POL) integrated switching regulators with a smaller footprint, using fewer components, and operating at higher current is challenging, especially for mobile applications. Questions generated as a result of field issues can be frustrating, even for the most experienced designers. This article means to demystify designers' concerns and to suggest ways to avoid subtle design pitfalls.

1 Introduction

Traditionally, RF and high-frequency designs were concerned with parasitics. Today, printed circuit boards (PCBs) and component parasitic elements are becoming an integral part of system designs, even for DC/DC regulator circuits. Integrated POL devices for the mobile arena are sometimes more difficult to tackle than high-power LDOs and switchers because of their smaller form factor. Also, they use smaller components, and their system-tight-fit requirements make it tougher to layout, debug, and implement changes. Recognizing these concerns, some semiconductor vendors are producing micro-power modules in an attempt to alleviate designers' frustration and help expedite their cycle time.

Consider some of the robust integrated sub-power management units (PMUs) with dual switchers and dual LDOs. Many find them perfect solutions for automotive, communication, industrial, and portable applications that require efficiency and compactness. Designing PMUs into handheld devices and compact subsystems can be challenging because of limited board space and noise opportunities that abound. It is what many vendors and mentors don't share that can get a design into trouble, making it challenging to understand why it doesn't function or meet target specifications!

This article focuses on some key layout subtleties and points out several frequently overlooked design parameters and design considerations relate to equivalent series resistance (ESR), load capacitor, vias, and feedback networks.

2 CIN Bypassing and Via Subtleties

Experienced designers should recognize that a switcher is a mixed signal device and not a digital circuit. The first issue that is evident is with supply pin bypassing. For devices with only a single VIN pin and one ground pin, the potential for functional problems is high. This is especially true when bond wires are used to bring internal analog, digital, and power rails onto the same device pin.

Consider a buck converter where the VIN pin involves a pulsed current that can be noisy from switching current through the inductor. When input bypassing becomes inadequate, the pulsed-noise ripple can be coupled into the supply rails internal to the reference generator, the error-amp, and comparator. This can cause their outputs to become modulated and noisy. The problem here is that the noise can cause these sub-circuits to make wrong decisions. A VIN pin that experiences even a couple hundred millivolts of noise being superimposed could render the converter inoperable. So what are the culprits? Primarily, they are the parasitic inductance between the bypass cap and the VIN pin. Misuse of vias and / or placement of CIN can also contribute to the problem. ESR might also be a factor, but it is less common. Do not underestimate a few millimeters of metal trace between CIN and VIN as this can make or break some designs.

A couple of nH of inductance at modestly high current and high di/dt, for example 1A/2ns, can be troublesome. Vias can introduce a relatively high inductance, as well as capacitance, and are best used for DC conduction. When high edge rate and current are involved, it is best to avoid them or use large vias liberally, if necessary. Consider some common expressions for inductance estimation as in Equation 1:

Trace inductance:

$$L = 0.2 * L * \left[\ln\left(\frac{2L}{W+H}\right) + 0.2235 * \left(\frac{W+H}{L}\right) + 0.5 \right] \text{nH} \quad (1)$$

where W, L, H are width, length, and height (metal thickness) respectively, in millimeters.

Via inductance:

$$L = \left(\frac{H}{5}\right) * \left[1 + \ln\left(\frac{4H}{D}\right)\right] \text{nH} \quad (2)$$

where H is the height and D the diameter of the via all in millimeters.

Example 1: Consider a 1.78 millimeter thick board (0.07 inches), a single via of diameter = 0.406 mm (16 mil) has L = 1.37 nH from the calculation in Equation 2. Assume use of a 2 MHz buck converter such as the LM26484 or LP3907 operating at 50 percent duty cycle and switching at 1A/2 ns edge rate. Enter these figures into the equation V= Ldi/dt = 1.37 nH*(1A/2ns) = 685 mV. This is the magnitude of switching noise that may develop on the VIN pin. If not mitigated, even a 150 mVPP transient in some buck converters could become disruptive or lead to severely degraded performance. Avoid using vias on power tracks. If absolutely necessary, use a liberal amount and choose larger diameters to reduce parasitic inductance. Managing the pulsed-current, path-induced voltage noise on I/O ports is critical. For a boost converter, the input current is smooth whereas the output current is pulsed, so output noise needs to be addressed similarly.

C_{IN} Bypassing and Metal Trace Subtleties

Example 2: Consider another non-optimal PCB layout of a stand-alone buck converter. This example involves the LM3670 buck in an application depicted in Figure 1. To improve the layout, the inductor can be shifted up a body length so one side connects to the switch node, while the other terminal butts directly to C_{OUT}. This tightens the current loop and reduces impedance and noise.

The real issue here is the C_{IN} bypass cap proximity to the VIN pin. With the present C_{IN} placement, it already is far away from the VIN pin. The additional bending introduces excessive parasitic inductance, as well as potential for radiated RF noise from the loopy routing. The 7 millimeter track length (0.9 mm wide, 0.035 mm thick PCB) plus such a profile can issue about 4.5 nH inductance when using Equation 1.

As mentioned, at relatively high current and/or fast edge rate, enough switching noise can be generated to cause problems. Typical issues include excessive output noise, large clock jitter or bi-modal clock pulses at the switching node, soft-start failure which causes output deviates from target value, or unstable output voltages give the appearance of false instability problems.

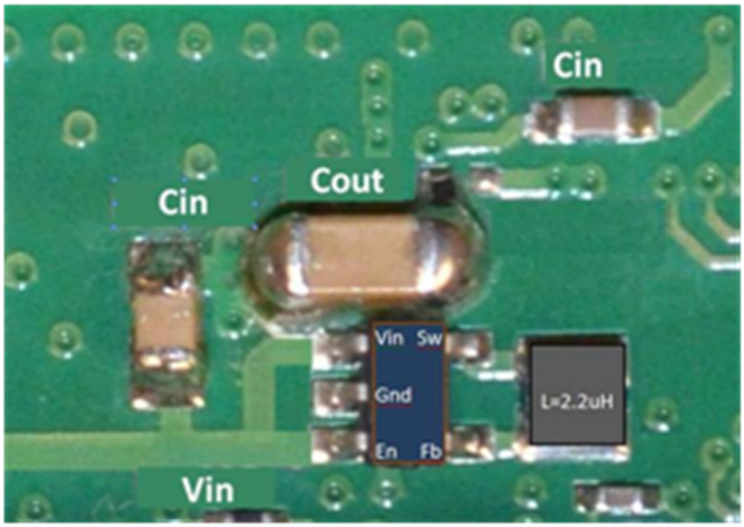

Figure 1. Step-down Converter Application PCB VIN Track Induces Excessive Parasitic Inductance

PMU Layout Subtlety Examples

In Figure 2 an additional sample PCB layouts of a dual buck, dual LDO sub-PMU application board is illustrated. It depicts a good layout that adheres to common good-layout practice and vendor recommendations. However, unnecessary or inadequate ground and power via feeds, extra power trace length induced inductance at C_{IN}, and longer high current loops layout can potentially sacrifice performance and cause issues. For example the “cross” via symbols on the GND and VIN islands should not be used, if possible. Also the metal trace between the device pins to C5 and C7 introduce potentially deleterious inductance. But this can be easily avoided with a better design. Figure 3 illustrates an enhanced re-layout that addresses the aforementioned issues. Note that V_{IN} bypass caps C5 and C7 have less trace inductance by their improved placement and removal of extraneous vias on power and ground tracks. Rotated C2 and C8 shorten traces so that C_{OUT} and L form tighter loops, thus improves efficiency and dynamic performance.

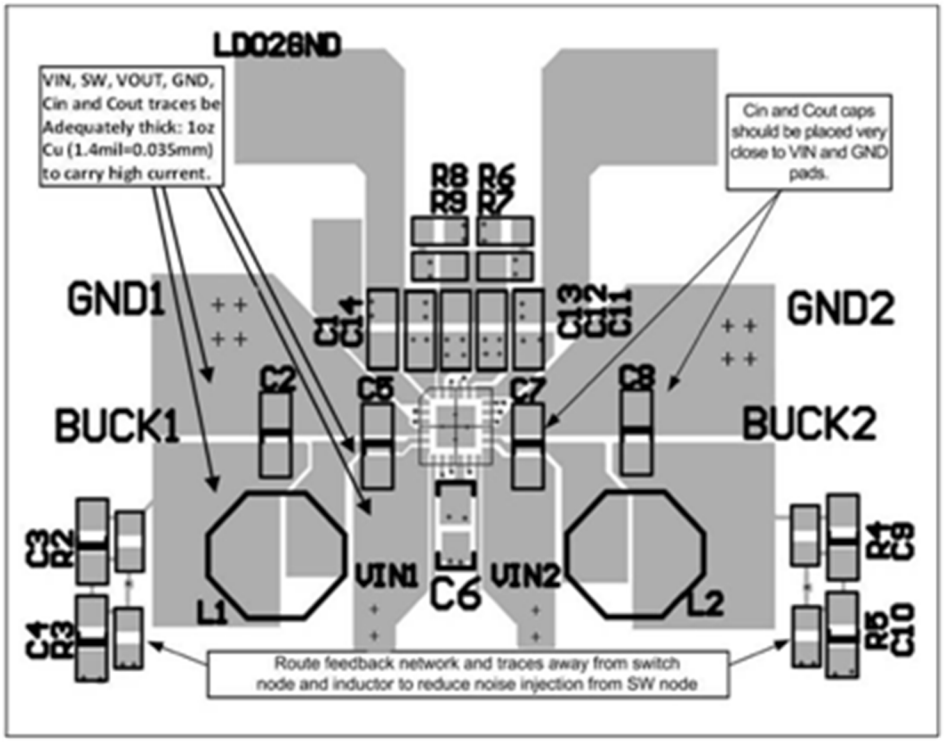

Figure 2. LM26480 PCB Bypass Caps Layout Appears Orderly and Follows Good Practice

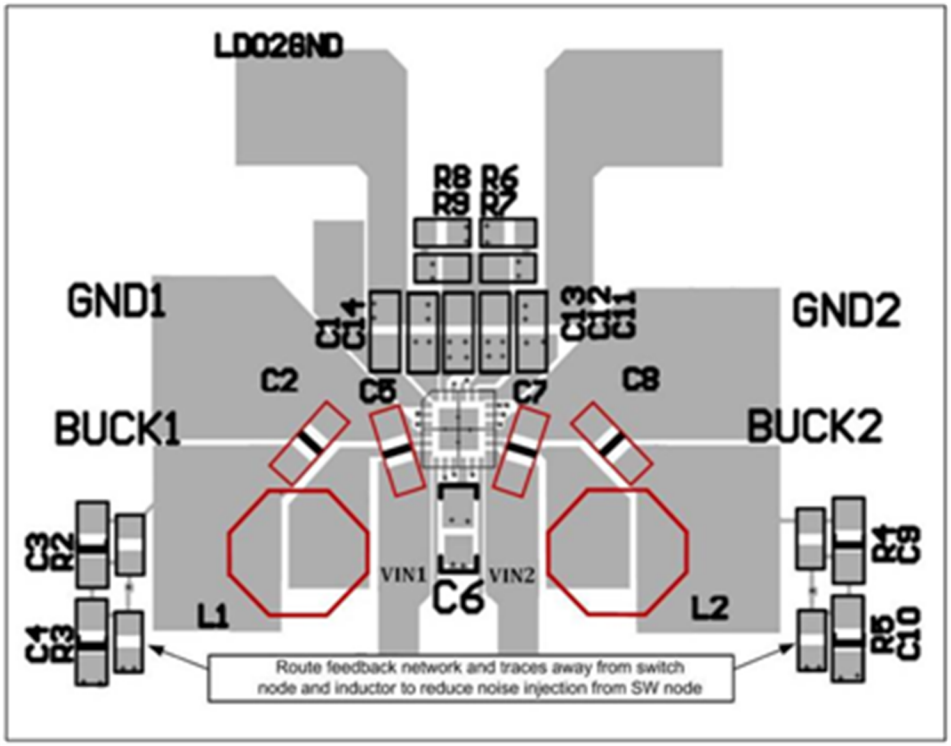

Figure 3. LM26480 in Demanding Apps - Subtle Layout of the Caps makes a Big Difference.

The examples in Figure 2 and Figure 3 clearly illustrate the importance of bypass cap layout. Regarding bypass cap layout, the axiom of the trade should be observed. Remember ACAP (as close as possible) when placing bypass cap connections to the device's supply and ground pins, and millimeter gain can deliver the desired performance. Another design issue that relates to bypassing oversight is electrical overstress (EOS). Mobile devices typically are specified at 5.5V maximum. This includes peak voltage due to transient from rail inductance in conjunction with high current edge rates. When peak voltage overshoots the maximum limit, over time the accumulated overstress could destroy the device.

To prevent EOS from occurring, it is imperative that parasitic trace inductance be minimized from the bypass cap to the supply pins. Adequate bulk caps on-board should be provided as necessary besides the recommended bypassing components. They must adequately cover a broad bandwidth and be strategically placed. A note of caution: do not let PCB vendors convince you that your layout cannot meet their "manufacturing and design rules." Sometimes performance takes precedence over conventional placement technique and appearance. If not satisfied with the results, seek other vendors who are willing to invest effort and resources to solve your problems and to advance the art and engineering solutions for tomorrow's needs.

External Adjustable Devices: C_{FF} and C_{BP}

Some switchers and LDOs have external feedback resistors and feed-forward caps. They appear counterproductive as the trend favors higher integration solutions. Folding passive components on-chip saves cost and board space, and obviates potential mismatching issues where external current and voltage setting components can be problematic.

However, there is a definite need to employ external components. This allows flexibility, customization, and facilitates production. With external adjustable devices, designs can achieve an infinite selection of voltage, current, frequency, and compensation target needs quickly and cost effectively that otherwise might not be obtained. But, if not designed with care, this solution can potentially lead to performance and instability issues. As with any product design and specification, there is a balance between tradeoffs and compromises. So what are the feedback and feed forward networks in an adjustable part all about? Figure 4 depicts a typical set of output external support components necessary for any given externally adjustable regulator, linear or switched type.

The external network gives additional poles and zeros. Rfb1 and Rfb2 are the feedback resistors to establish the target output voltage. C_{FF} is the feed forward capacitor. In conjunction with Rfb1, they form a zero that tends to advance the loop phase used for stability and ripple reduction. C_{BP} is a high-frequency bypass cap which helps to reject noise at the feedback node. This enhances performance and stability, and forms a parasitic pole with Rb2. Load cap, C_{OUT}, has an equivalent series resistance (ESR), and the two forms another zero. Thus, ESR plays a dominant role in stability and transient response. Lastly, C_{OUT} and R_{LOAD} make up the load pole, which also affects loop stability. In particular, loading changes can cause load-pole shifts that can either help or hinder stability.

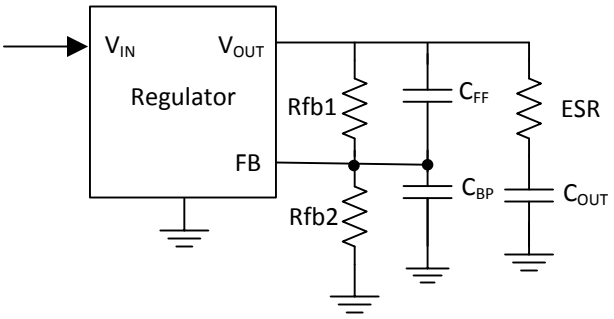

Figure 4. Typical Regulator Output External Feedback and Load Support Components

Some common issues associated with external networks are board parasitic capacitance affecting C_{FF} and C_{BP}. Without dwelling on the transfer function of the entire loop, you can appreciate the role C_{FF} and R_{FB} play by recognizing the poles and zeroes they contribute: fz = [1/(2π*Rfb1*C_{FF})] and fp = [1/(2π* C_{FF}*(Rfb1//Rfb2)-1)].

Effectively, fz boosts the high-frequency loop gain to aid transient response and stability. Consider C_{FF}, thought of as an AC short element to counter ripple and noise signals riding on V_{OUT}. With reduced noise signal on the output, the feedback resistors scale the DC output without the AC component. This eliminates an error term, which improves output accuracy and ripple performance.

Similarly, C_{BP} can be viewed as an AC shunt on a noisy signal coupled onto the feedback node. It helps averaging a cleaner feedback potential to the error-amp results which also improves output accuracy. For mobile applications, C_{FF} and C_{BP} values typically are in the order of tens of pF. Depending on the design and material of a PCB, board capacitance can approach the range of C_{FF} values used and may result in output oscillation and instability phenomenon. In such circumstances, the C_{FF} value must be reduced accordingly.

Figure 5 and Figure 6 demonstrate the result of an excessive C_{FF} case where the system clock edge becomes jittery, and output has a large AC component riding on it respectively (suggested value is 12 pF typical). This is one of those seemingly inexplicable phenomenon encountered in manufacturing. When the value of C_{FF} is reduced, or when it is not installed, the phenomenon is resolved (see Figure 7 and Figure 8). Another infrequently encountered phenomenon is that when the output voltage becomes lower than the target value, due to large output ripple and/or noise on V_{OUT}. The remedy is to trim C_{FF} or increase C_{BP}.

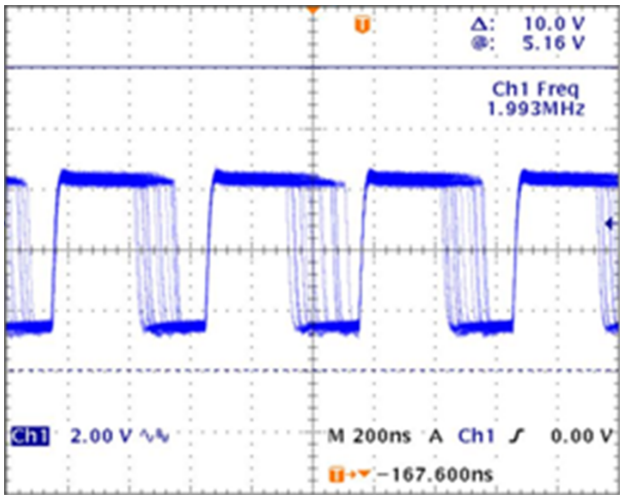

Figure 5. Switch Clock Excessive Jitter from PCB Parasitic in Manufacturing Subtlety

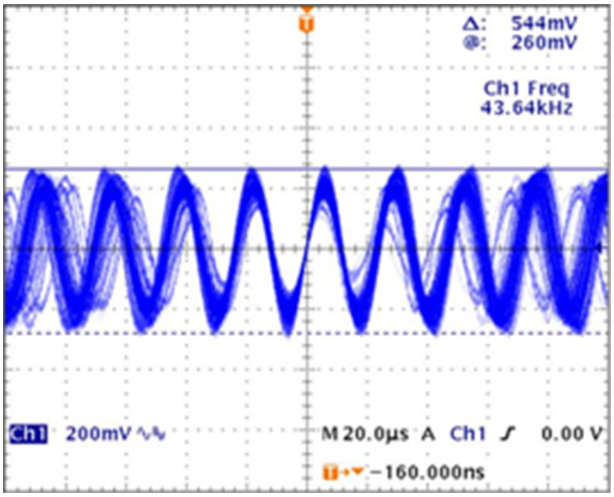

Figure 6. Noisy and Large Ripple on V_{OUT} and V_{IN} can Plague Designs due to Parasitics

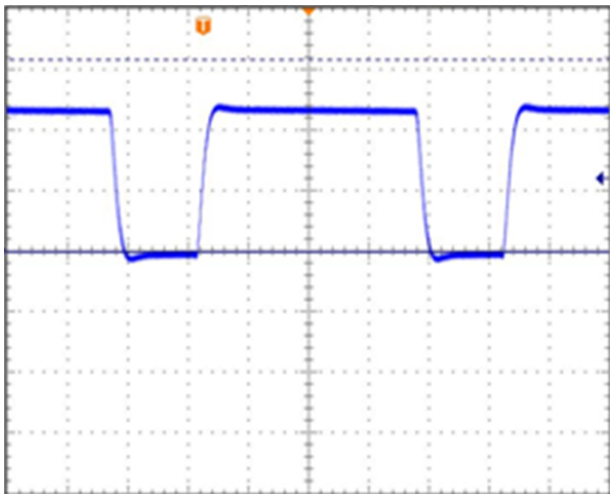

Figure 7. Clean Switch Clock Results When the Subtle Culprit is Identified (C_{FF} in this case)

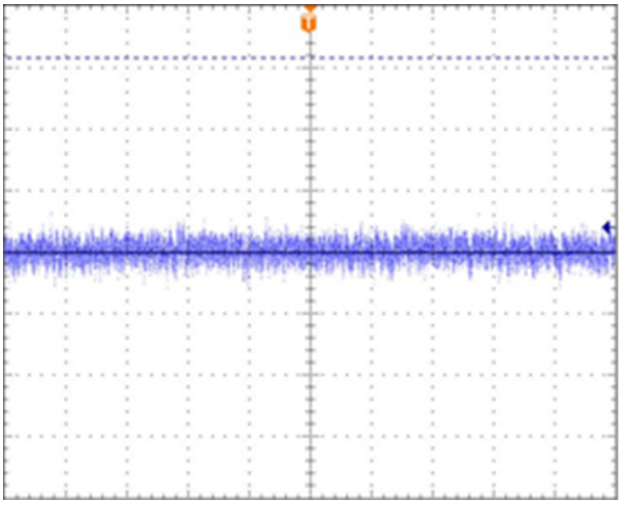

Figure 8. Output Becomes Clean When Component and Manufacturing Issues are Remedied

C_{OUT} ESR and ESL Affect Loop Stability and Response

Ceramic capacitors with X5R and X7R dielectrics require less phase and gain margin versus electrolytic type due to less parameter variations. Ceramic capacitors significantly decrease the size and cost of the output filter because of their low ripple merit. They offer compact footprint and typically very low ESR and ESL. The parasitic load zero (Fzesr) and pole (Fpesr) contributed by the load cap's ESR, however, can be significant.

When ESR changes, both Fzesr and Fpesr are shifted upward or downward; the loop stability is affected. This applies to switchers and LDO alike. Regulator vendors often issue a recommended ESR value range to ensure users follow their suggested stable region of ESR employed values for their design. Data sheets may guide the designers to select the lowest ESR value for best transient response. Conversely, vendor's application notes might suggest designers choose an adequately large ESR value to assure stability. Which is correct? Actually, they are both right.

From a transient point of view, it is important to minimize the amount of ESR. However, since the ESR and output capacitance form a dominant pole in the compensation (particularly in the case of most LDOs), some finite amount of ESR is usually required to guarantee stability. So in practice, design is ALWAYS a compromise to tailor toward one's prioritized targets. Additionally, parasitic elements from PCB layout may increase the ESR and ESL at C_{OUT}, which can critically affect the regulator's transient response and performance. The ESR * C_{OUT} product [for example, 1/(2pi * ESR * C_{OUT})] offers a convenient figure of merit for stability concerns. It allows a quick estimation of whether it may be too close to the switching frequency (FSW), the dominant pole, or affect adjacent poles and zeros.

What are Your Switcher ESR and ESL Budgets?

For a given design with a desirable transient response target, let's estimate them as:

1. ESL: From the expression of voltage develop across an inductor, V=Ldi/dt , it can be transposed to ESL = $\Delta V_{DROPMAX}$ / (ΔI/Δtime rise). This gives the allowable ESL for a given design, where $\Delta V_{DROPMAX}$ is the maximum voltage excursion budget allowed for a given load current step, ΔI is the magnitude of the load current step, and Δtime rise is the rise time of the current step.
2. To obtain the ESR figure, derive the voltage droop due to the COUT: From the expression of current traversing through a capacitor, I=Cdv/dt, it can be rewritten to V_{DROOP} = ΔI *Δt/C_{OUT}, where ΔI is the magnitude of the load current step, and Δt is the response time of the regulator. (Δt is an apriori quantity; unfortunately, one usually needs it to have knowledge of it, or determine it empirically.) For a first order estimate, utilize the system's loop bandwidth, FBW. (Typically this is 1/10 to 1/5 of the FSW. Converting FBW to the time constant sought, τ = 1/(2πFBW) = Δt).
3. ESR: The transient voltage excursion involved is the difference between the voltage expressions from the above derivation. ESR = ($\Delta V_{DROPMAX}$– V_{DROOP}) / ΔI, which gives the maximum allowable ESR target for the given design.

ESR and ESL on Output Cap Concerns

ESL can change by a factor of two or more over frequency, while ESR is rather tame, comparatively. ESR is quite flat over frequency and varies at no more than 10 to 20 percent over frequency. However, ESR can vary a lot over operating conditions. That is why data sheets may specify ESR for the load cap over a range of 100:1. The reason is for adequate coverage of stability and performance concerns regarding the position of the load zero and the effects from temperature, bias, and frequency.

A governing expression of ESR for capacitor is:

$$ESR = \text{dissipation factor} / 2\pi * \text{Freq} * \text{Cap} \quad (3)$$

From Equation 3, you can see that ESR depends on frequency, capacitance, and dissipation factor (DF). DF relates to the materials, construction, process, etc., in the making of the ceramic cap. In C_{OUT} ESR selection for a switcher design, one generally uses the manufacturer's characteristic curve on ESR versus frequency to determine the target value required. (For LDO applications, there is practically no frequency parameter involved. Hence, the values picked may correspond to DC or the lowest frequency.) Other parameters that can affect ESR are often overlooked. For instance, temperature can change DF profoundly, as much as 10X at cold temp.

Unless a product is designed for controlled ambient operation, particular attention must be paid when selecting capacitors for very low-temperature operation. This is to ensure the design is functional and stable over temperature, and meets static and dynamic performance targets over the temperature range of operation. Another important temperature effect on ceramic capacitors is that ceramic caps can exhibit a reduction of capacitance, by as much as –50%, at cold temperature operation. This is yet another consideration that some designers often overlook when specifying C_{OUT} for stability and ripple performance over temperature.

Summary

Most switcher and LDO data sheets or their related application reports/user guides contain PCB guidelines and recommendations, or relevant references to help designers craft a suitable layout to achieve optimal system performance. Unfortunately, some notes and suggestions are regurgitated from generalized textbook guidelines, past industrial publications, or copied and pasted from another data sheet. Sometimes, documents neglect to address the shrinking form factor, fine-pitch packaging, new materials,

and higher speed/edge rate involved in today's integrated power devices. Thus, the supposedly useful information conveyed might be too general or antiquated, and fail to take into account the seemingly negligible parasitic elements that can manifest large ripple noise and stress from fast-edge switching and fine track-width designs. Furthermore, temperature and bias effects on passives are crucial design considerations that often are neglected and can lead to stability and dynamic response issues.

This article presented common oversights and discussed inadequate information from component vendors that may confound even the most experienced system engineer and power designers. A detailed review on ESR, ESL, and feedback network is included to help readers become aware of their system impact. In general PCB layout designs and external components are more prone to affect system stability than the integrated circuits. Real case examples are illustrated with diagrams and waveforms to facilitate understanding of the underlining issues. Companion solutions and design techniques for improving board design and avoiding common application perils are also discussed.

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Revision History

Changes from Original (May 2013) to A Revision	Page
• Changed caption for Figure 6	7

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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