AN-1715 LP3943/LP3944 as a GPIO Expander

ABSTRACT

This application report describes how to use LP3943/44 as a general-purpose input/output (GPIO) expander. It is recommended that circuit data sheets are read first and used in conjunction with this document.

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1 General Description

LP3943/44 are integrated LED drivers with SMBUS/I^{2}C compatible interface. They have open drain outputs with 25 mA maximum output current. LP3943 has 16 outputs while LP3944 has 8 outputs. The state of the outputs can be read through output status registers. This enables the use of LP3943/44 as a general purpose input output (GPIO) expander. To enable output high pull-up resistors are required for all LED outputs that are going to be used as digital outputs. This is due to open drain configuration of the LED outputs. LP3943/44 also have two programmable pulse width modulation (PWM) generators that can freely be set to control any of the outputs.

2 Features

- SMBUS/I^{2}C to Parallel input/output expander
- 16 (8) Open drain outputs that can be used as GPIO pins
- Two programmable PWM generators that can be linked to any outputs
- 3 programmable SMBUS/I^{2}C address pins allows 8 different addresses
- 2.3 V to 5.5 V operating voltage
- Reset input
- QFN24 Package

3 Typical Application Circuit

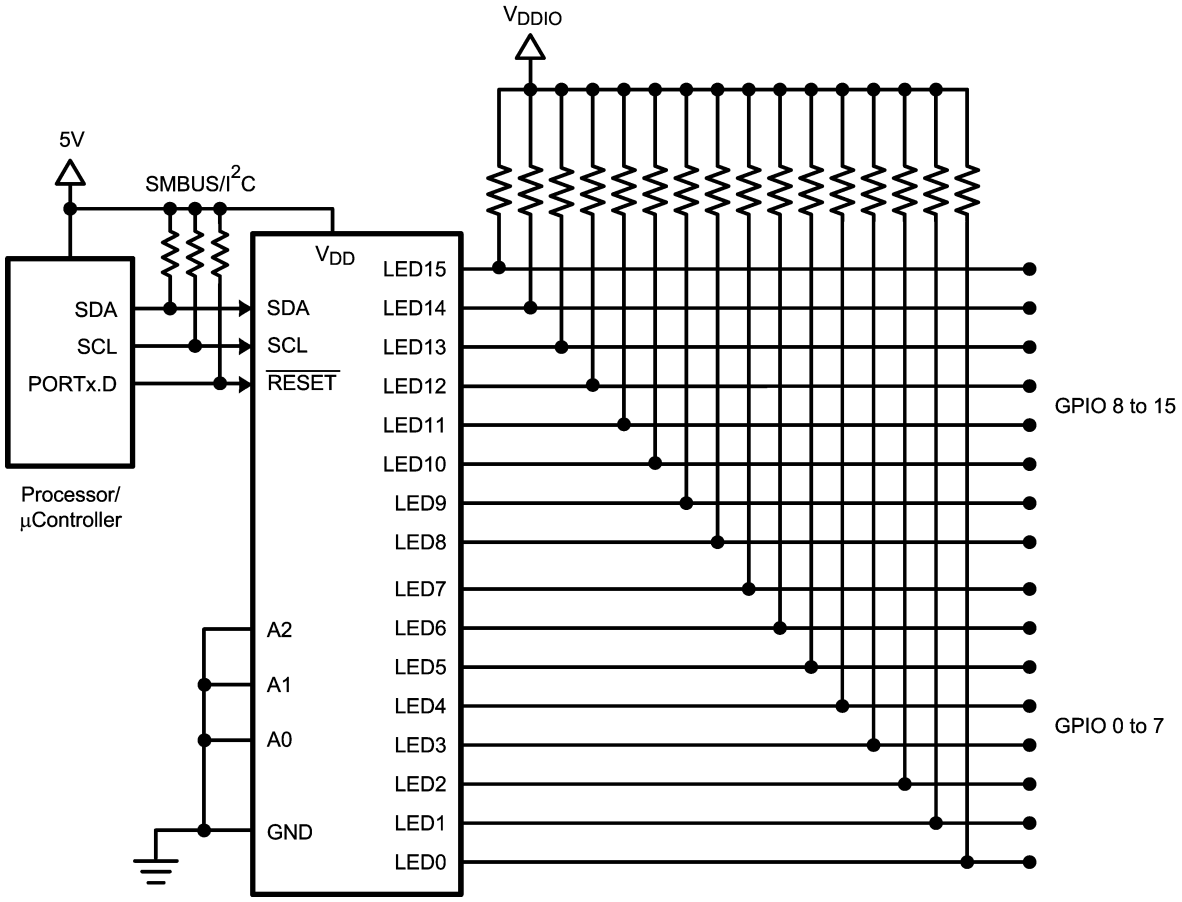

Figure 1. LP3943 Configured to 16 Channel GPIO Expander

4 Block Diagram

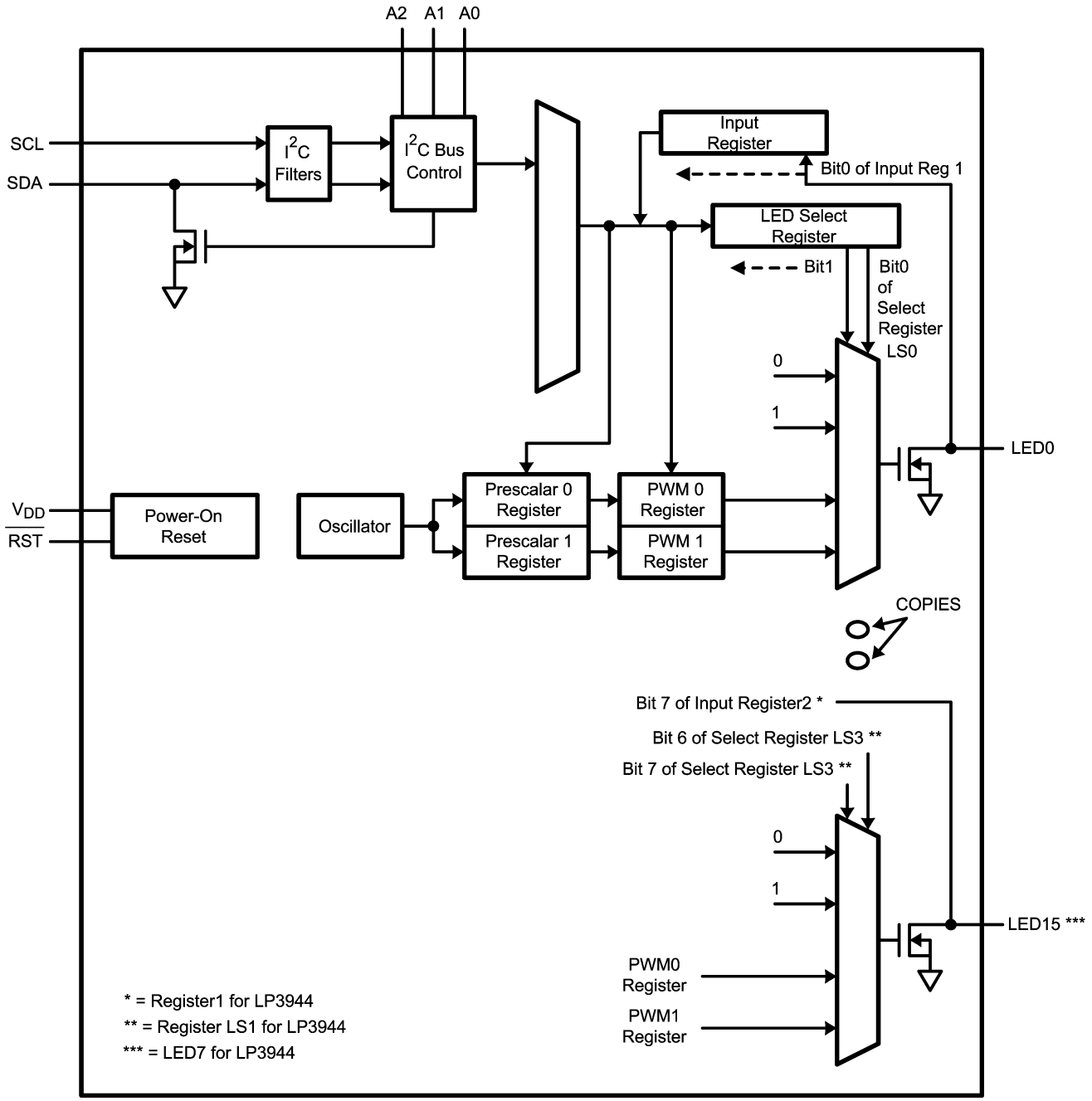

Figure 2. LP3943/44 Block Diagram

5 Register Table

When used only as GPIO expander registers, 0x00 to 0x01 (0x00 for LP3944) and 0x06 to 0x09 (0x06 to 0x07 for LP3944) are of interest. Registers 0x00 and 0x01 are used to read the status of the I/Os. Registers 0x06 to 0x09 are used to control the status of the outputs. However, all outputs do not have to be set as GPIOs. Some of them can be set to drive LEDs or used as PWM generators. When used in this kind of mixed mode configuration register, 0x02 to 0x05 are used for programing the PWM generators.

Table 1. LP3943/44 Register Table [(1)]

Address	Register Name (LP3944)	Read/Write	Function (LP3944)
0x00	Input 1	Read Only	LED0 to 7 Input Register
0x01	Input 2 (Register 1)	Read Only	LED 8 to 17 Input Register (None)
0x02	PSC0	R/W	Frequency Prescaler 0
0x03	PWM0	R/W	PWM Register 0
0x04	PSC1	R/W	Frequency Prescaler 1
0x05	PWM1	R/W	PWM Register 1
0x06	LS0	R/W	LED0-3 Selector
0x07	LS1	R/W	LED4-7 Selector
0x08	LS2 (Register 8)	R/W	LED8-11 Selector (None)
0x09	LS3 (Register 9)	R/W	LED12-15 Selector (None)

(1) Where registers of the devices differ LP3944 registers are shown in brackets. For more detailed register explanation, see the device-specific data sheets.

6 SMBUS/ I²C Interface

The SMBUS/I²C bus is a multi-master serial interface designed to connect low speed peripherals to a microcontroller. SMBUS/I²C uses only two bidirectional open-drain lines: Serial Data (SDA) and Serial Clock (SCL). Both lines need to be connected to a positive power supply with pull-up resistors. SMBUS/I²C bus uses a 7-bit address space. The LP3943/44 has four static address bits and three bits are selectable with address select inputs. This allows up to 8 LP3943/44s to be connected to a single SMBUS/I²C bus. For detailed information on how to control LP3943/44 with SMBUS/I²C bus, see the device-specific data sheet.

7 I/O Ports

The LP3943's 16 open drain outputs (8 outputs in LP3944) are entirely independent and can be used as inputs or outputs as you prefer. When used as signal outputs, the open drain structure can not produce the logic high state. For this reason, all output ports need a pull-up resistor to enable both signal levels. Pull-up resistors can be connected to different voltage level than the circuit to create a simple level shifting. When used as inputs, pull-up resistors are not required if the feeding circuitry can produce both signal levels at adequate levels.

LP3943/44 outputs have four different states as described in the data sheet. Two of these states are used when outputs are configured as GPIOs: Hi-Z and output LOW. When used as output with pull-up resistors, Hi-Z equals to logic high and output LOW to logic low. When outputs are configured to inputs, the output state needs to be set to Hi-Z. State of the outputs are controlled through registers LS0 to LS3 (LS0 and LS1 in LP3944). Because four different output states are available, two control bits per output are required. After startup, all outputs are set to Hi-Z by default.

8 Read Mode (Input Mode)

All ports that are used as inputs should be set to Hi-Z mode. The status of the inputs are read through the input registers. Outputs LED0 to LED7 are read through register 0x00 (Input 1) and outputs LED8 to LED17 through register 0x01 (Input 2). Note that pins that are configured to outputs are read also. To read the status of the outputs, the master (microcontroller) first addresses the slave device (LP3943/44). Since LP3934/44 only supports write during chip addressing, the eight bit is set to "0" (write). LP3943 acknowledges this and the master sends the address of the register to be read. After LP3943/44 acknowledges this, the master creates a repeated start followed by a device address with eight bit set to "1" (read). LP3943 acknowledges this and sends the data of the register to the SDA line. After this, the transmission is either ended with STOP condition or addressing of the next register is started. For more detailed description on register read, see the device-specific data sheets.

If the data on the input pins changes faster than the master can read it, that data will be lost.

9 Write Mode (Output Mode)

To write to an output, the master (microcontroller) first addresses the slave device (LP3943/44). By setting the eight bit to "0", the write mode is entered. The slave acknowledges this and the master sends the address of the register to be written. After the slave has acknowledged this, the master sends the data. After this, the transmission is ended with STOP condition or addressing of the next register is started. Each selector register controls the state of four outputs. All four outputs need to be written at the same time. If only one output needs to be changed, the master must know the states of the other three outputs in the same selector register. This can be done by first reading the status of the selector register and then writing the same values to those register bits. Also if input and outputs are on the same selector register care must be taken not to write inputs to output LOW. Writing input low can cause large amounts of current flow through the input if logic high is applied to it.

10 Auto Increment

When multiple registers are written or read at the same time, a lot of addressing is required on the I2C bus. LP3943/44 supports the Auto Increment function to minimize this traffic. Auto increment automatically increments the register address after write or read. This is continued until the write or read sequence is ended with STOP condition. This allows to read or write all registers with only one addressing. For more information about Auto Increment, see the device-specific data sheets.

11 Pull-up Resistors

The values of the pull-up resistors depends on the required strength of the logic high state. Note that in logic low state, the open drain output pins of the LP3943/44 can sink up to 25 mA currents but the source current depends on the pull-up resistors. Smaller pull-up resistor values result to higher source currents but the current consumption is also increased during output low.

12 Tips and Tricks

Since four outputs are always written at the same time, it is wise to group the inputs and outputs regarding these registers. For example, if 4 inputs and 12 outputs are required, LED0 to LED3 could be used as inputs and LED4 to LED15 as outputs. This way, register 0x06 (LS0) would not need any write operations and during output changes there would not be danger of writing to the inputs. Also, the outputs that perform a certain function could be grouped to the same selector registers. If all I/Os need to be set to the Hi-Z state, applying a logic low to the RST pin for at least 10 ns will set the device to its default state (all outputs in Hi-Z).

Note that all outputs do not have to be set as digital inputs and outputs. Some of the outputs can drive LEDs or other peripherals, and the rest of them can be set as GPIOs. Figure 3 shows an example of LP3944 in this kind of mixed mode configuration. Outputs LED0 to LED2 are connected in parallel to drive a vibration motor with a current up to 75 mA. The outputs are controlled with the PWM generator 0 with PWM frequency set to the minimum (0.625 Hz). LED3 is driving a speaker to generate audible effect. PWM generator 1 is set to control LED3 with 160 Hz maximum frequency. LED4 and LED5 are set as inputs and are connected to input switches with proper pull-up resistors. LED6 and LED7 are used to drive indicator LEDs. Indicator LEDs can be controlled either on and off or they can be synchronized to vibration motor to generate combined vibrating and visual alarm. In this example, indicator LEDs and input switches are in the same control register (LS1). Switch inputs must be kept in output Hi-Z when writing indicator LEDs on and off. Table 2 shows how to set the registers for this example.

This is just a single example to show how LP3943/44 can be used in a variety of applications. If 16 inputs and outputs are not enough, up to 8 LP3943s can be connected to single SMBUS/I^2C bus to bring up to 128 input and output channels available.

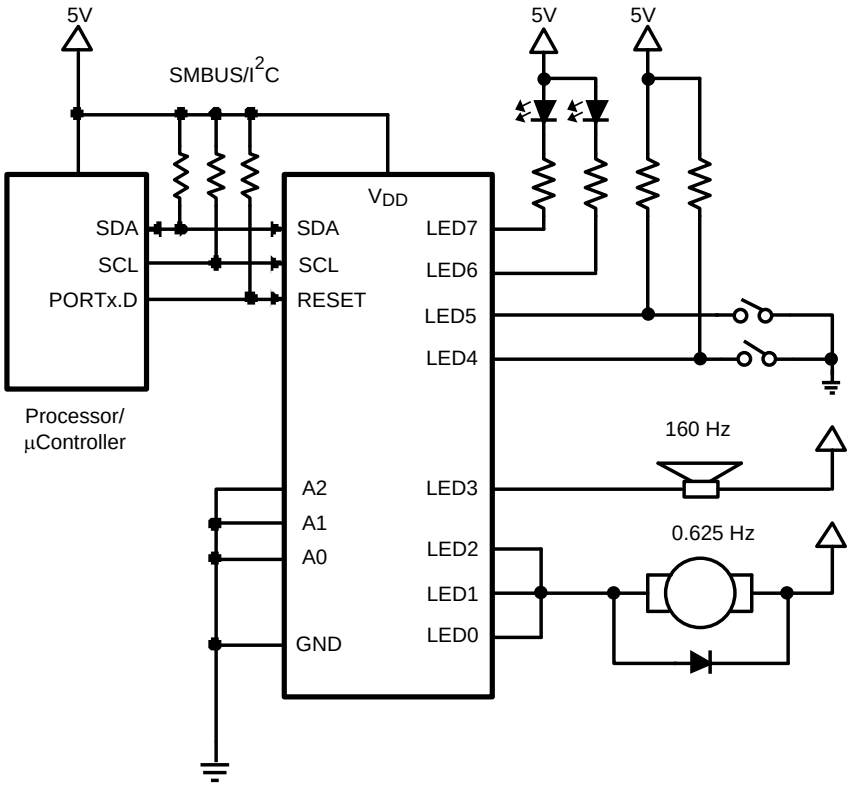

Figure 3. LP3944 in Mixed Mode Configuration

Table 2. Example Register Settings

Address (HEX)	Register Name	Register Value (BIN)	Description
0x00	Input 1	xxxxxxxx	Input read register
0x01	Register1	xxxxxxxx	None
0x02	PSC0	11111111	PWM frequency for the vibration motor, set to 0.625 Hz (PWM0)
0x03	PWM0	10000000	Duty cycle for the vibration motor, set to 50%
0x04	PCS1	00000000	PWM frequency for the speaker, set to 160 Hz (PWM1)
0x05	PWM1	10000000	Duty Cycle for the speaker, set to 50%
0x06	LS0	11101010	LED3 set to PWM1, LED0 to LED2 set to PWM0
0x07	LS1	01010000	LED4 and LED5 set to Hi-Z (input), LED6 and LED7 set to output LOW (LEDs are on)
0x08	Register 8	xxxxxxxx	None
0x09	Register 9	xxxxxxxx	None

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