Application Report
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LDOs Thermal Performance in Small SMD Packages

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ABSTRACT

This application report covers common questions regarding linear regulators and thermal metrics. This document also compares continuous-load-condition and pulsed-load-condition thermal performance of low dropout linear regulators (LDOs).

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1 Purpose

This application note covers common thermal questions related to LDOs in small surface mount device (SMD) packages, provides an overview on thermal resistance and characterization parameters, and explores LDO thermal performance under continuous load conditions and pulsed load conditions. In addition, *Appendix B* provides a list of valuable thermal resources and tools provided by Texas Instruments.

2 Fundamentals

Package thermal limitation is a key parameter for linear regulators, especially when the application requires large difference between input power and output power. Nearly all of the dissipated power by the linear regulators converts into heat and in turn increases the junction temperature. High junction temperature can affect the lifetime reliability and accelerate common failures.

Thermal performance varies from package to package dependent on lead frame, bond wire, mold compound, die-attach adhesive, die-size ratio to package, number of pins, thermal pad. Some common characteristics of SMD packages are:

- For small-outline no leads (SON) packages, the primary conduction path for heat is through the exposed power pad to the printed circuit board (PCB). To ensure the device does not overheat, connect the exposed pad, through thermal vias, to an internal ground plane with an appropriate amount of copper PCB area.
- On the ball grid array (BGA) package, the primary conduction path for heat is through the bumps to the PCB.

A well-designed application board enhances the package capability to dissipate heat. Properly sizing of the thermal plane, the thermal connection to the exposed pad, and strategic component placement improves the thermal performance of the package.

Power dissipation (P_D) within the device depends on the power that transform into heat. P_D depends on input voltage, output voltage, and load conditions. To calculate power dissipation use Equation 1.

$$P_{D(MAX)} = (V_{IN(MAX)} – V_{OUT}) \times I_{OUT(MAX}) \quad (1)$$

To minimized thermal dissipation while achieve higher efficiency, use the lowest available voltage drop option or voltage difference between input and output that would still be greater than the minimum dropout voltage (V_{DO}). However, keep in mind that higher voltage drop or input-output voltage difference results in a better power supply rejection ratio (PSRR) and transient performance.

2.1 Thermal Metrics

Thermal Information relevant to each package is available in the *Specifications* section of Texas Instruments data sheets. Figure 1 show a typical thermal table.

Package drawing nomenclature

Package type

THERMAL METRIC[1]		LP5907			UNIT
		DBV (SOT-23)	DQN (X2SON)	YKE (DSBGA)	
		5 PINS	4 PINS	4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193.4	216.1	206.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	102.1	161.7	1.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	45.8	162.1	37.0	
ψ_{JT}	Junction-to-top characterization parameter	8.4	5.1	15.0	
ψ_{JB}	Junction-to-board characterization parameter	45.3	161.7	36.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	123.0	n/a	

Thermal Resistance

Thermal Characterization

Figure 1. LP5907 Thermal Metrics Table

The thermal metrics are widely adopted in the semiconductor industry. The Joint Electron Device Engineering Council (JEDEC) and the Electronic Industries Alliance (EIA) regulate these standardized thermal metrics.

The following boards are the main types of JESD 51-X boards used to characterized SMD:

- JESD51-7: A highly effective thermal conductivity test board for leaded SMD packages:
  - Trace layers and layer thickness (High K 2s2p)
  - Component trace, 2 oz. (0.035 mm)
  - Plane 1, 1 oz. solid (0.070 mm)
  - Plane 2, 1 oz. solid (0.070 mm)
  - Backside trace, 2 oz. (0.035 mm)
- JESD51-5: This board is an extension of thermal test board standards for packages with direct thermal attachment mechanisms:
  - The stackup is the same as the JESD51-7 but with thermal vias with a diameter of 0.3 mm placed in a grid array of 1-mm × 1-mm trace squares separated by 0.2-mm spaces. Directly under the exposed thermal pad.

2.2 Thermal Metric Differences

Figure 1 shows two thermal metrics: thermal resistance and thermal characterization parameter. The thermal resistance represents the heat flowing along a particular path between the junction and the other location (for example, case, board, ambient, and so forth) as shown in Figure 2. In the contrary, the thermal characterization parameter does not provide the thermal resistance on a specific path, but provides the total system heat independent of the thermal path. The thermal characterization has two main measurement terms, the junction-to-case center top and junction-to-board. Figure 3 shows the total heat reading independent of the thermal path.

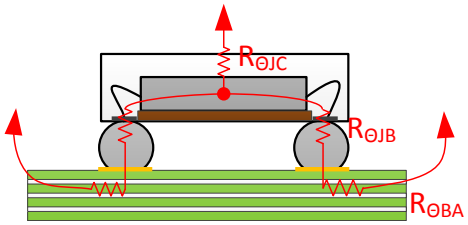


Figure 2. DSBGA Cross-Sectional View

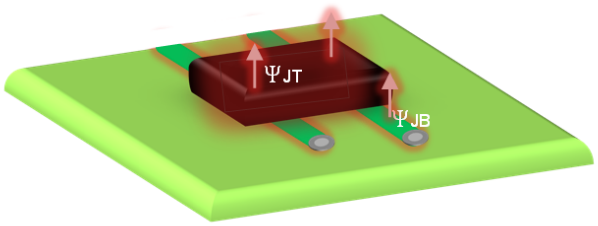


Figure 3. DSBGA Top View

2.2.1 Thermal Resistance

The Greek symbol Theta (θ) represents the thermal resistance. Theta is followed by a subscript that represents the thermal resistance path, For example, $R_{\theta JB}$ stands for the thermal resistance between the junction and the application board.

List of theta subscripts and meaning:

- $R_{\theta JA} = (T_J – T_A)/ P_D$: Total thermal resistance from junction to ambient. T_J = junction temperature; T_A = ambient temperature.
- $R_{\theta JC}$: thermal resistance from junction to case
- $R_{\theta JB}$: thermal resistance from junction to board
- $R_{\theta CA}$: thermal resistance from case to ambient
- $R_{\theta BA}$: thermal resistance from board to ambient (dependent on the PCB characteristics and layout)

The $R_{\theta JA}$ is a conservative measure of the package ability to dissipate heat to the ambient environment. The sole purpose of $R_{\theta JA}$ is to serve as a baseline to compare the thermal performance of a package to another package in a standardized test environment. Figure 4 shows an example of thermal resistance comparison between two packages the YKA-DSBGA package and DRV-WSON package. YKA-DSBGA has lower $R_{\theta JB}$ and $R_{\theta JC\ (top)}$ than the DRV-WSON, but the DRV-WSON package has a lower total thermal resistance from junction to ambient than the YKA-DSBGA package due to the exposed thermal pad which brings down the overall thermal resistance from junction to ambient ($R_{\theta JA}$).

THERMAL METRIC(1)		LP5910		UNIT
		YKA (DSBGA)	DRV (WSON)	
		4 PINS	6 PINS	
$R_{\theta JA}$ (2)	Junction-to-ambient thermal resistance, High-K	202.8	79.2 (3)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	3.3	110.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	36.0	48.7	
Ψ_{JT}	Junction-to-top characterization parameter	0.4	5.2	
Ψ_{JB}	Junction-to-board characterization parameter	36.0	49.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	18.1	

Figure 4. Thermal Resistance Comparison Between Packages

$R_{\theta JA}$ provides a great package-to-package comparison value but, unfortunately, Theta does not approximate or predict the thermal performance of a particular package in a specific application because Theta is dependent on the PCB characteristics and board layout.

2.2.2 Thermal Characterization

The Greek symbol Psi (Ψ) shown in Figure 4 represents the thermal characterization parameter. The thermal characterization values are not thermal resistance values, but rather package-specific thermal characteristics that offer practical and relative means of estimating junction temperatures on a particular application board. The junction is approximated by measuring the case temperature or board temperature (measured 1 mm from the device pin) and then using Equation 2 or Equation 3.

List of Ψ subscripts and meanings:

- Ψ_{JT}: Junction-to-top characteristic parameter
- Ψ_{JB}: Junction-to-board characteristic parameter

Equation 2 approximates junction temperature using the measured case top temperature:

$$T_{J(MAX)} = T_{TOP} + (\Psi_{JT} \times P_{D(MAX)}) \quad (2)$$

where

- T_{TOP} = is the case temperature measured on top of the device package

Equation 3 approximates junction temperature using the measured board temperature (temperature adjacent to a device pin):

$$T_{J(MAX)} = T_{BOARD} + (\Psi_{JB} \times P_{D(MAX)}) \quad (3)$$

where

- T_{BOARD} = is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For more information about the thermal characteristics ΨJT and ΨJB, see the TI Application Report *Semiconductor and IC Package Thermal Metrics* (SPRA953), available for download at www.ti.com.

For more information about measuring T_{TOP} and T_{BOARD}, see the TI Application Report *Using New Thermal Metrics* (SBVA025), available for download at www.ti.com.

For more information about the EIA/JEDEC JESD51 PCB used for validating $R_{\theta JA}$, see the TI Application Report *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs*, also at (SZZA017), www.ti.com.

3 Thermal Performance of SMD Packages

This section evaluates and compares the thermal performance of LP5907 and LP5910 LDOs under continuous load conditions and pulsed load conditions. All the measurements in the following subsections were taken under typical lab conditions at room temperature 23°C and without controlled airflow.

3.1 Test Boards, Devices, and Equipment

3.1.1 Boards

3.1.1.1 θJA_LP5907_BGA

θJA_LP5907_BGA does not represent a board but the theoretical junction temperature of LP5907UVE calculated using the simulated JESD51-7 $R_{\theta JA}$ (206.1°C/W) and Equation 4 to calculate the junction temperature:

$$T_{J(MAX)} = T_{A(MAX)} + (R_{\theta JA} \times P_{D(MAX)}) \quad (4)$$

3.1.1.2 JESD_M

JESD_M has the same layers and traces requirements as a JESD_51-7 standard board, but with minor deviations from the standard. JESD_M has two 0402 capacitors close to the IN and OUT pins of the LDO in order to accommodate compensation capacitors to assure stability and functionality of the LP5907UVX-2.5/NOPB .

3.1.1.3 LP5907_BGA

The LP5907_BGA board is the LP5907UV-1.8EVM Evaluation board populated with LP5907UVX-2.5/NOPB

3.1.1.4 JESD_H

The JESD_H board has the same dimensions as the JEDEC_M board, but thermally optimized by adding a copper fill surrounding the LP5907UVX-2.5/NOPB, adding various thermal vias to lower the thermal resistance and two more intermediate layers.

3.1.1.5 LP5907_SOT23

The LP5907_ SOT23 board is an SOT23 EVM populated with LP5907MFX-2.5/NOPB.

3.1.1.6 LP5907_X2SON

The LP5907_ X2SON board is an X2SON EVM populated with LP5907SNX-2.5/NOPB.

3.1.1.7 LP5910_WSON

The LP5910_ WSON is the LP5910DRV18EVM evaluation module populated with LP5910-1.8DRVR.

3.1.1.8 LP5910_BGA

The LP5910_ WSON is the LP5910YKA18EVM evaluation module populated with LP5910-1.8YKAR.

NOTE: Refer to *Appendix A* for additional evaluation board details as board layers, PCB layout and component placement.

3.1.2 Devices and Packages

3.1.2.1 LP5907 Ultra-Low-Noise, 250-mA Linear Regulator for RF and Analog Circuits

The LP5907 is a linear regulator capable of supplying 250-mA output current. Designed to meet the requirements of RF and analog circuits, the LP5907 device provides low noise, high PSRR, low quiescent current and low line or load transient response figures. Using new innovative design techniques, the LP5907 offers class-leading noise performance without a noise bypass capacitor and the ability for remote output capacitor placement.

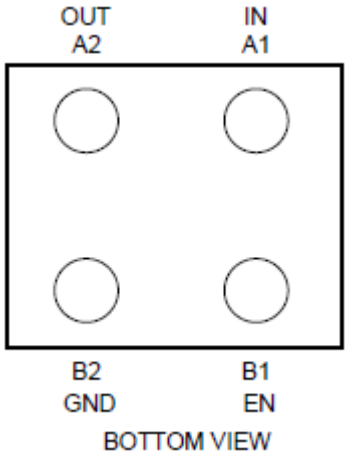


Figure 5. LP5907 DSBGA Package ($R_{\theta JA}$ = 206.1°C/W)

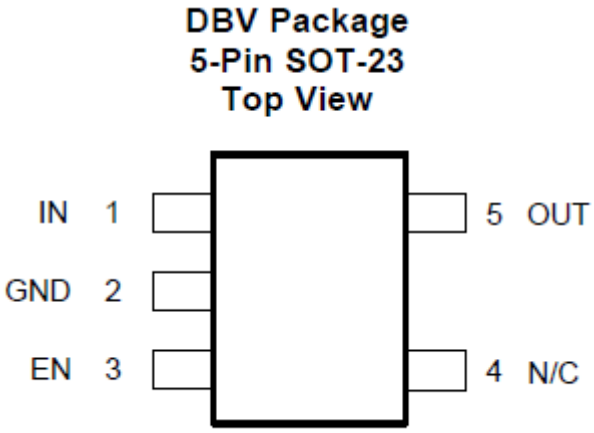


Figure 6. LP5907 SOT Package ($R_{\theta JA}$ = 193.4°C/W)

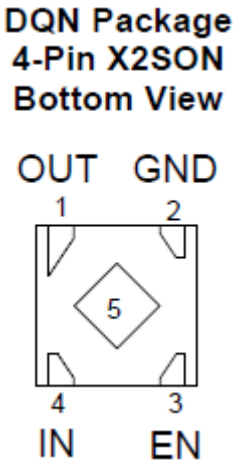


Figure 7. LP5907 X2SON Package ($R_{\theta JA}$ = 216.1°C/W)

3.1.2.2 LP5910 Ultra-Low-Noise, 300-mA Linear Regulator for RF and Analog Circuits

The LP5910 is a linear regulator capable of supplying up to 300 mA of output current. Designed to meet the requirements of RF and analog circuits, this device provides low noise, high PSRR, low quiescent current and superior line transient and load transient response. Using new innovative design techniques the LP5910 offers class-leading noise performance without a noise bypass capacitor and with the option for remote output capacitor placement.

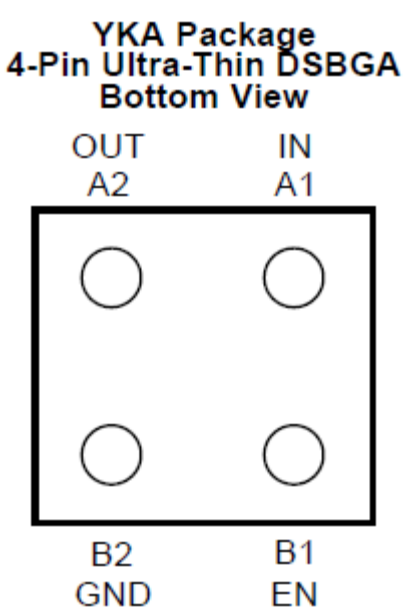


Figure 8. LP5910 DSBGA Package ($R_{\theta JA}$ = 202.8°C/W)

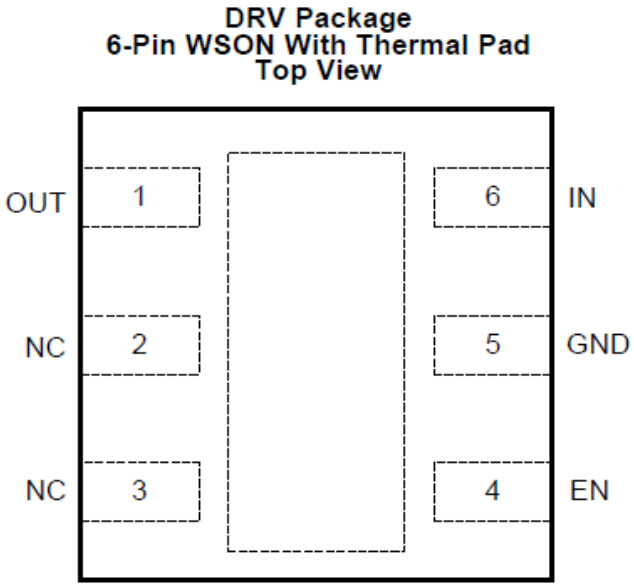


Figure 9. LP5910 WSON Package ($R_{\theta JA}$ = 79.2°C/W)

3.1.3 Equipment Used

Table 1 shows the test equipment used in the subsequent sections

Table 1. Test Equipment

TEST EQUIPMENT	PART NUMBER
DC voltage supply	Agilent E3631A
Multimeter	Agilent E34401A
Thermal camera	Optotherm InfraSight MI320

3.2 Continuous Load Conditions

This section tests the thermal performance of SMD LDOs under continuous load conditions. The output load is a resistive passive element.

Test procedure:

1. Calculate power dissipation (P_D) using Equation 1 and maintain the same P_D for all the boards under test.
2. Measure the device case (top) temperature when the device is thermally stable.
3. Approximate junction temperature using Equation 2.
4. Repeat procedure for increments of 25% power dissipation.

3.2.1 Thermal Comparison Between JESD51-7 Simulated and Real Board

The simulated JESD51-7 board is used to obtain conservative $R_{\theta JA}$ values; however, the board does not take into consideration the compensation components like external capacitors and resistors, nor does it compensate for ambient conditions such as air flow and ventilation.

In the following thermal comparison comparison, the simulated board as JESD51-7 is referenced; the constructed evaluation board is referred to as JESD_M. The JESD_M follows all the regulations from the standard JESD51-7 but it contains copper pads close to the input and output pins for the required capacitors and was tested at room temperature under regular laboratory conditions. For JESD_M layers stack and layout printout refer to *Appendix A* of this document.

The evaluation results are presented in Figure 10 and, as expected, the board tested in the lab (JESD_M) outperformed the simulated JESD51-7 board by 5% to 15% depending on the power dissipation.

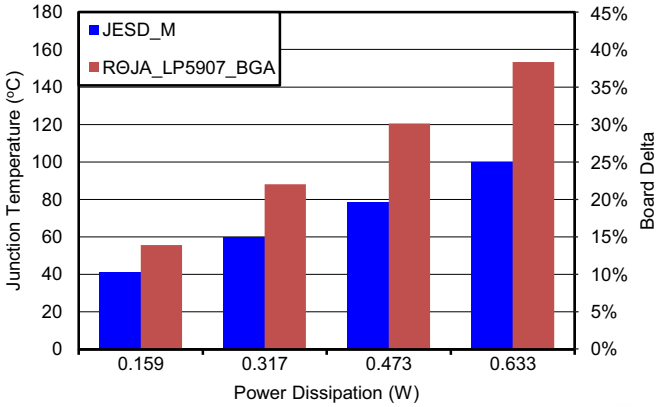


Figure 10. Comparison between JESD_M and JESD51-7

3.2.2 DSBGA Evaluation Boards Comparison

This exercise compares the junction temperature of the LP5907 in DSBGA packages mounted on various evaluation boards:

- θJA_LP5907_BGA: calculated junction temperature with standard JEDEC $R_{\theta JA}$ values
- JESD_M board: Modified JEDEC board
- JESD_H board: Highly optimized thermal board
- LP5907_BGA: Standard evaluation module

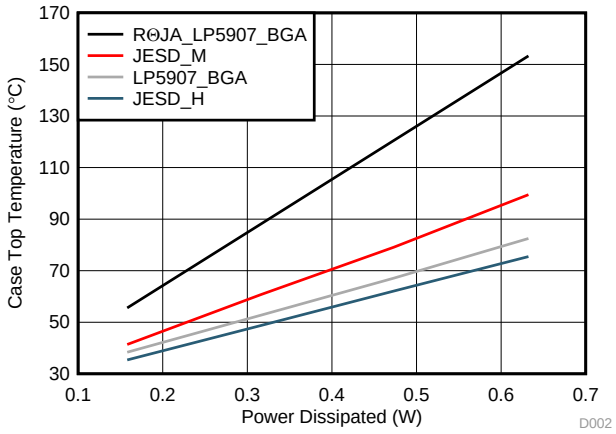


Figure 11. LP5907 DSBGA Board Comparison

Figure 11 compares the same device in the same package mounted on different boards. The thermal resistance drops with larger copper areas, for this reason the JESD_H board present the lowest junction temperature and the θJA_LP5907_BGA and JESD_M boards present the lowest thermal performance.

3.2.3 Comparison Between DSBGA Package and WSON Package

Figure 12 compares the junction temperature the LP5910 in the same voltage trim and similar board but in two different packages WSON package and DSBGA package, and confirms that the WSON package has better thermal performance than the DSBGA package.

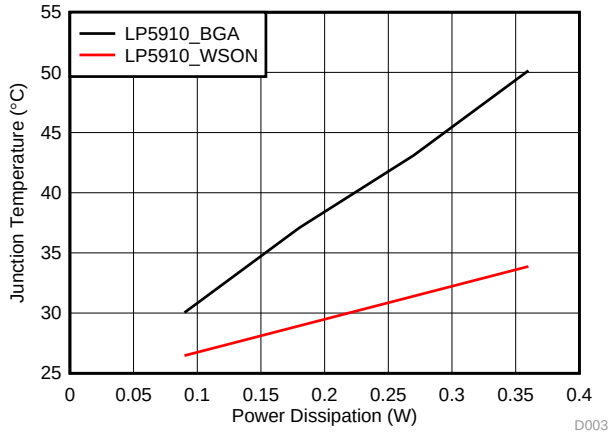


Figure 12. LP5910 Packages Comparison

3.3 Package Thermal Performance Comparison

Figure 13 and Table 2 show that the thermal resistance $R_{\theta JA}$ correlates with the junction temperature calculated with the measured case temperature. When the package thermal resistance is higher the junction temperature increases at a faster rate.

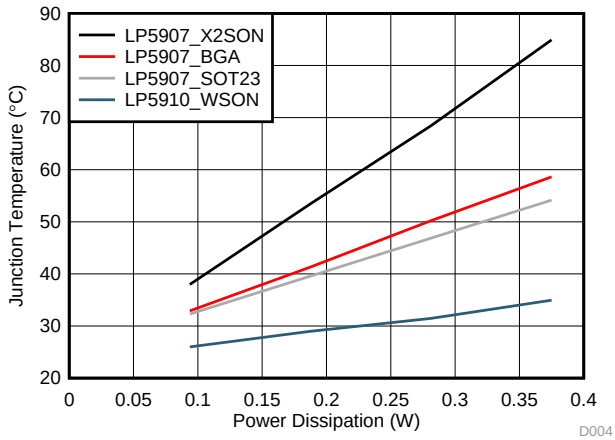


Figure 13. SOT, SON, and BGA Package Thermal Response Comparison

Table 2. Thermal Performance Comparison

DEVICE	PACKAGE TYPE	$R_{\theta JA}$ (°C/W)	MEASURED TEMPERATURE at P_D = 375 mW (°C)
LP5907	DQN (X2SON)	216.1	83
	YKE (DSBGA)	206.1	53
	DBV (SOT-23)	193.4	51
L5910	DRV (WSON)	79.2	33

3.4 Case Temperature Under Pulsed-Load Conditions

This section explores the thermal behavior of a linear regulator under pulse load conditions.

Test procedure:

- A passive resistive load was applied to LP5907_BGA output.
- Power dissipation during the ON time was 625 mW; the magnitude of the load remained the same for all the iterations.
- The device was evaluated under four load duty cycles conditions: 4s, 400 ms, 40 ms and 4 ms tuned to achieve various ON time scenarios as shown in Figure 14 , Figure 15, Figure 16, and Figure 17.
- The device case temperature was continuously measured as shown in Figure 14 , Figure 15, Figure 16, and Figure 17.

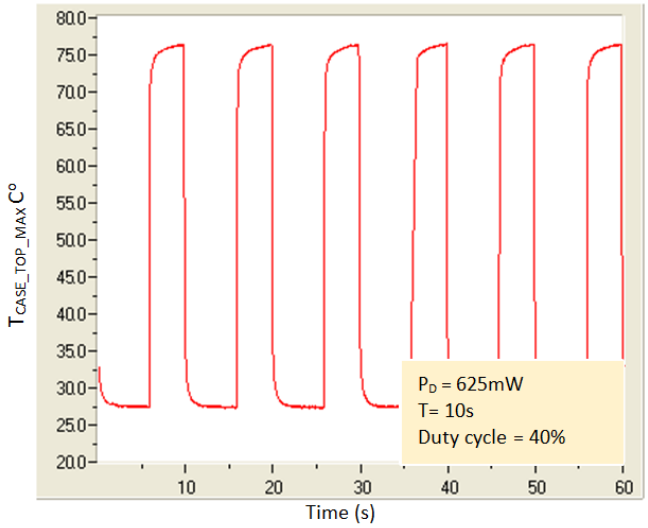


Figure 14. Load Pulse Duration 4s

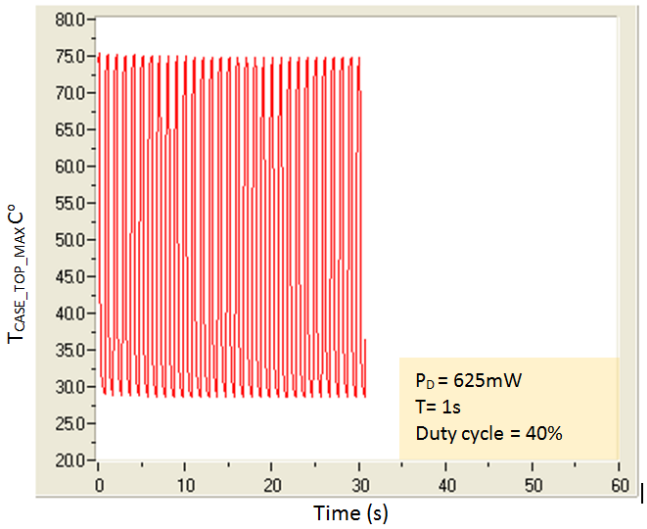


Figure 15. Load Pulse Duration 400 ms

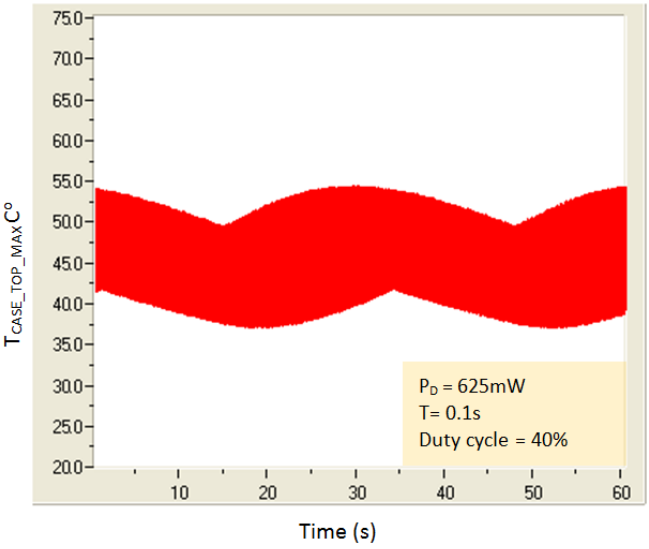


Figure 16. Load Pulse Duration 40 ms

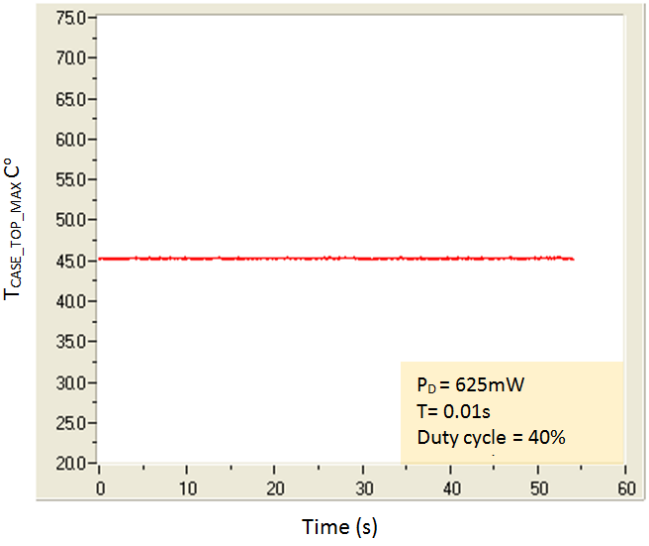


Figure 17. Load Pulse Duration 4 ms

As expected, a low-frequency load pulse presents a lower maximum case temperature — this statement is true for up to tens of milliseconds as shown in Figure 18; at higher frequencies the case temperature starts to rise at a faster rate. These results vary depending on the thermal mass and thermal resistance of the package and board layout.

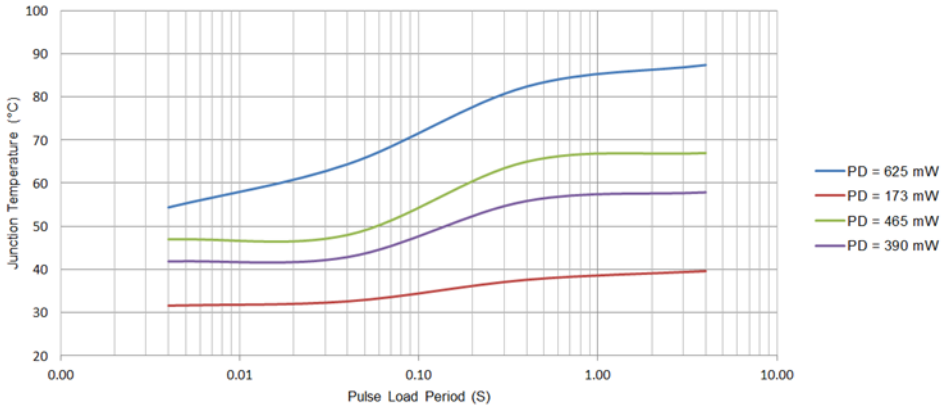


Figure 18. Transient Thermal Response Graph for LP5907 DSBGA

4 Frequently Asked Questions

The power tree requires a high PSRR and low noise LDO, but the LDO cannot support the load conditions?

Use a switcher regulator followed by an LDO or use two LDOs in current sharing configurations as shown in the following links:

TI Application Report: *Ballast Resistors Allow Load Sharing Between Two Paralleled DC/DC Converters* (SLVA250)

Video: Can't Take the Heat? Share the Current

Does the thermal PAD connected to GND make a substantial thermal difference?

TI highly recommends connecting the expose thermal PAD or TAB to a copper area and to maximize the thermal response vias must connect the PAD to inner solid ground planes. The total thermal improvement from the tab depends on the package, power dissipation, thermal pad dimension, the thickness of the top layer copper, isolating material between layers, number and dimension of vias, number of components surrounding the device due to thermal coupling effect, and airflow.

As an example, the following two cases were evaluated using X2SON package; the test conditions were the same in the two cases.

- Case A: The thermal pad connected to a solid ground area
- Case B: Thermal pad floating, not connected

  Case A had 20% better thermal performance than the Case B. In a package with a bigger thermal PAD, the thermal improvements could be even greater.

What are the common layout practices to improve thermal response?

Good layout practices to improve PCB and system design are:

- Spread out hot device on PCB
- Maximize GND layer in PCB
- No breaks in heat flow through planes
- Increase PCB layers or thickness
- Widen PCB traces near devices
- PCB vias under or near device
- System air vents near to device system air vents near device
- Global and local airflow
- Heat sink (Individual, group and chassis)
- Gap filler material up to chassis
- Metal screws from PCB to chassis

However, device layout depends on package type; TI data sheets include layout recommendations in the *Layout* section. Figure 19 shows a layout example taken from the LP5900 datasheet.

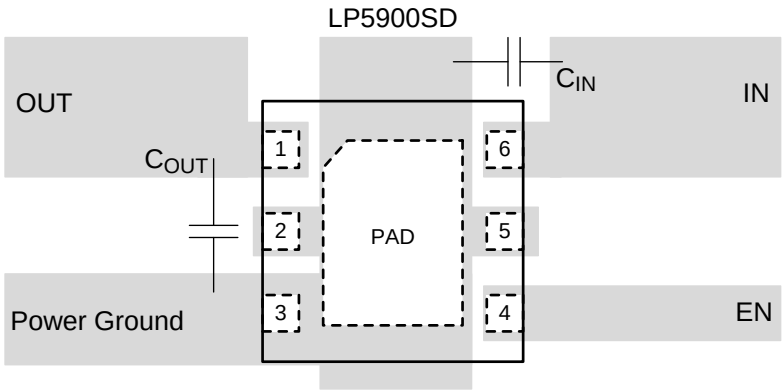


Figure 19. LP5900 WSON Layout

On the other hand, for recommended pad dimensions, refer to the *Mechanical, Packaging, and Orderable Information* section at the end of the data sheet. Figure 20 shows the recommended land pattern for LP5900.

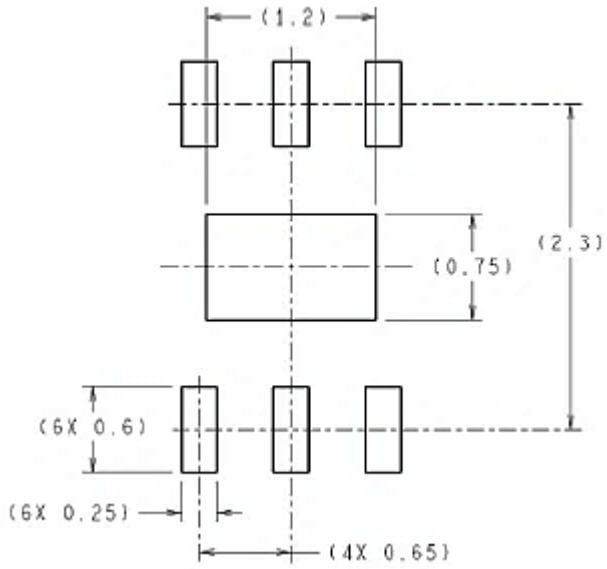


Figure 20. LP5900 Recommended Land Pattern

Is it possible to approximate the thermal resistance in the application board without a thermal camera or thermocouple sensor?

Yes, the thermal resistance from junction to ambient in a particular application board can be approximated by slowly increasing the power dissipation until the device enters into thermal shutdown then plugging the values in Equation 5. T_J can be obtained from the *Recommended Operating Conditions* table in the data sheet.

$$R_{\theta JA} = T_J – T_A / P_D \quad (5)$$

See the video at the following link for an example and detailed explanation of this procedure:

1.5 Engineer IT: Measuring Thermals - How Hot is Your LDO?

5 TI Tools and Support

5.1 Thermal Analysis

This Thermal Analysis page provides easy access to the tools and information needed to understand and design thermal systems including design tools, lab analysis recommendations, education, and FAQs. Select this thermal analysis link to see more information.

5.2 Thermal Calculator

Texas Instruments is creating a collection of useful engineering calculators and tools to facilitate design implementation.

- TI Gadgets/Widgets
- PCB Thermal Calculator
- TI Application Report *Using Thermal Calculation Tools for Analog Components* (SLUA566)

5.3 WebTHERM™ Online Thermal Simulation

The WEBENCH® WebTHERM online tool simulates the thermal behavior of a WEBENCH custom power design. All of the components within a design are integrated on a validated reference printed circuit board (PCB) design. The user defines the environment, and the problem is solved using the fast and accurate simulator of the tool.

WebTHERM is constantly adding new features and supporting additional devices.

5.4 Technical Library

Multiple technical document types may be selected, enabling users to download data sheets, errata, application notes, user guides, selection guides, solution guides, simulation models, white papers, design files, and more.

- Thermal application notes
- SMT and packaging application notes

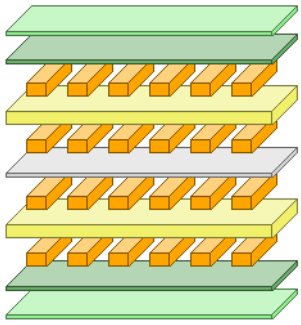
5.5 Video

Training videos are used to better understand LDOs and include more information on designing the best ADC power supply, stabilizing an LDO, measuring LDO noise and PSRR, sourcing 5 A or more with current sharing regulators, measuring thermal resistance between junction temperature and ambient, and measuring the ADC power supply rejection.

Engineer IT LDO Training Videos

Evaluation Board Layers Stack and Layout Printout

A.1 JESD_M



Layer Name	Type	Material	Thickness (mm)	Dielectric Material	Dielectric Constant	Pullback (mm)	Orientation
Top Overlay	Overlay						
Top Solder	Solder Mask/Co...	Surface Material	0.01016	Solder Resist	3.5		
Top Layer	Signal	Copper	0.07				Top
Dielectric1	Dielectric	Core	0.45	FR-4	4.8		
Signal Layer 1 (...	Signal	Copper	0.035				Not Allowed
Dielectric 3	Dielectric	Prepreg	0.45	FR-4	4.8		
Signal Layer 2 (V...	Signal	Copper	0.035				Not Allowed
Dielectric 2	Dielectric	Core	0.45	FR-4	4.8		
Bottom Layer (G...	Signal	Copper	0.07				Bottom
Bottom Solder	Solder Mask/Co...	Surface Material	0.01016	Solder Resist	3.5		
Bottom Overlay	Overlay						

Figure 21. JESD_M Layer Stackup

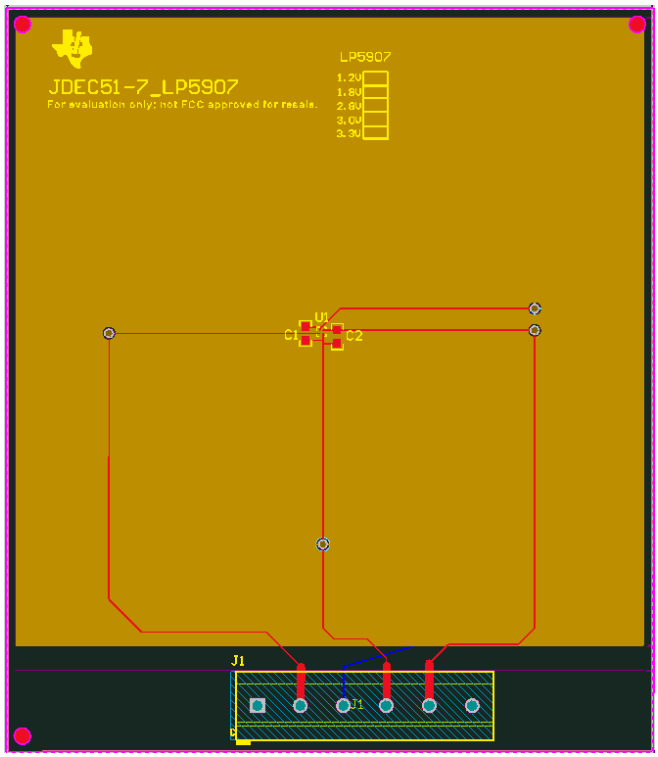


Figure 22. JESD_M Top

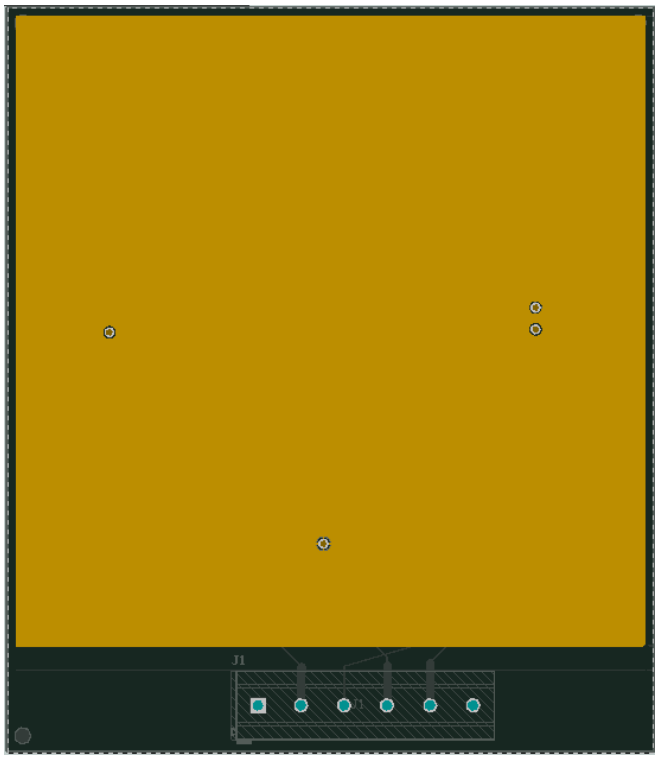


Figure 23. JESD_M Signal Layer 1

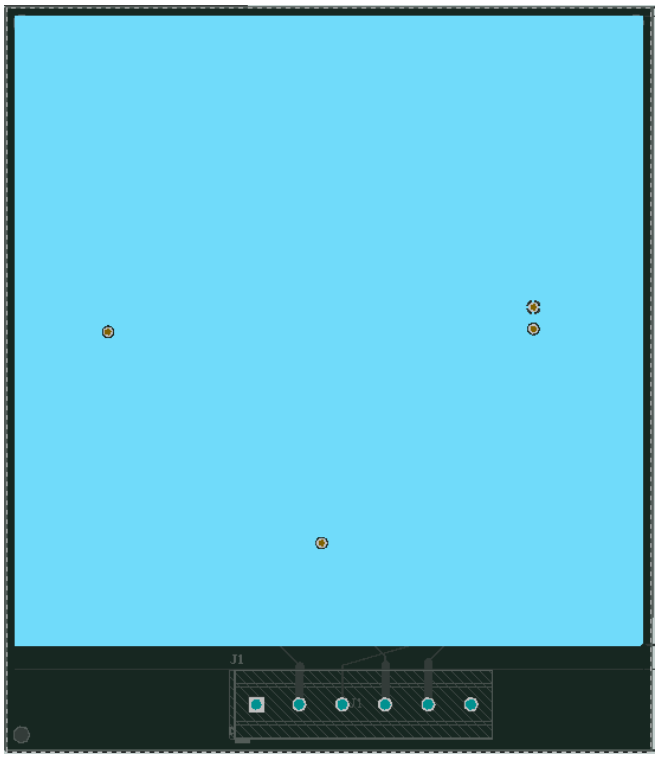


Figure 24. JESD_M Signal Layer 2

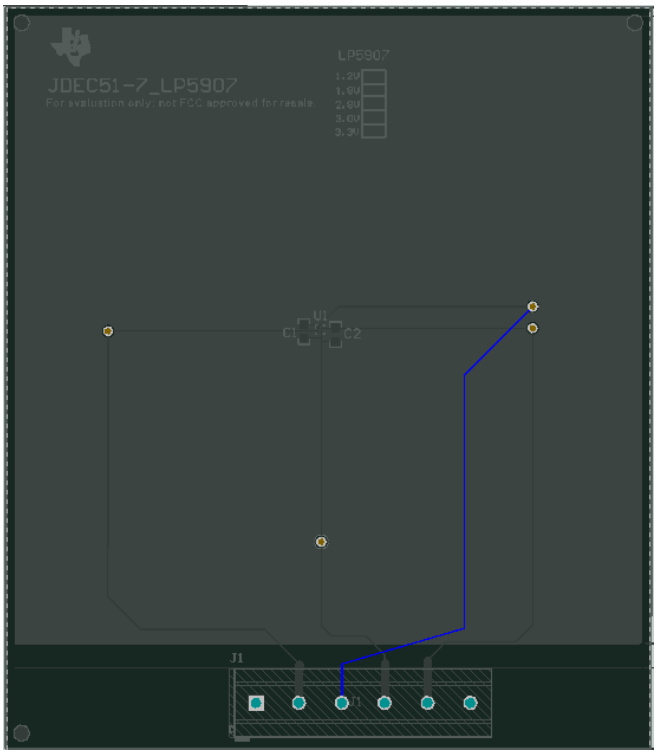
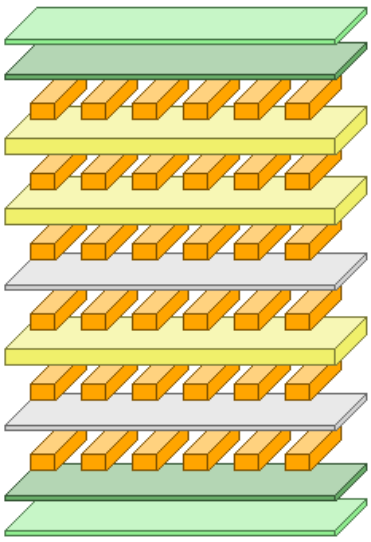


Figure 25. JESD_M Bottom

A.2 JESD_H



Layer Name	Type	Material	Thickness (mm)	Dielectric Material	Dielectric Constant
Top Overlay	Overlay				
Top Solder	Solder Mask/Co...	Surface Material	0.01016	Solder Resist	3.5
Top Layer	Signal	Copper	0.07		
Dielectric 1	Dielectric	Core	0.25	FR-4	4.8
Signal Layer 1 (...	Signal	Copper	0.036		
Dielectric 2	Dielectric	Core	0.127	FR-4	4.8
Signal Layer 2 (V...	Signal	Copper	0.035		
Dielectric 3	Dielectric	Prepreg	0.327	FR-4	4.8
Signal Layer 3 (...	Signal	Copper	0.035		
Dielectric 4	Dielectric	Core	0.254	FR-4	4.8
Signal Layer 4 (V...	Signal	Copper	0.036		
Dielectric 5	Dielectric	Prepreg	0.254	FR-4	4.8
Bottom Layer (G...	Signal	Copper	0.07		
Bottom Solder	Solder Mask/Co...	Surface Material	0.01016	Solder Resist	3.5
Bottom Overlay	Overlay				

Figure 26. JESD_H Layer Stackup

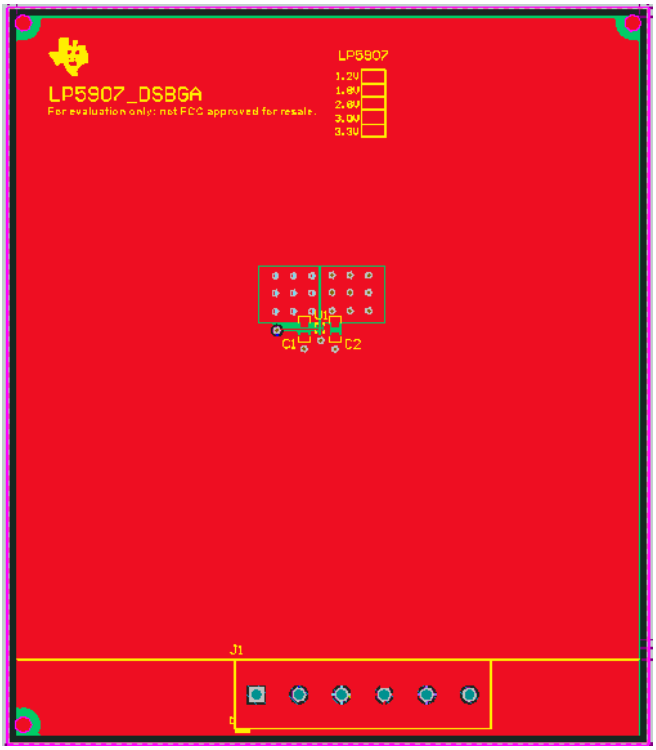


Figure 27. JESD_H: Top

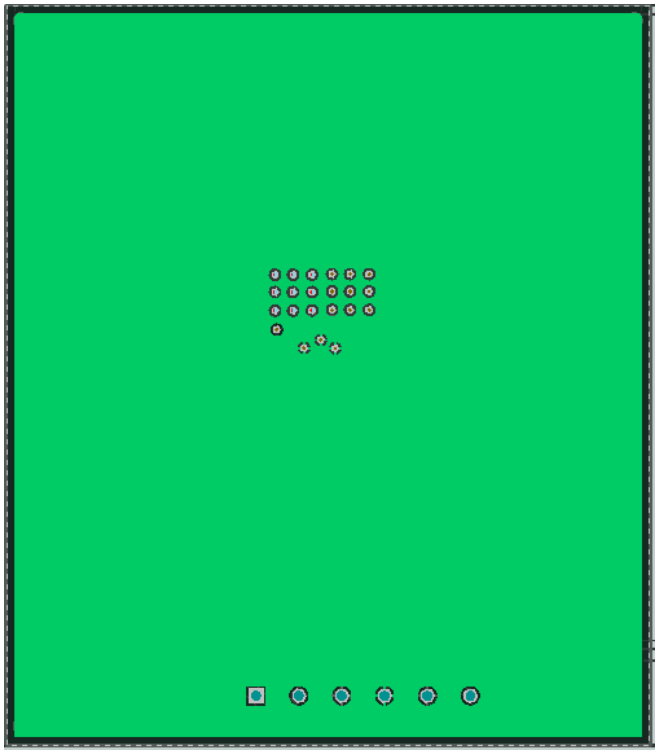


Figure 28. JESD_H: Signal Layer 1

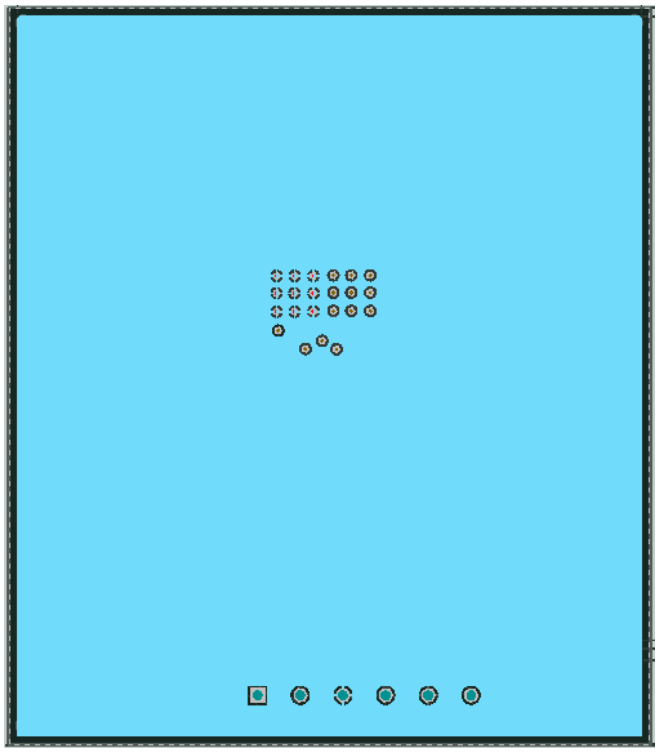


Figure 29. JESD_H: Signal Layer 2

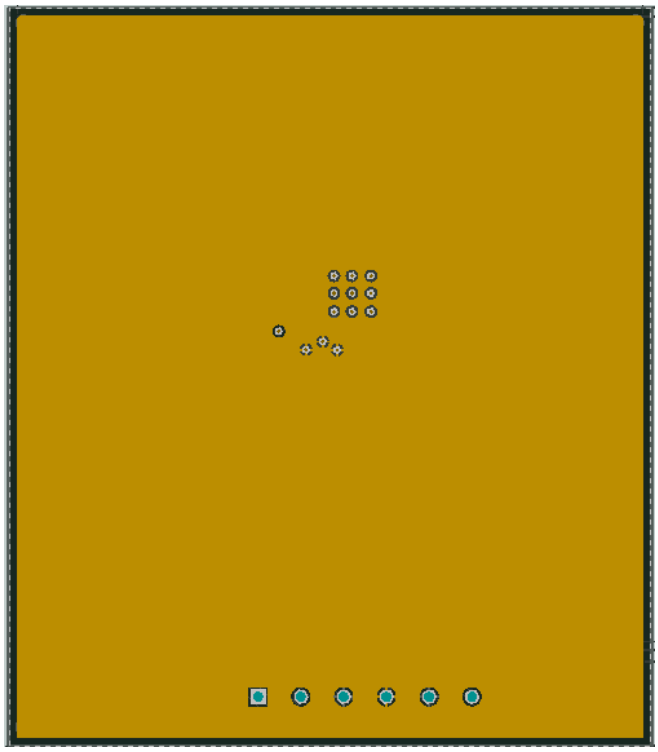


Figure 30. JESD_H: Signal Layer 3

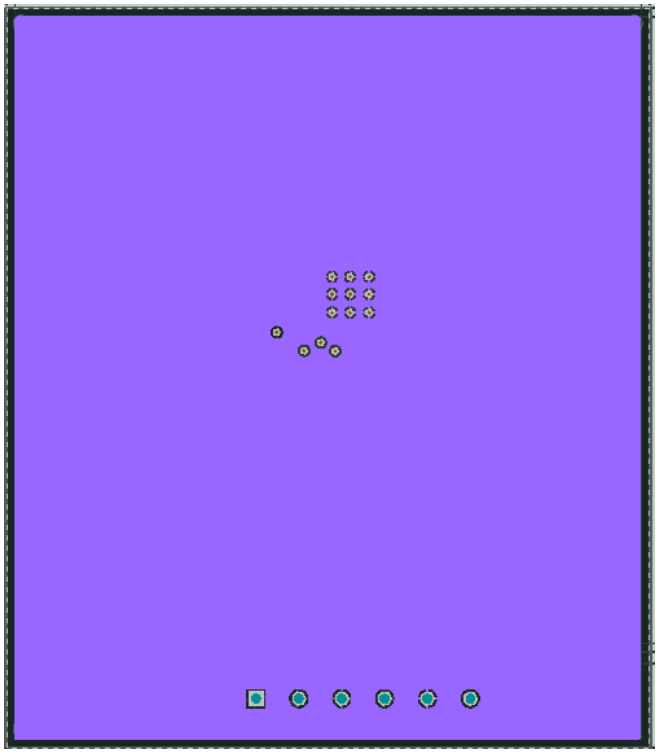


Figure 31. JESD_H: Signal Layer 4

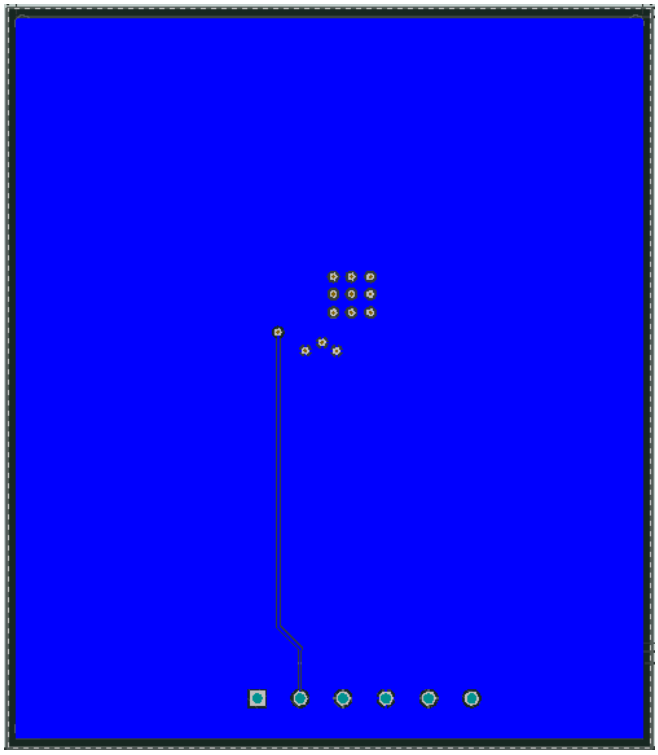
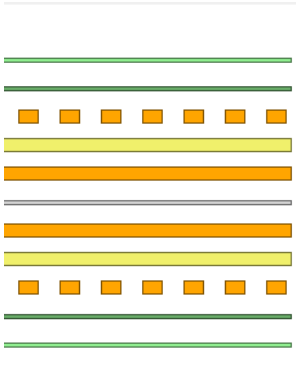


Figure 32. JESD_H: Bottom

A.3 LP5907_BGA



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant	Pullback (mil)	Orientation
Top Overlay	Overlay						
Top Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5		
Top Layer	Signal	Copper	2				Top
Dielectric1	Dielectric	Core	58	FR-4	4.8		
InternalPlane1	Internal Plane	Copper	1.4			20	
Dielectric2	Dielectric	Prepreg	12.6	FR-4	4.8		
InternalPlane2	Internal Plane	Copper	1.4			20	
Dielectric3	Dielectric	Core	12.6	FR-4	4.8		
Bottom Layer	Signal	Copper	2				Bottom
Bottom Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5		
Bottom Overlay	Overlay						

Figure 33. LP5907_BGA: Layer Stackup

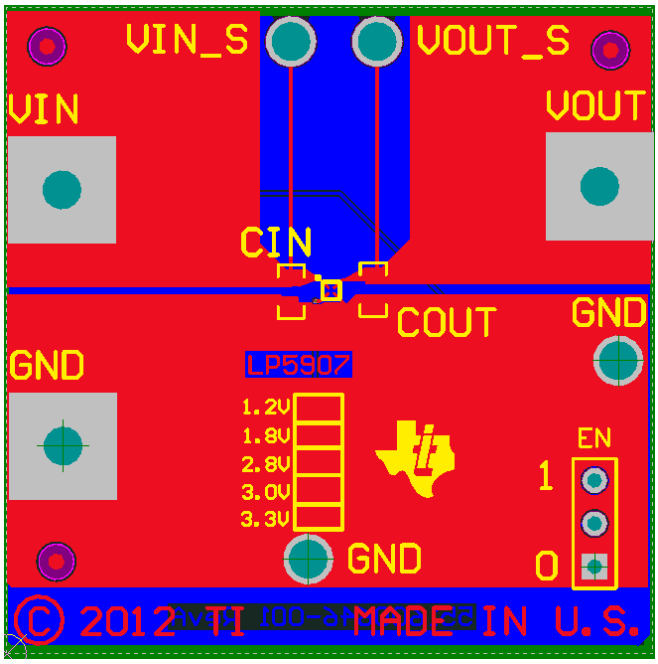


Figure 34. LP5907_BGA: Top Layer Silk Screen

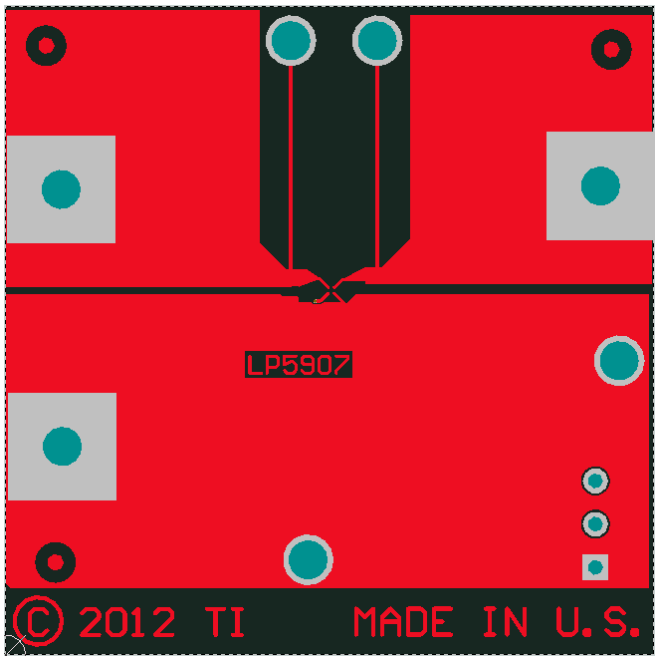


Figure 35. LP5907_BGA: Top Layer

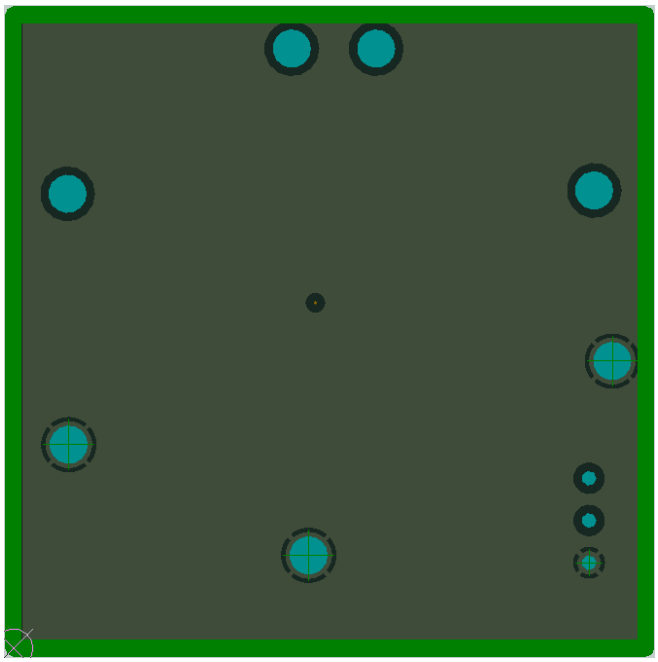


Figure 36. LP5907_BGA: Internal Plane 1

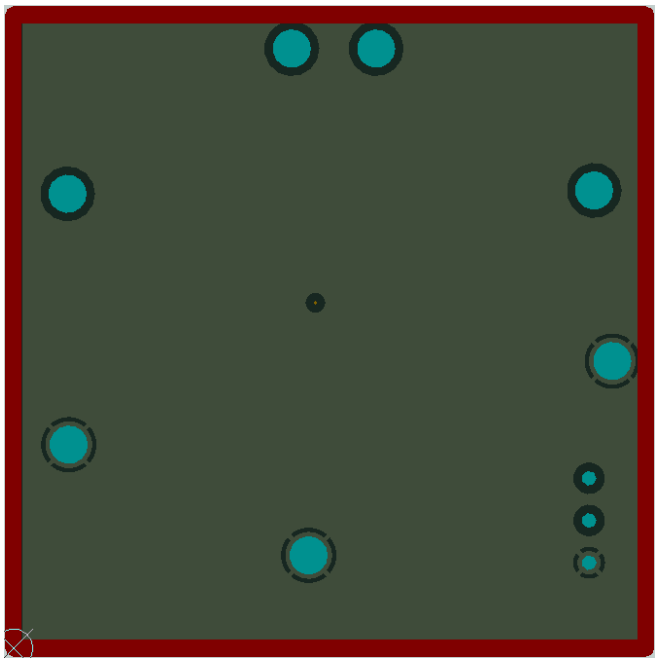


Figure 37. LP5907_BGA: Internal Plane 2

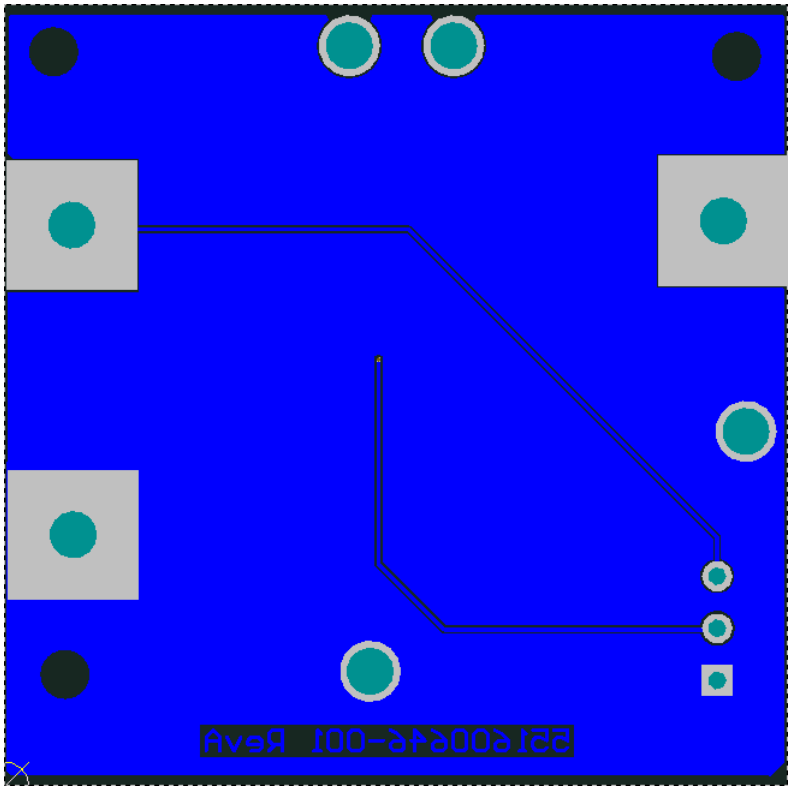
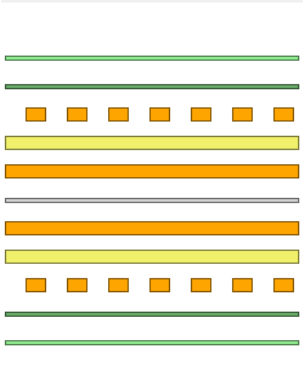


Figure 38. LP5907_BGA: Bottom Layer

A.4 LP5907_SOT23



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant	Pullback (mil)	Orientation
Top Overlay	Overlay						
Top Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5		
Top Layer	Signal	Copper	2				Top
Dielectric1	Dielectric	Core	58	FR-4	4.8		
InternalPlane1	Internal Plane	Copper	1.4			20	
Dielectric2	Dielectric	Prepreg	12.6	FR-4	4.8		
InternalPlane2	Internal Plane	Copper	1.4			20	
Dielectric3	Dielectric	Core	12.6	FR-4	4.8		
Bottom Layer	Signal	Copper	2				Bottom
Bottom Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5		
Bottom Overlay	Overlay						

Figure 39. LP5907_SOT23: Layer Stackup

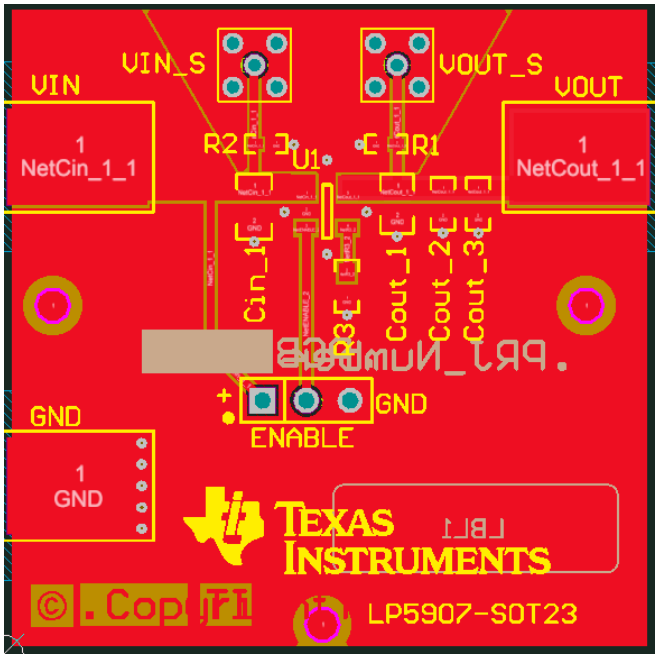


Figure 40. LP5907_SOT23: Top Layer Silk Screen

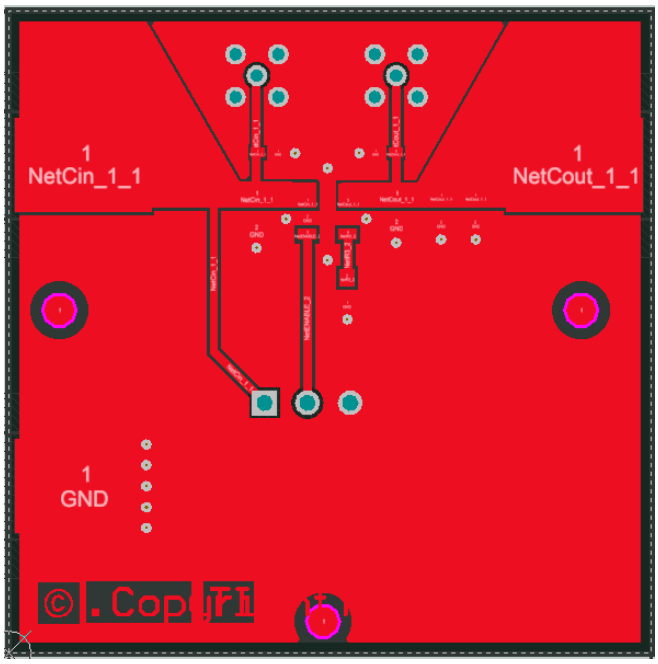


Figure 41. LP5907_SOT23: Top Layer

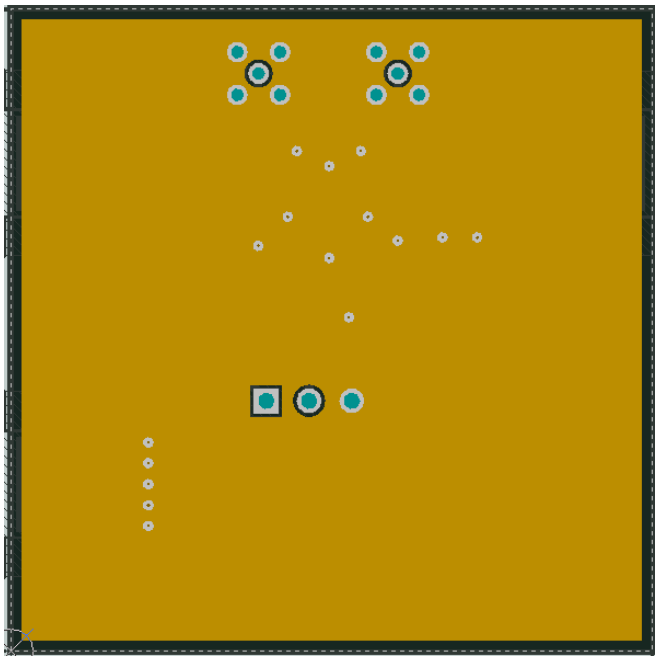


Figure 42. LP5907_SOT23: Internal Plane 1

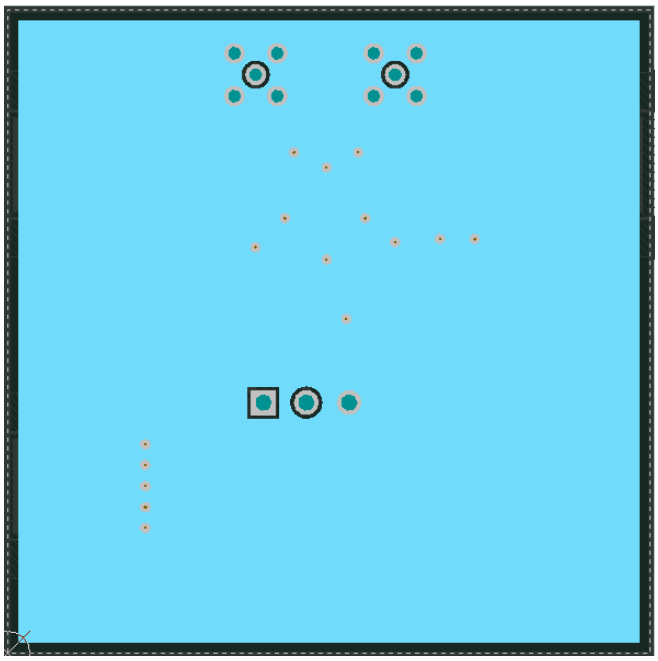


Figure 43. LP5907_SOT23: Internal Plane 2

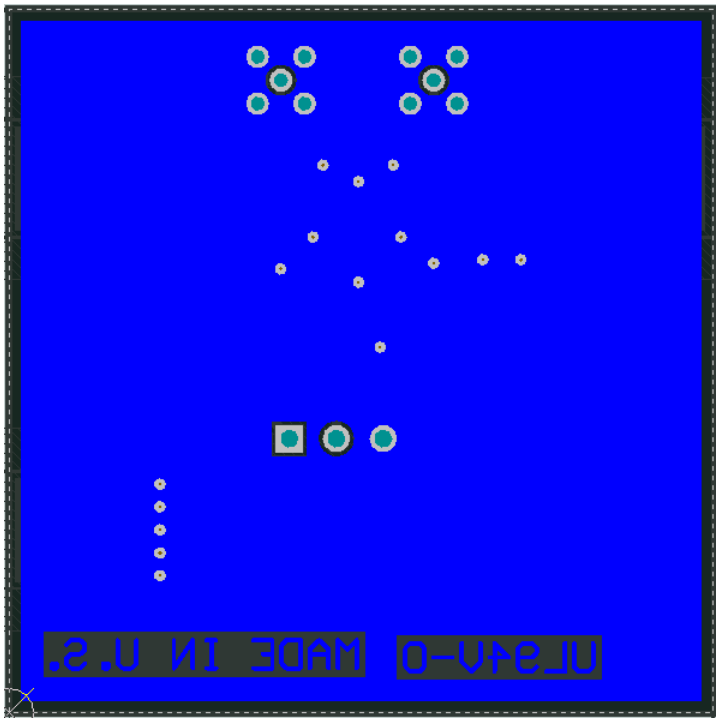


Figure 44. LP5907_SOT23: Internal Plane 3

A.5 LP5907_X2SON

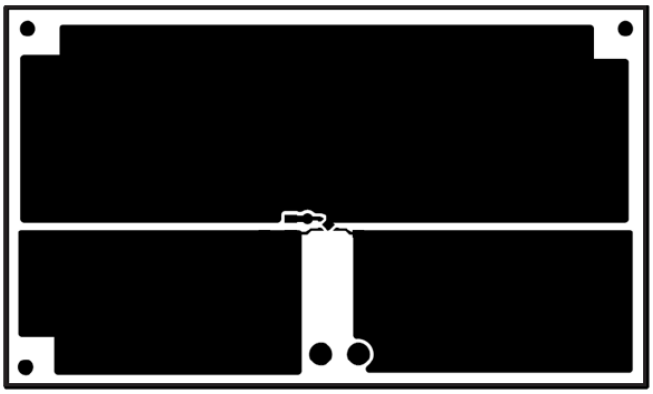


Figure 45. LP5907_X2SON: Top Layer

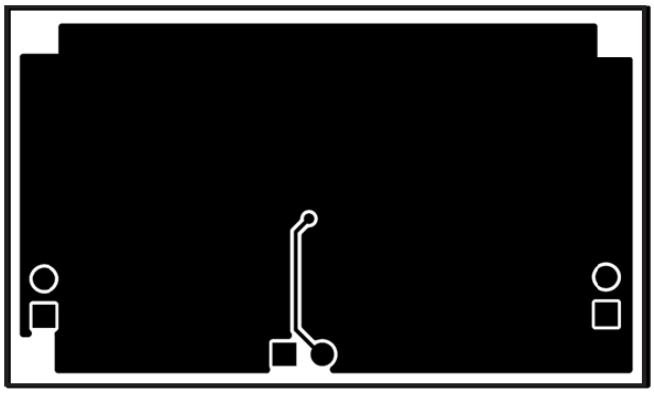
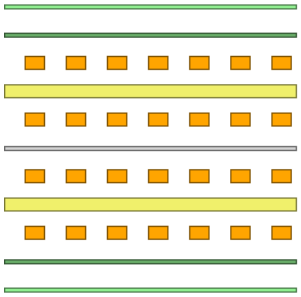


Figure 46. LP5907_X2SON: Bottom Layer

A.6 LP5910_WSON



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant	Pullback (mil)	Orientation
Top Overlay	Overlay						
Top Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5		
L1(TOP)	Signal	Copper	1.4				Top
Dielectric1	Dielectric	Core	10	FR-4	4.6		
L2	Signal	Copper	1.4				Not Allowed
Dielectric2	Dielectric	Prepreg	35	FR-4	4.6		
L3	Signal	Copper	1.4				Not Allowed
Dielectric3	Dielectric	Core	10	FR-4	4.6		
L4(BOT)	Signal	Copper	1.4				Bottom
Bottom Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5		
Bottom Overlay	Overlay						

Figure 47. LP5910_WSON: Layer Stackup

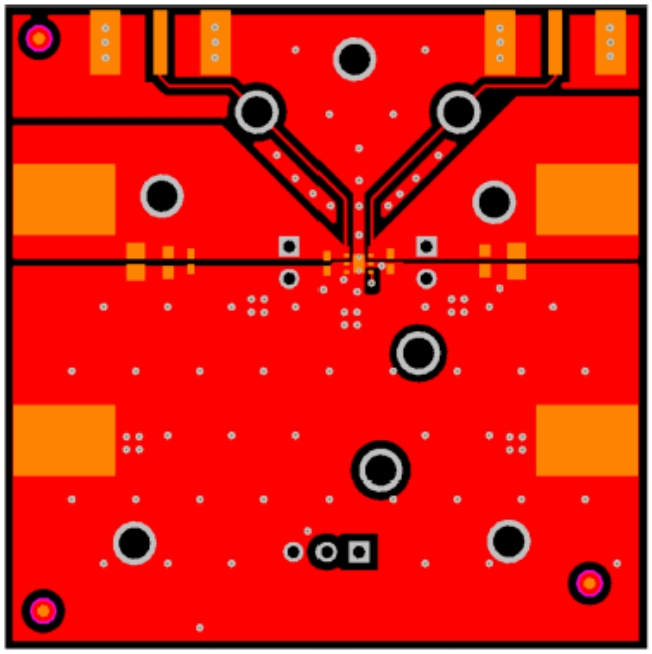


Figure 48. LP5910_WSON: Top Layer

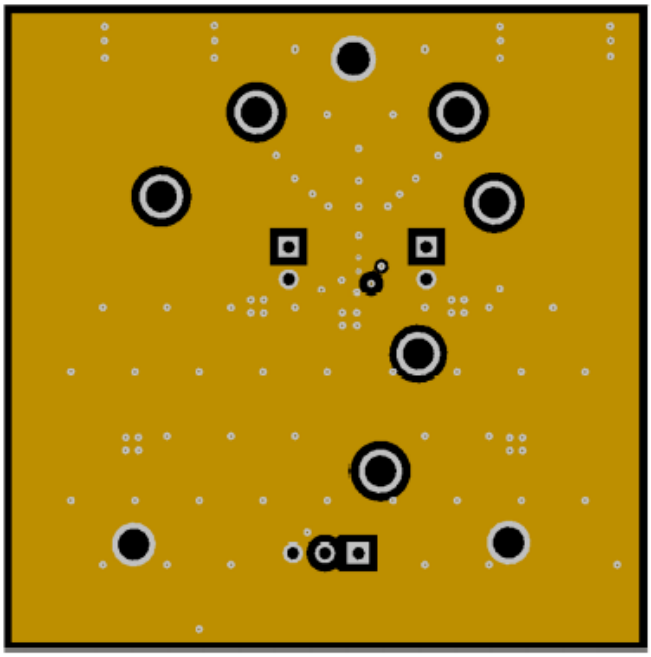


Figure 49. LP5910_WSON: L1

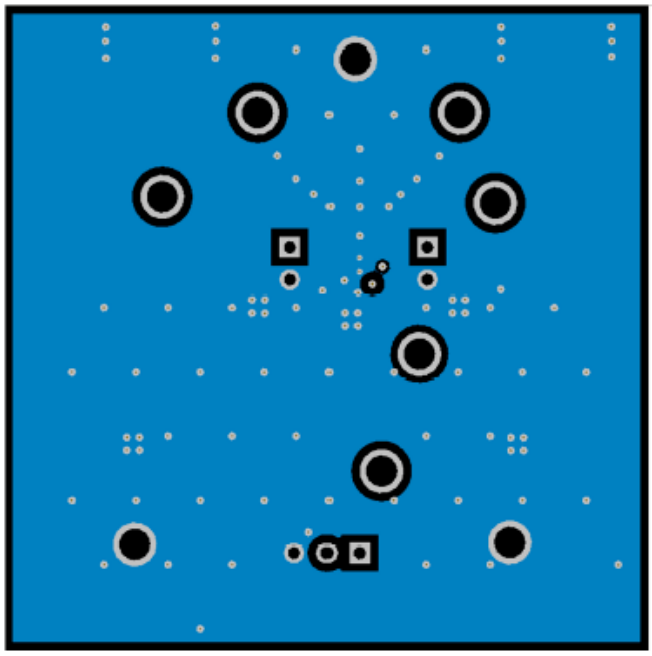


Figure 50. LP5910_WSON: L2

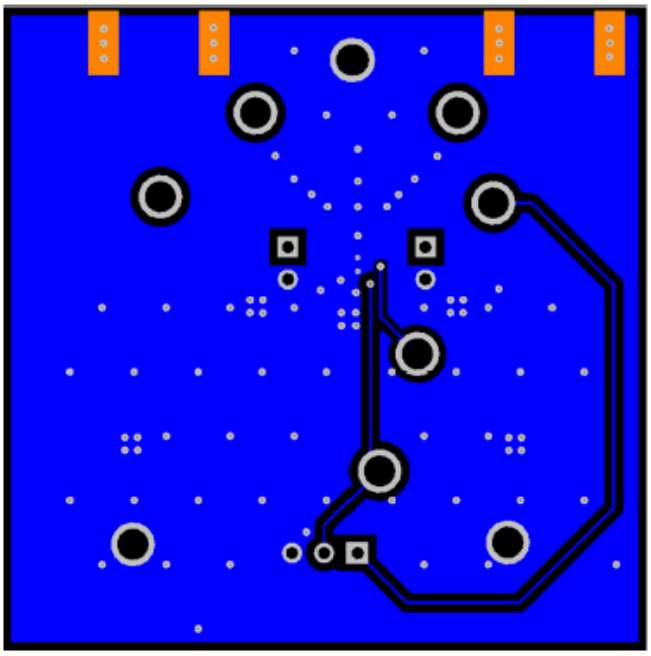
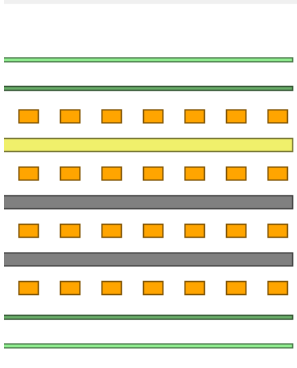


Figure 51. LP5910_WSON: Bottom Layer

A.7 LP5910_BGA



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant	Pullback (mil)	Orientation
Top Overlay	Overlay						
Top Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5		
L1(TOP)	Signal	Copper	1.4				Top
Dielectric1	Dielectric	Core	10	FR-4	4.8		
L2	Signal	Copper	1.4				Not Allowed
Dielectric2	Dielectric	None	35.6	FR-4	4.8		
L3	Signal	Copper	1.4				Not Allowed
Dielectric3	Dielectric	None	10	FR-4	4.8		
L4(BOT)	Signal	Copper	1.4				Bottom
Bottom Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5		
Bottom Overlay	Overlay						

Figure 52. LP5910_BGA: Layer Stackup

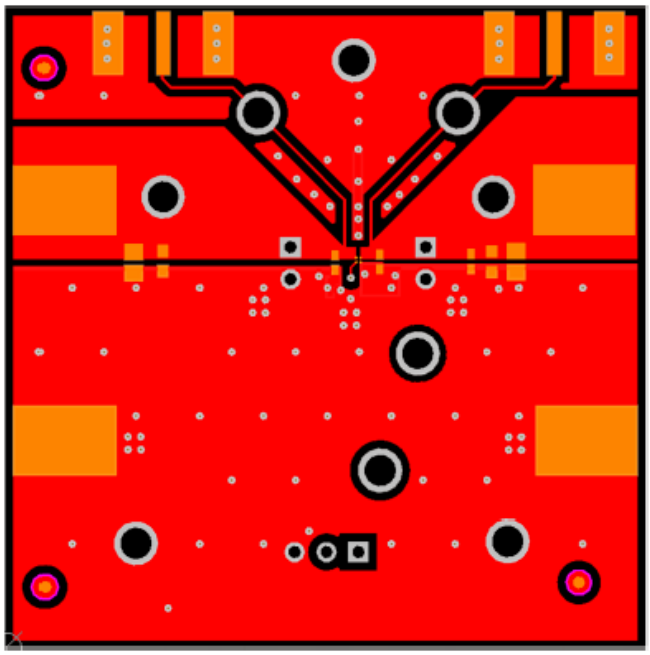


Figure 53. LP5910_BGA: Top Layer

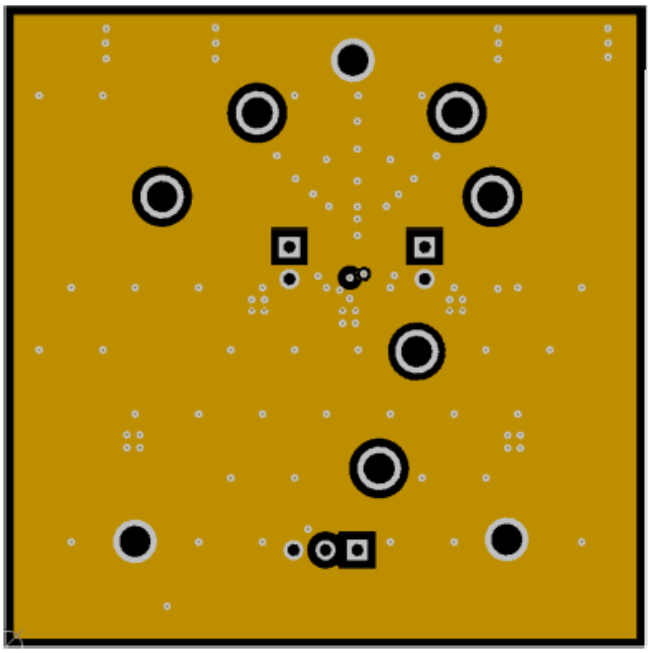


Figure 54. LP5910_BGA: L1

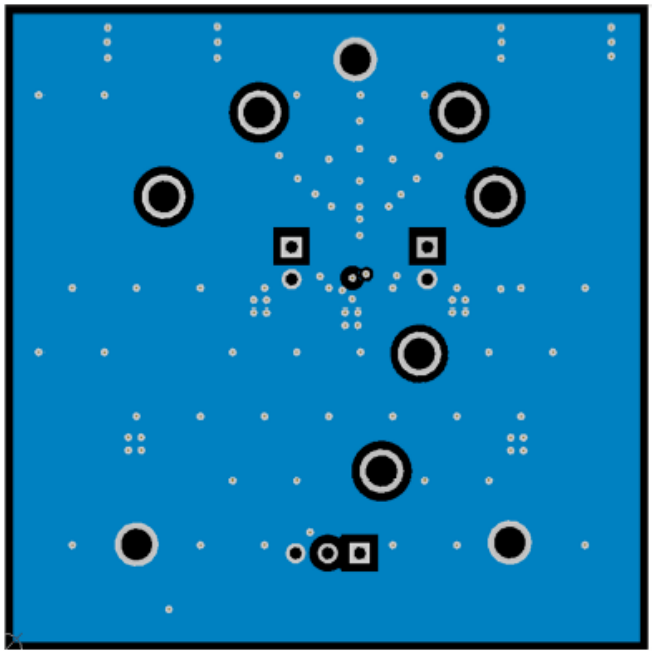


Figure 55. LP5910_BGA: L2

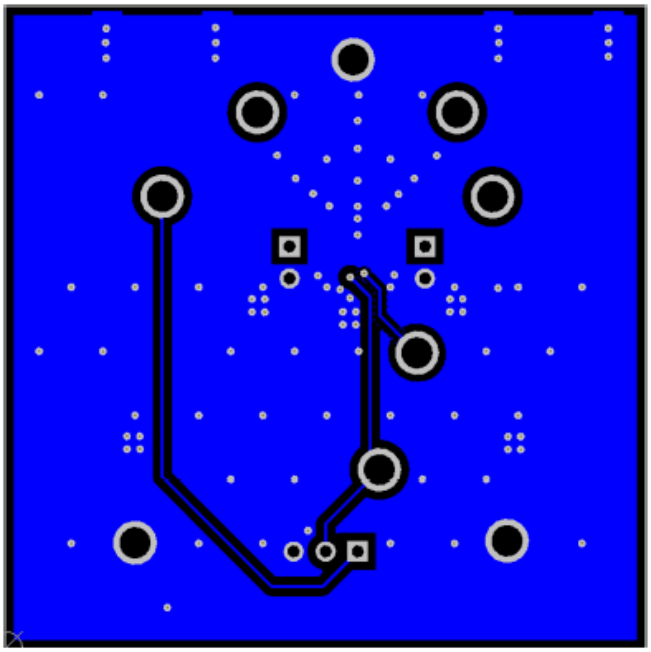


Figure 56. LP5910_BGA: Bottom Layer

References

Semiconductor and IC Package Thermal Metrics (SPRA953)

PowerPAD™ Thermally Enhanced Package (SLMA002)

AN-1112 DSBGA Wafer Level Chip Scale Package (SNVA009)

MicroStar BGA_ Packaging Reference Guide (SSYZ015)

AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Packages (SNVA183)

Appendix E: Understanding Integrated Circuit Package Power Capabilities

One-Page Thermal Reference Sheet (SLRR012)

Linear Regulator Design Guide For LDOs (SLVA118)

Using New Thermal Metrics (SBVA025)

Measuring the Thermal Impedance of LDOs in Situ (SLVA422)

Using Thermal Calculation Tools for Analog Components (SLUA566)

Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs (SZZA017)

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