Application Note

Power Supply Design for Semidrive X9P/X9U

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ABSTRACT

This document details the design considerations of a power solution for the Semidrive X9P/X9U SoC (system-on-chip) power rails using the LP8756x-Q1, LP8752x-Q1, and LP8732-Q1 family power management ICs. Additional TPS74501-Q1 LDOs are used for the peripheral rails. This power solution assumes an input voltage of 5 V (±5%). If the system input voltage is higher, for example a car battery, a buck converter as a pre-regulator with high enough current capability should be used to generate a supply voltage of 5 V. Automotive qualified components are used for the power solution.

The LP875610B-Q1 has four buck converters configured to work as single 4-phase converter with maximum 16A load current for the core rail. LP87562R-Q1 is configured to work as 3-phase converter for the CPU rail and then additional single phase rail for the peripherals. LP87521S-Q1 has four buck converters configured to work as single 4-phase converter with maximum 10A load current for the GPU rail. LP875241J-Q1 is configured to work as four single phase converter for the peripheral rails. LP873248-Q1 is used for the safety power rails. These devices are OTP programmable, meaning default register values are set in TI production line to desired values for this platform without further need for customer to change settings through I^2C bus. Full orderable part numbers for these OTP spins are LP875610BRNFRQ1, LP87562RRNFRQ1, LP87521SRNFRQ1, LP875241JRNFRQ1, and LP873248RHDRQ1. See the Technical Reference Manuals for the specific part numbers for more details on the OTP settings.

This power solution is an example how Semidrive X9P/U required rails can be powered with TI PMICs. Sequencing is handled through programmable startup and or shutdown delays of the PMICs and GPIOs and it only requires a single Enable signal from the system to initiate the sequencing. This power solution is possible to customize and optimize based on the actual use case regarding current requirements and used peripherals.

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Trademarks

1 Design Parameters

Table 1-1 shows the power rails, load requirements and Measurements shows typical performance data.

Table 1-1. Design Parameters

VOLTAGE (V)	RAIL NAME	MAX LOAD (mA)	LOAD CAPABILITY (mA)	SOURCE	Domain
1.8	VDD_RTC_1V8	< 500	500	TPS74501-Q1 (LDO)	RTC
0.8	VDDIO_RTC_0V8	< 500	500	TPS74501-Q1 (LDO)	RTC
0.8	VSFT_0V8	1500	2000	LP873248-Q1 Buck0	Safety
1.8	VDDA_SAF	720	2000	LP873248-Q1 Buck1	Safety
3.3	VDDIO_GPIO(1)	< 300	300	LP873248-Q1 LDO0	Safety
3.3	VDDIO_GPIO(2)	< 300	300	LP873248-Q1 LDO1	Safety
0.8	VDD_AP_0V8, VDD_DRAM_0V8	16000	16000	LP875610B-Q1 B0+B1+B2+B3	Application Processor
0.85	VDD_CPU_0V8	12000	12000	LP87562R-Q1 B0+B1+B2	Application Processor
0.8	VDD_MIPI_0V8, VDD_PCIE_0V8, VDD_USB	900	4000	LP87562R-Q1 B3	Application Processor
0.85	VDD_GPU_0V8	10000	10000	LP87521S-Q1 B0+B1+B2+B3	Application Processor
1.8	VDDA_1V8	2280	2500	LP875241J-Q1 B0	Application Processor
3.3	VDDH_3V3	1200	2500	LP875241J-Q1 B1	Application Processor
1.1	VDDQ_DRAM	3000	4000	LP875241J-Q1 B2	Application Processor
0.6	VDDLP_DRAM	600	1000	LP875241J-Q1 B3	Application Processor
1.8	VDD_LP4_1V8	200	500	TPS74501-Q1 (LDO)	Application Processor

2 Power Solution

Figure 2-1 shows power tree with LP875610B-Q1, LP87562R-Q1, LP87521S-Q1, LP875241J-Q1, and TPS74501-Q1 devices powering the X9P/U application processor rails.

Figure 2-2 shows power tree with LP873248-Q1 PMIC powering the X9P/U safety rails.

Figure 2-3 shows power tree with two TPS74501-Q1 LDOs powering the X9P/U RTC rails.

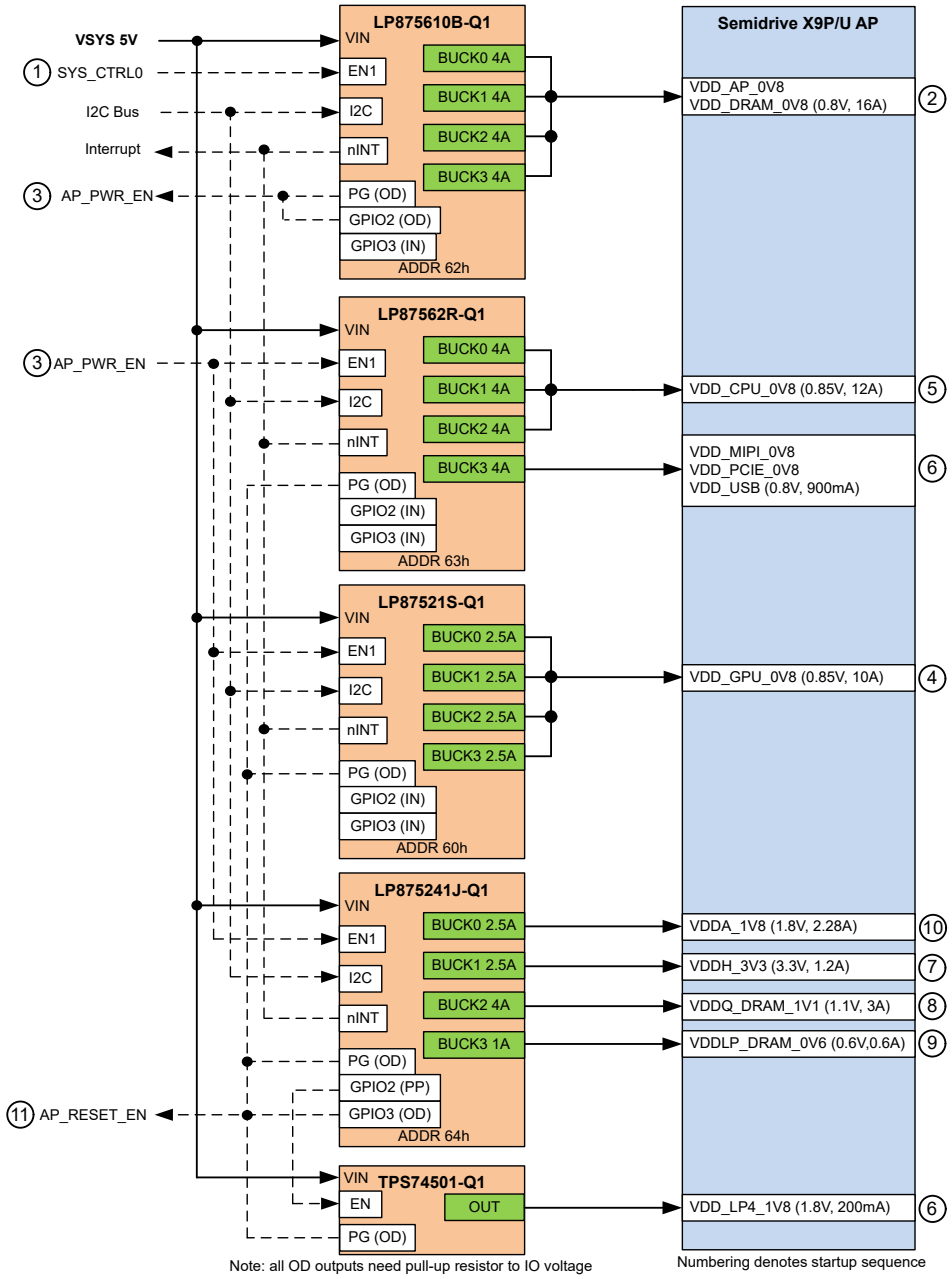

Figure 2-1. Semidrive X9P/U AP Power Block Diagram

Main features:

- 5 V supplied from pre-regulator
- After the devices are powered, the microcontroller or preregulator PGOOD can set the SYS_CTRL0 high to initiate the startup sequence for application processor rails.
- Startup and or shutdown delays are controlled internally in the LP875x-Q1 sequencers and discrete LDO is controlled with PMIC GPIO with pre-set delays.

- I²C can be used to read status registers and reset interrupts.
- PMIC devices have dedicated I²C address so they can share the same I²C bus.
- Combined PG signal from LP875x-Q1 and TPS74501-Q1 act as AP_RESET_EN signal for the SoC. Any failure on the rail voltages will keep the SoC in reset state until fault is cleared.

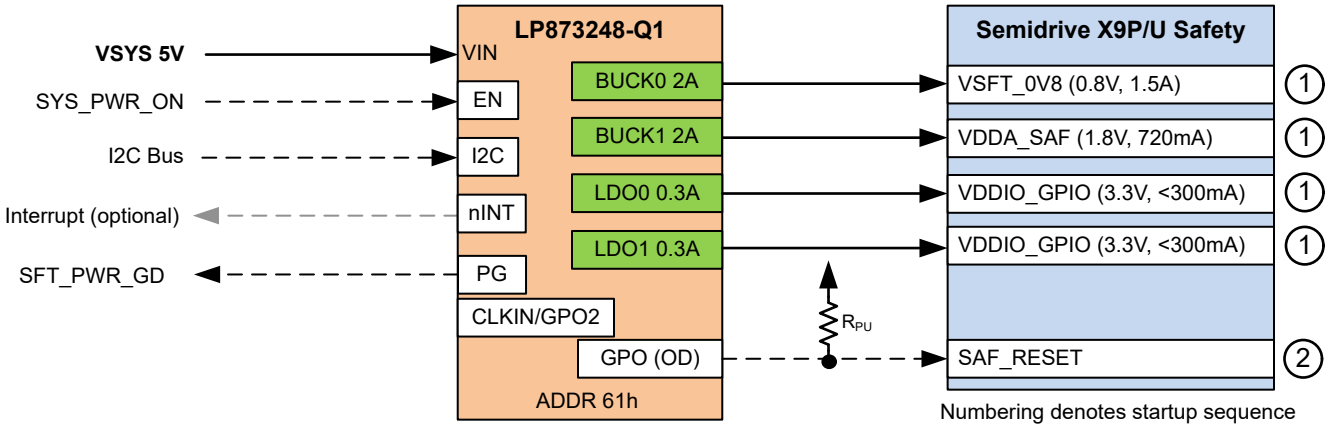

Figure 2-2. Semidrive X9P/U Safety Power Block Diagram

Main features:

- 5 V supplied from pre-regulator
- After the devices are powered, the microcontroller or preregulator PGOOD can set the SYS_PWR_ON high to initiate the startup sequence for safety rails.
- Startup delays are controlled internally in the LP873248-Q1 sequencer.
- I²C can be used to read status registers and reset interrupts.
- All PMIC devices in this system have dedicated I²C address so they can share the same I²C bus.
- GPO signal from LP873248-Q1 act as SAF_RESET signal for the SoC. SFT_PWR_GD signal can be used for fault indication, or combined with the SAF_RESET signal (both outputs are open-drain).

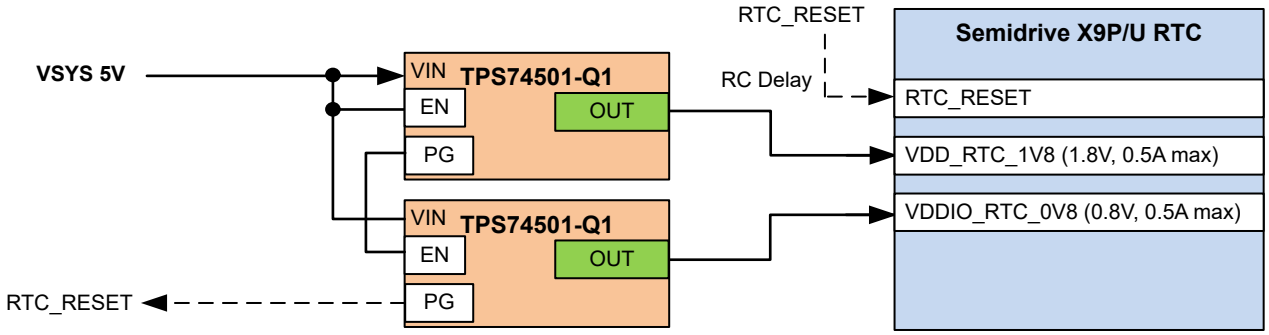

Figure 2-3. Semidrive X9P/U RTC Power Block Diagram

Main features:

- 5 V supplied from pre-regulator
- VDD_RTC_1V8 supply starts as soon as supply voltage reaches TPS74501-Q1 UVLO rising threshold (1.33-V typ).
- VDDIO_RTC_0V8 starts when VDD_RTC_1V8 has reached the target voltage and PG is set high.
- When VDDIO_RTC_0V8 has reached the target voltage level the PG is set high. Additional RC delay is used for the RTC_RESET signal.

3 Sequencing

3.1 Startup, Application Processor

Figure 3-1 shows startup timing of the power rails and corresponding signals.

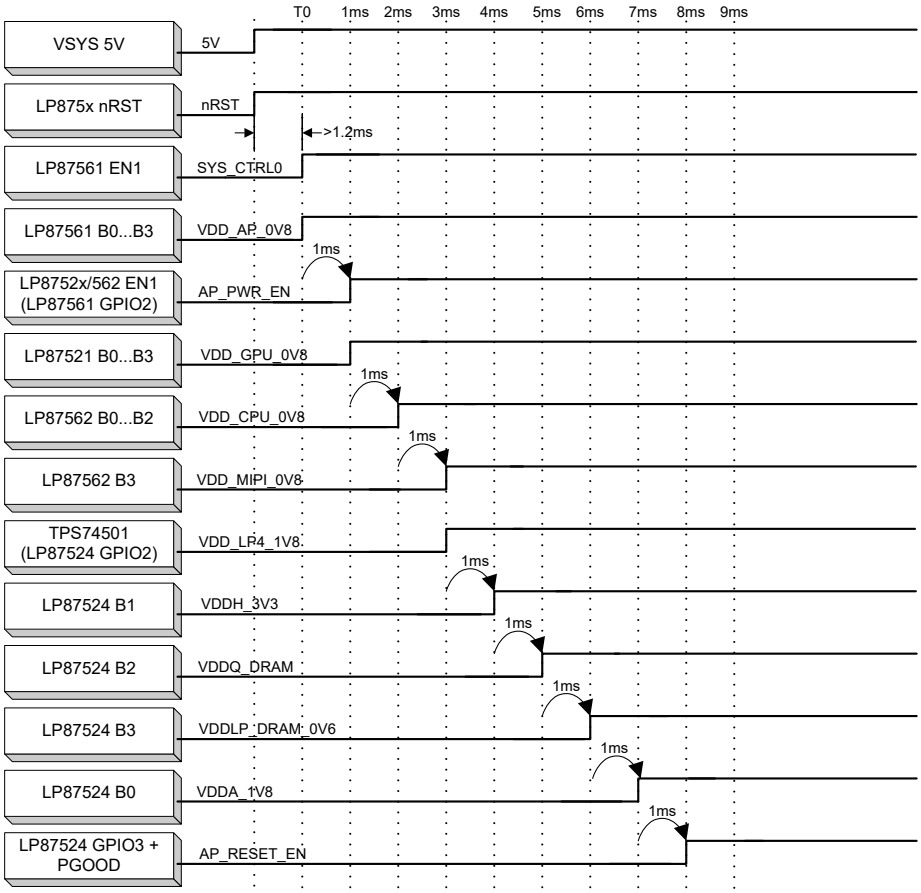

Figure 3-1. Application Processor Power Startup Timing Diagram

3.2 Shutdown, Application Processor

Figure 3-2 shows an example of shutdown timing of the application processor power rails and corresponding signals.

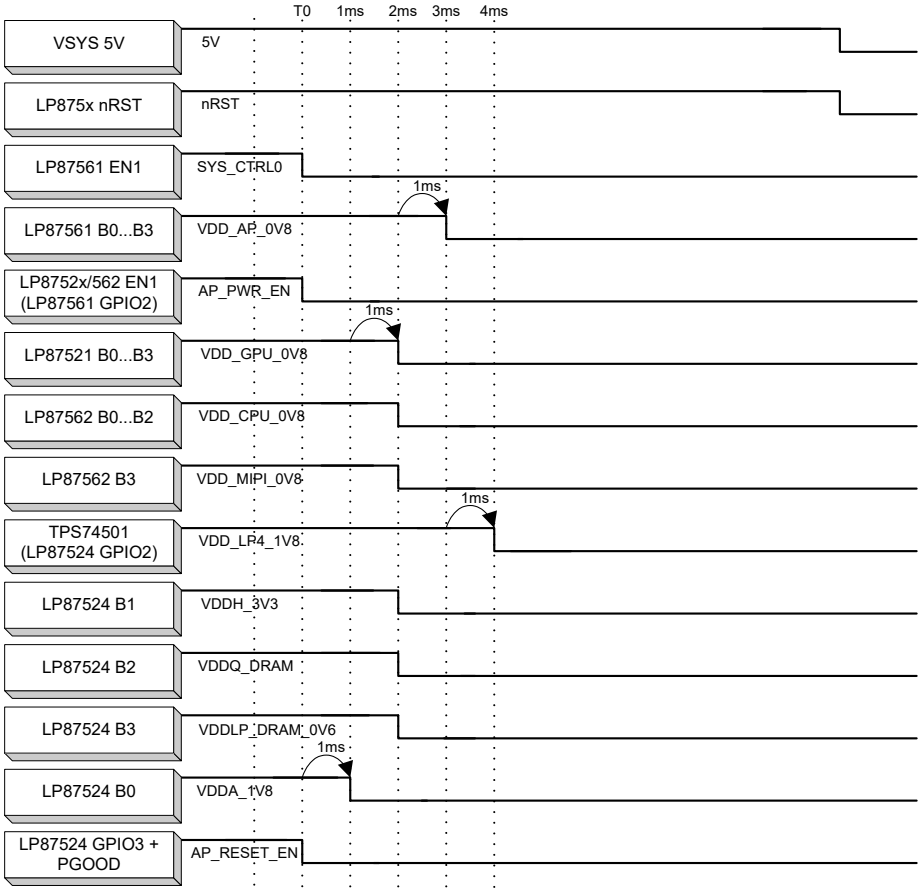

Figure 3-2. Application Processor Shutdown Timing Diagram

3.3 Startup, Safety

Figure 3-3 shows startup timing of the safety power rails and corresponding signals.

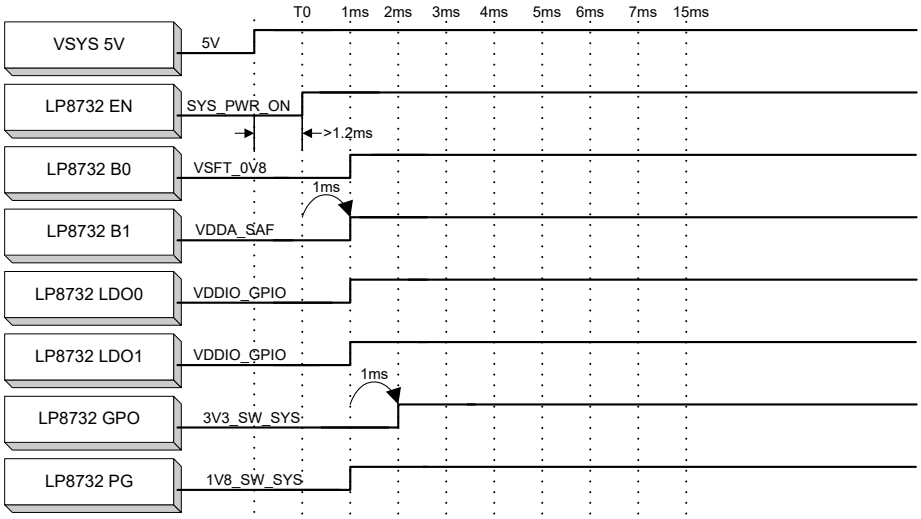

Figure 3-3. Safety Power Startup Timing Diagram

3.4 Shutdown, Safety

Figure 3-4 shows an example of shutdown timing of the safety power rails and corresponding signals.

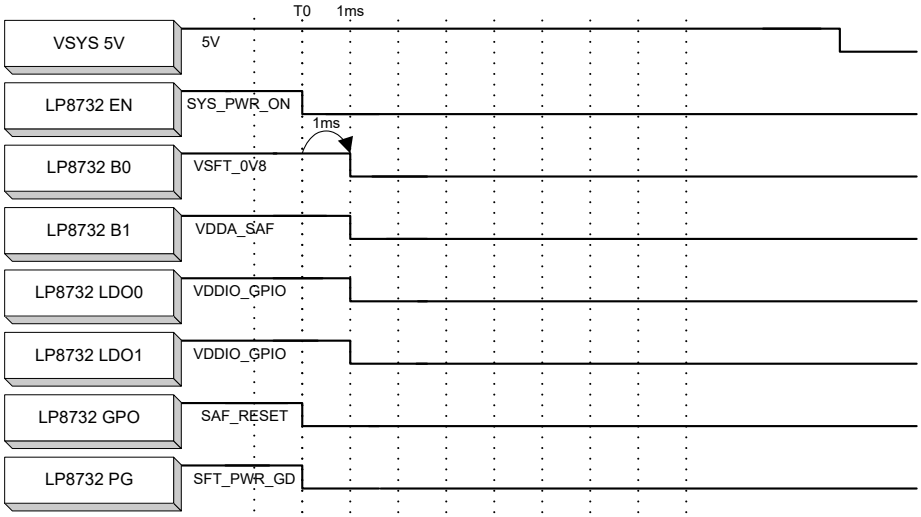

Figure 3-4. Safety Shutdown Timing Diagram

3.5 Startup, RTC

Figure 3-1 shows startup timing of the RTC power rails and corresponding signals.

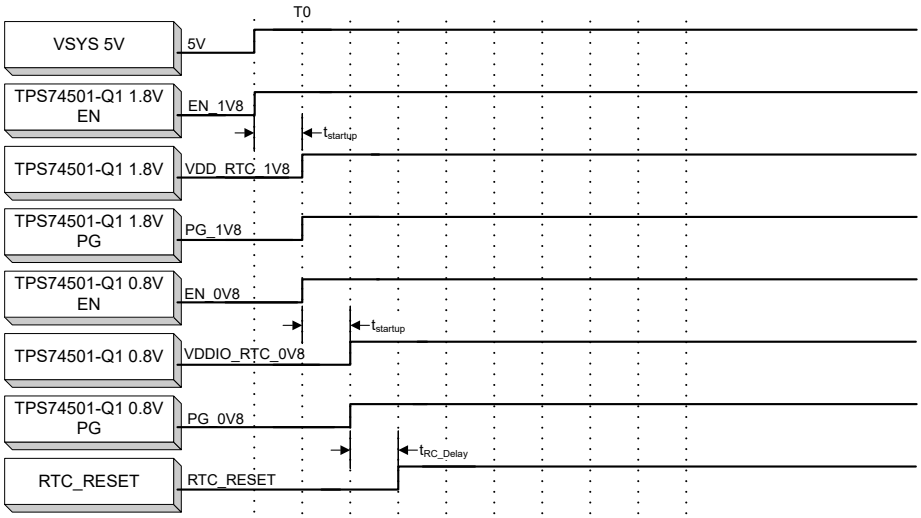

Figure 3-5. RTC Power Startup Timing Diagram

3.6 Shutdown, RTC

Figure 3-2 shows an example of shutdown timing of the RTC power rails and corresponding signals.

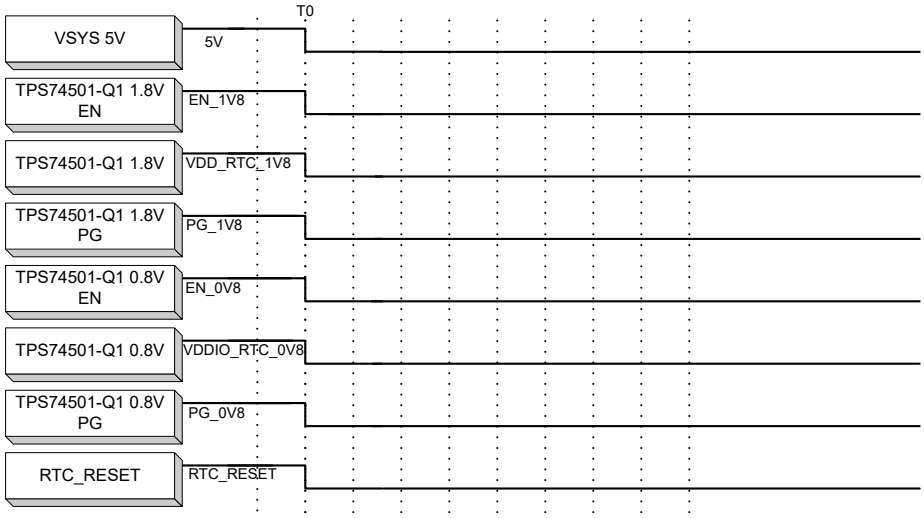

Figure 3-6. RTC Shutdown Timing Diagram

4 Schematic

Figure 4-1 through Figure 4-7 show the Semidrive X9P/X9U power tree schematic with critical components.

For guidance on layout, please refer to the data sheet application section and EVM user guide for the particular device.

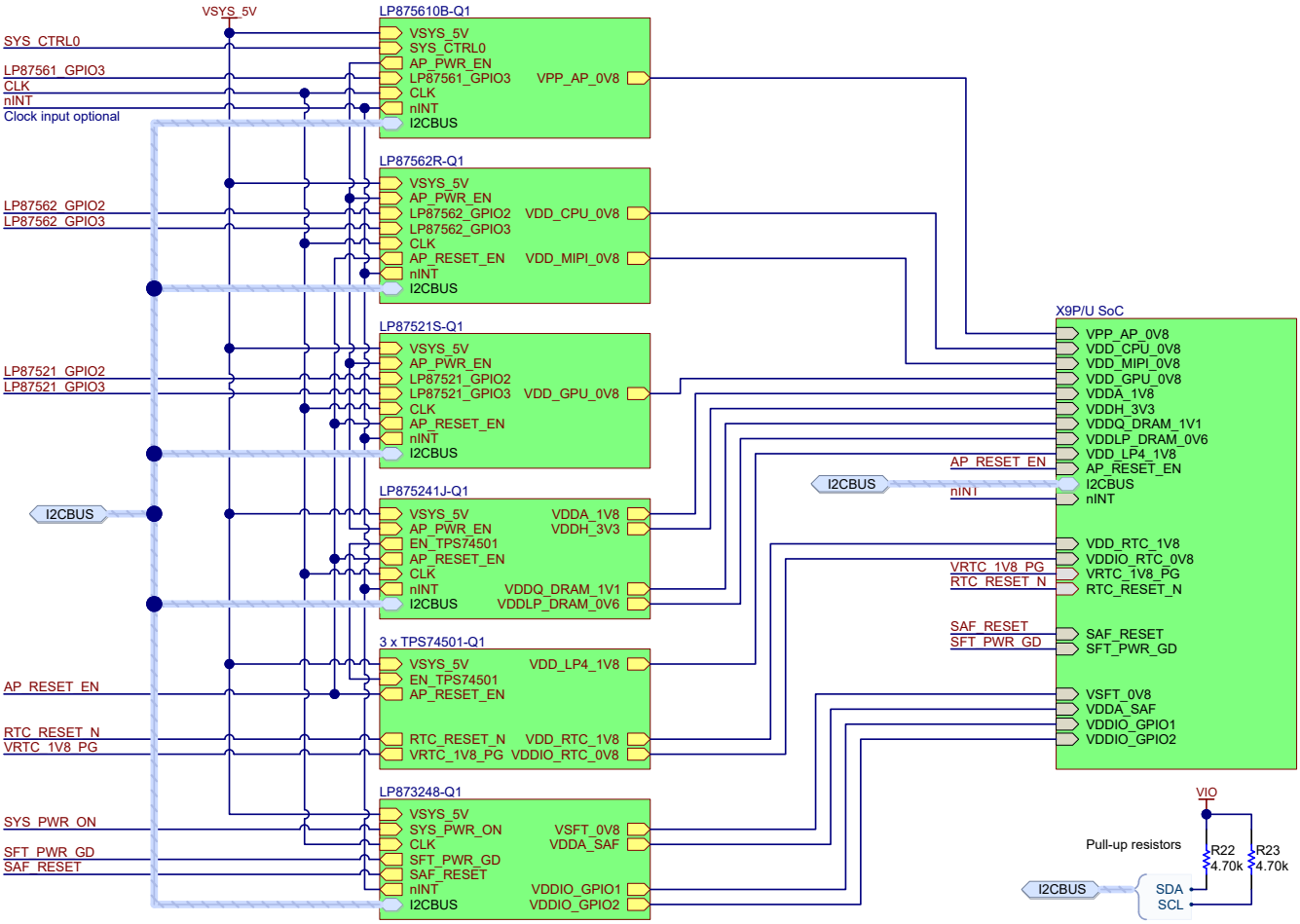

Figure 4-1. X9P/X9U Top Level Schematic

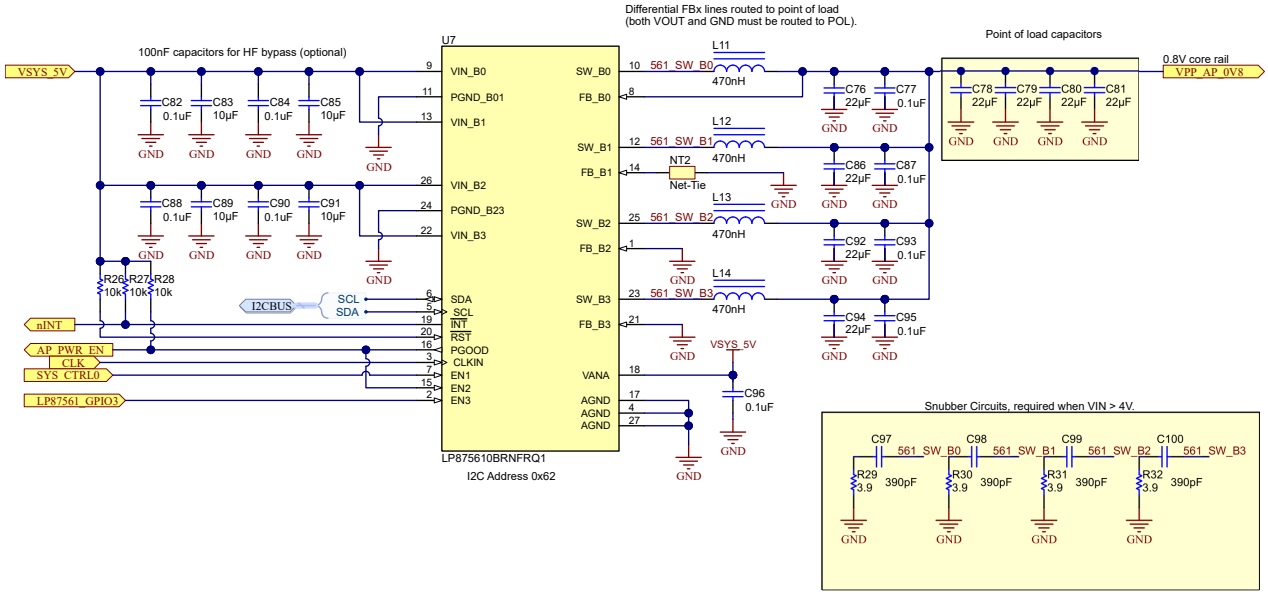

Figure 4-2. LP875610B-Q1 Schematic

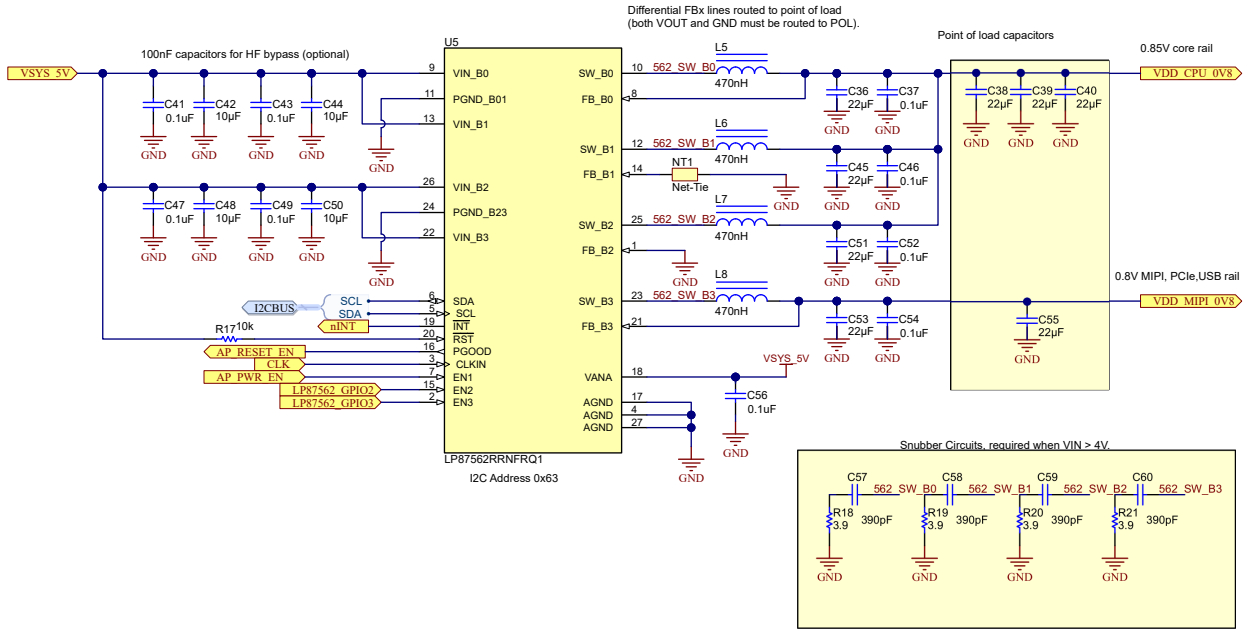

Figure 4-3. LP87562R-Q1 Schematic

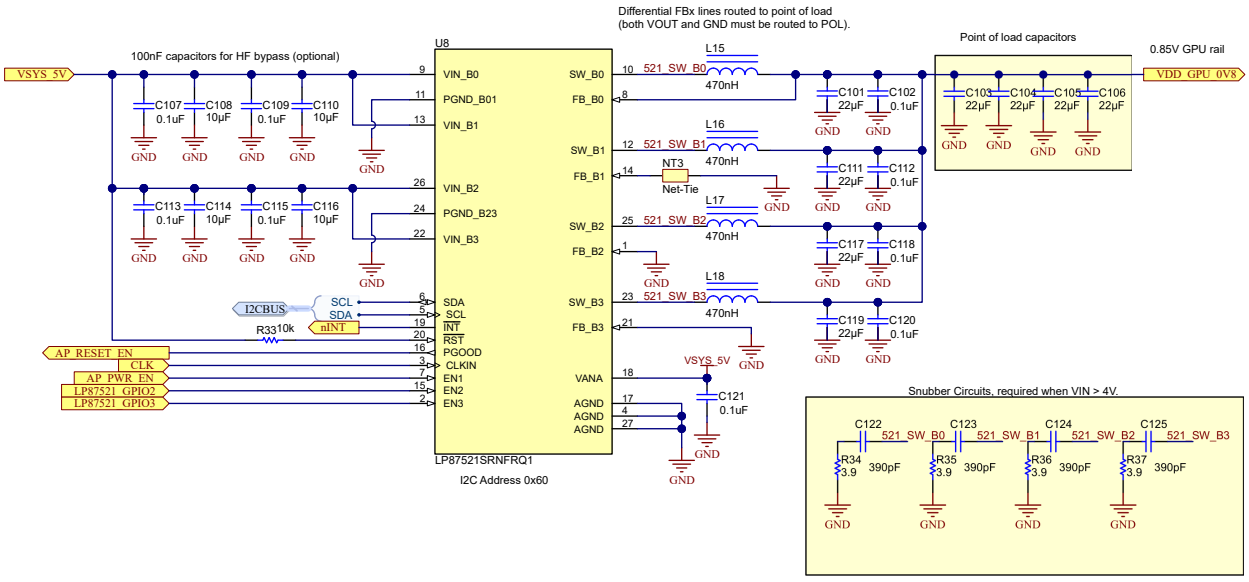

Figure 4-4. LP87521S-Q1 Schematic

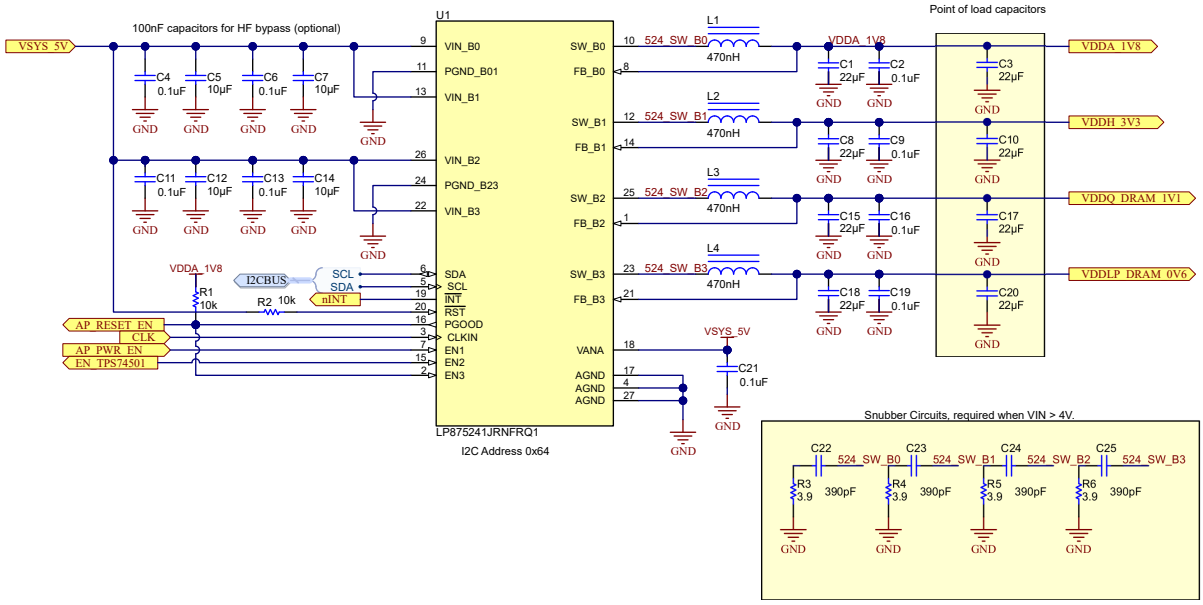

Figure 4-5. LP875241J-Q1 Schematic

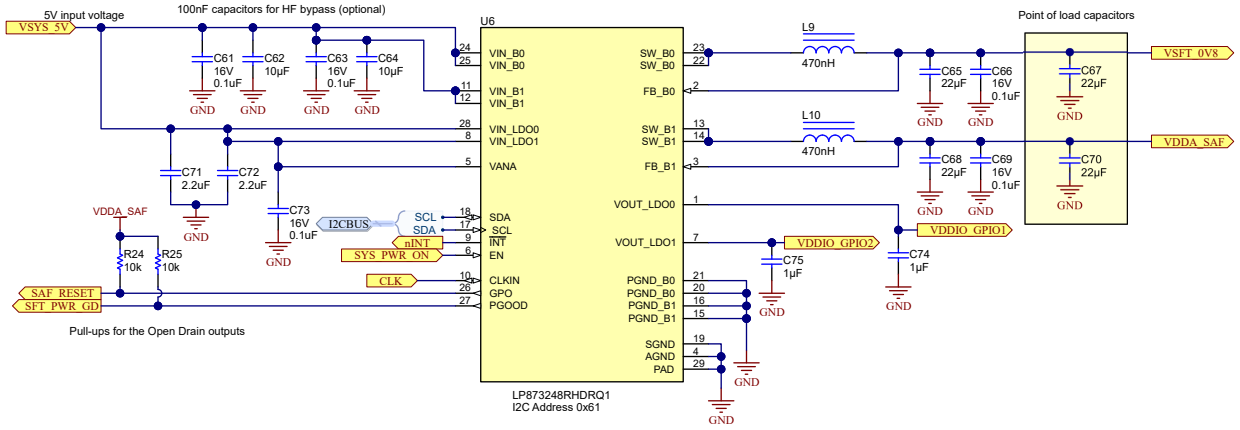

Figure 4-6. LP873248-Q1 Schematic

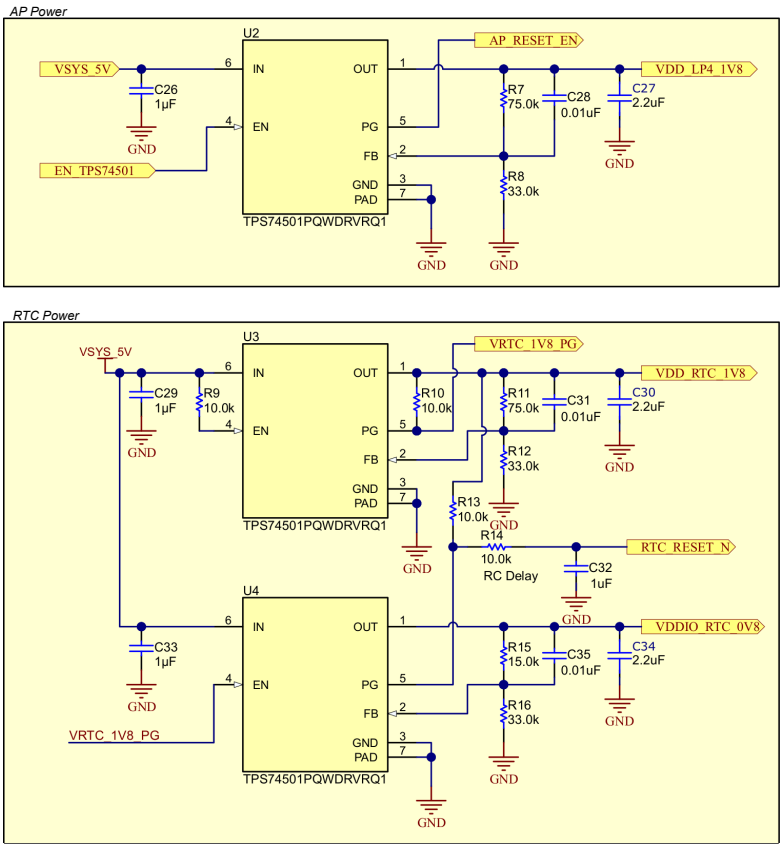

Figure 4-7. TPS74501-Q1 Schematic

5 Software Drivers

This solution supports control through I^2C bus.

Linux drivers for the LP875x-Q1 and LP8732-Q1 are available in public git repository. These can be used to help integrate the LP875x-Q1 / LP8732-Q1 control to system software:

LP8756x-Q1

- https://github.com/torvalds/linux/blob/master/drivers/mfd/lp87565.c
- https://github.com/torvalds/linux/blob/master/drivers/regulator/lp87565-regulator.c
- https://github.com/torvalds/linux/blob/master/drivers/gpio/gpio-lp87565.c

LP8732-Q1

- https://github.com/torvalds/linux/blob/master/drivers/mfd/lp873x.c
- https://github.com/torvalds/linux/blob/master/drivers/regulator/lp873x-regulator.c
- https://github.com/torvalds/linux/blob/master/drivers/gpio/gpio-lp873x.c

Note: Every header file is in the *include* folder starting from the root directory. So once in *include folder*, the user can navigate to the relevant header file. For example, the LP87565.h file: https://github.com/torvalds/linux/blob/master/include/linux/mfd/lp87565.h.

6 Recommended External Components

Table 6-1 shows the recommended external components to use in this solution with the LP8756x-Q1, LP8752x-Q1, LP873248-Q1, and TPS74501-Q1. It also shows the total solution size, including the PMIC device and the external components.

Table 6-1. Bill of Materials

COUNT	VENDOR	PART NUMBER	SYSTEM COMPONENT	W (mm)	L (mm)	H (mm)	UNIT AREA(1)	TOTAL BOARD AREA(1)
4	TI	LP875x-Q1	Configurable 4-phase Buck	4.00	4.50	0.90	27.50	110.00
16	Murata	DFE252012PD-R47M	LP875x Inductor 0.47 µH, Imax 4.0A, Rdc typ 21mOhm	2.50	2.00	1.20	10.50	168.00
16	Murata	GCM21BR71A106KE22	LP875x SMPS Input Capacitor 10µF, 10 V, 10%	2.00	1.25	1.25	6.75	108.00
32	Murata	GCM21BD70J226ME35	LP875x SMPS Output Capacitor 22 µF, 10 V, 10%	2.00	1.25	1.25	6.75	216.00
4	Murata	GCM155R71C104KA55D	LP875x Input Capacitor 0.1µF, 16 V, 10%	1.00	0.50	0.50	3.00	12.00
16	TDK	CGA2B2C0G1H391J050BA	LP875x Snubber capacitor, 390 pF	1.00	0.50	0.50	3.00	48.00
16	Vishay-Dale	CRCW04023R90JNED	LP875x Snubber resistor, 3R9	1.00	0.50	0.50	3.00	48.00
1	TI	LP8732-Q1	Configurable 2 Bucks and 2 LDOs	5.00	5.00	0.90	36.00	36.00
2	Murata	DFE252012PD-R47M	LP8732-Q1 Inductor 0.47 µH, Imax 4.0 A, Rdc typ 21mOhm	2.50	2.00	1.20	10.50	21.00
2	Murata	GCM21BR71A106KE22	LP8732-Q1 SMPS Input Capacitor 10 µF, 10 V, 10%	2.00	1.25	1.25	6.75	13.50
4	Murata	GCM21BD70J226ME35	LP8732-Q1 SMPS Output Capacitor 22 µF, 10 V, 10%	2.00	1.25	1.25	6.75	27.00
2	Murata	GRT155C71A225KE13	LP8732-Q1 LDO Input Capacitor 2.2 µF, 6.3 V, 10%	1.00	0.50	0.50	3.00	6.00
2	Murata	GCM155C71A105KE38	LP8732-Q1 LDO Output Capacitor 1.0 µF, 16 V, 10%	1.00	0.50	0.50	3.00	6.00
1	Murata	GCM155R71C104KA55D	LP8732-Q1 Input Capacitor 0.1 µF, 16 V, 10%	1.00	0.50	0.50	3.00	3.00
3	TI	TPS74501-Q1	Low Dropout Regulator	2.00	2.00	1.00	9.00	27.00
3	Murata	GCM188R71C105KA64D	LDO Input Capacitor 1 µF	1.00	0.50	0.50	3.00	9.00
3	Murata	GRT155C71A225KE13	LDO Output Capacitor 2.2 µF, 6.3 V, 10%	1.00	0.50	0.50	3.00	9.00
6			LDO Set resistors	1.00	0.50	0.50	3.00	18.00
3	TDK	CGA2B3X7R1H103K050BB	LDO CFF Capacitor 10 nF, 50 V, 10%	1.00	0.50	0.50	3.00	9.00
							TOTAL	894.50 mm^2
							Routing area calculated with 0.3 routing factor	383.36 mm^2
							Total area	1277.86 mm^2

(1) Assuming 1 mm keep-out around each component, and multiplying by component count

7 Measurements

Test data can be found in the Application Curves section of the following data sheets:

- *LP8756x-Q1 16A Buck Converter With Integrated Switches*
- *LP8752x-Q1 10-A Buck Converter With Integrated Switches*
- *LP8732xx-Q1 Dual High-Current Buck Converter and Dual Linear Regulator*
- *TPS745-Q1 500-mA LDO With Power-Good in Small Wettable Flank WSON Packages*

Additional bench test data for efficiency in specific conditions for this power tree can be seen in this section. TI PMIC Efficiency Estimation Tool (PEET) can be used also for calculating efficiency and thermal performance: PEET-GUI.

Measurements were taken on the LP87320Q1EVM with default components.

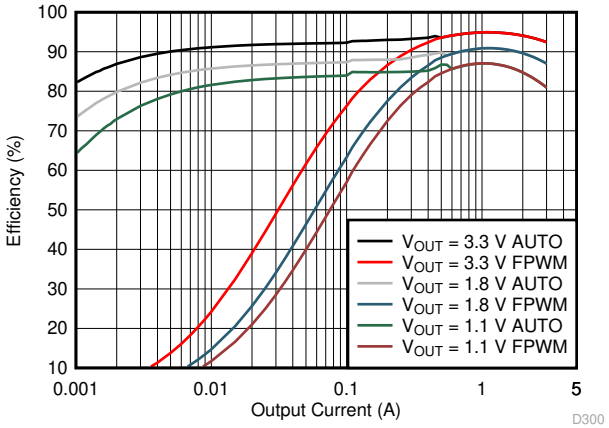

Figure 7-1. LP873248-Q1 Efficiency with Vin = 5 V, 25°C

8 Summary

With this presented solution with the LP875610B-Q1, LP87562R-Q1, LP87521S-Q1, LP875241J-Q1, and LP873248-Q1 PMICs + discrete LDOs, it is possible to meet power requirements for Semidrive X9P/X9U application processor while maintaining good efficiency. Sequencing is handled in PMICs and only one EN signal is needed from the controller. Solution is compact due to minimum number of external components. I^2C control allows diagnostic and PMIC control if needed.

9 References

See these references for additional information:

1. Texas Instruments, *LP8756x-Q1 16A Buck Converter With Integrated Switches* data sheet.
2. Texas Instruments, *LP875610B-Q1 Technical Reference Manual*,
3. Texas Instruments, *LP87562R-Q1 Technical Reference Manual*,
4. Texas Instruments, *LP8752x-Q1 10-A Buck Converter With Integrated Switches* data sheet.
5. Texas Instruments, *LP87521S-Q1 Technical Reference Manual*.
6. Texas Instruments, *LP875241J-Q1 Technical Reference Manual*.
7. Texas Instruments, *LP8732xx-Q1 Dual High-Current Buck Converter and Dual Linear Regulator* data sheet.
8. Texas Instruments, *LP873248-Q1 Technical Reference Manual* .
9. Texas Instruments, *TPS745-Q1 500-mA LDO With Power-Good in Small Wettable Flank WSON Packages* data sheet.

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