

Power Supply Design for Horizon Robotics Journey 3 Using LP87562S-Q1



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ABSTRACT

This document details the design considerations of a power solution for the Horizon Robotics Journey 3 (J3) SoC (system-on-chip) power rails using the LP87562S-Q1 power management IC. Additional TPS74801-Q1 LDO and TPS62442-Q1 dual bucks are used for the peripheral rails. This power solution assumes an input voltage of 3.3 V or 5 V ($\pm 10\%$). If the system input voltage is higher, for example a car battery, a buck converter as a pre-regulator should be used to generate a supply voltage of 3.3 V or 5 V. All components in this solution are automotive qualified.

The LP87562S-Q1 has four buck converters configured to work as single 3-phase converter for the core rail and additional single phase buck for the 1.8 V peripheral rail. This PMIC is OTP programmable, meaning default register values are set in TI production line to desired values for this platform without further need for customer to change settings. Full orderable part numbers for this OTP spin is LP87562SRNFRQ1. See the Technical Reference Manual for the specific part number for more details on the OTP settings.

This power solution is an example how required rails for J3 can be powered with TI PMICs. This power solution is possible to customize and optimize based on the actual use case regarding SoC variant, current requirements, used peripherals, and so forth. This solution supports also diagnostic and control through I²C bus.

Table of Contents

1 Design Parameters	2
2 Power Solution	2
3 Sequencing	3
3.1 Startup	3
3.2 Shutdown	3
4 Schematic	4
5 Software Drivers	5
6 Recommended External Components	6
7 Measurements	7
8 Summary	7
9 References	7

List of Figures

Figure 2-1. J3 Power Solution Block Diagram	2
Figure 3-1. J3 Power Startup Timing Diagram	3
Figure 3-2. Shutdown Timing Diagram	3
Figure 4-1. J3 Top Schematic	4
Figure 4-2. LP87562S-Q1 Schematic	4
Figure 4-3. TPS74801-Q1 Schematic	5
Figure 4-4. TPS62442-Q1 LDO Schematic	5

List of Tables

Table 1-1. Design Parameters	2
Table 6-1. Bill of Materials	6

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1 Design Parameters

Table 1-1 shows the power rails, load requirements, and startup or shutdown sequencing requirements and Measurements shows typical measurement data.

Table 1-1. Design Parameters

VOLTAGE (V)	RAIL NAME	LOAD CAPABILITY (mA)	SOURCE
0.8	VDD_CORE_0V8	12000	LP87562S-Q1 Buck0+1+2
1.8	VDD_1V8	4000	LP87562S-Q1 Buck3
0.8	VDD_0V8	1500	TPS74801-Q1
1.0	VDD_1V0	2000	TPS62442-Q1 Buck1
1.1	VDD_1V1	2000	TPS62442-Q1 Buck2

2 Power Solution

Figure 2-1 shows a block diagram of LP87562S-Q1, TPS74801-Q1, and TPS62442-Q1 devices powering the J3 SoC power rails.

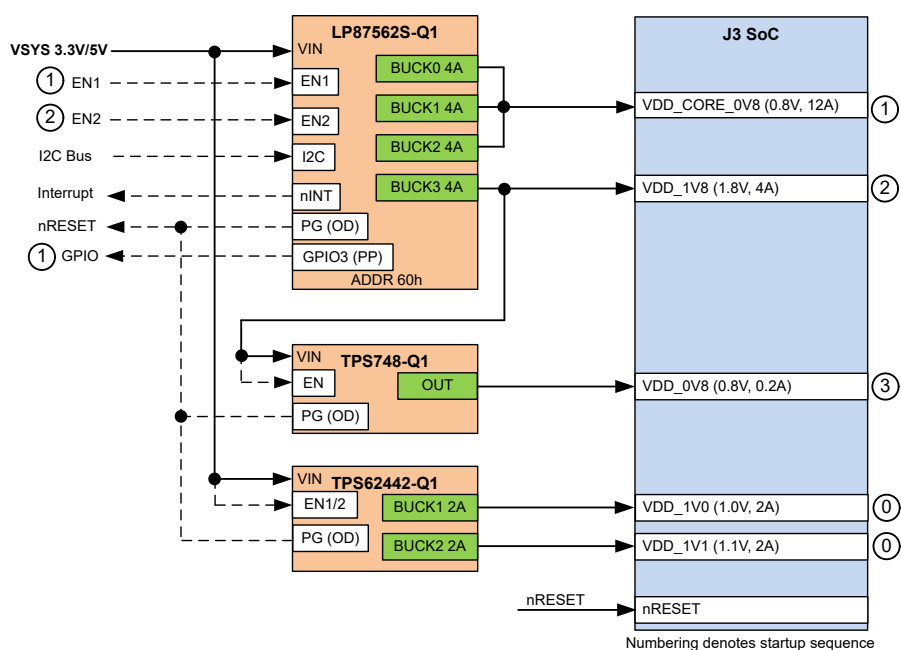


Figure 2-1. J3 Power Solution Block Diagram

Main features:

- Power sequencing for VDD_CORE_0V8 (EN1) and VDD_1V8 (EN2) are controlled with microcontroller or pre-regulator PG signal.
- I²C can be used to read status registers and reset interrupts.
- PGOOD signals act as nRESET signal for the SoC
- Interrupt signal can be used for fault detection
- LP87562S-Q1 GPIO3 output can be used to control other PMICs as well

3 Sequencing

3.1 Startup

Figure 3-1 shows an example startup timing of the power rails and corresponding signals.

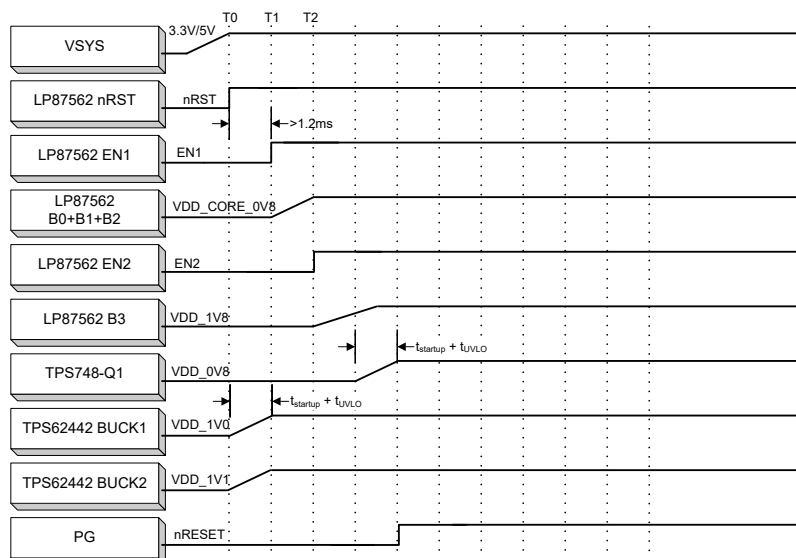


Figure 3-1. J3 Power Startup Timing Diagram

3.2 Shutdown

Figure 3-2 shows an example of shutdown timing of the power rails and corresponding signals.

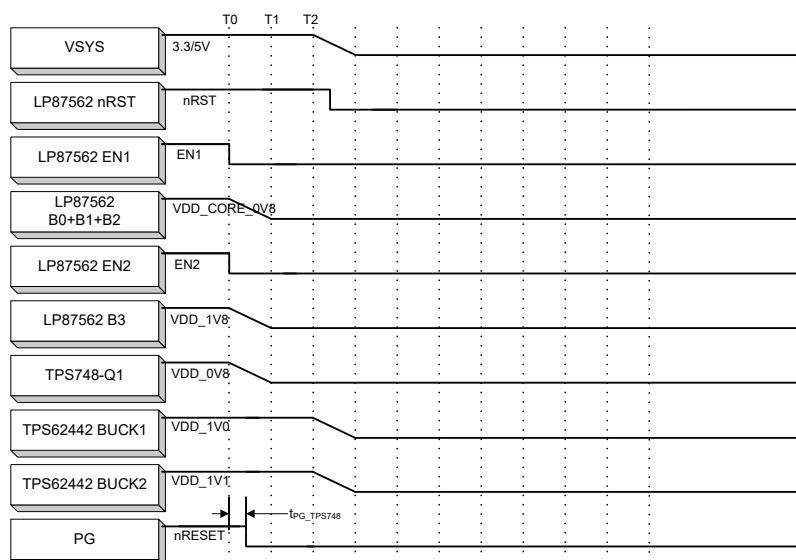


Figure 3-2. Shutdown Timing Diagram

4 Schematic

Figure 4-1 through Figure 4-4 show the J3 power tree schematic with critical components. Snubbers are needed for LP87562S-Q1 when input voltage of the system is >4 V, otherwise they are optional. For layout guidance please refer to the corresponding device data sheet and EVM user guide.

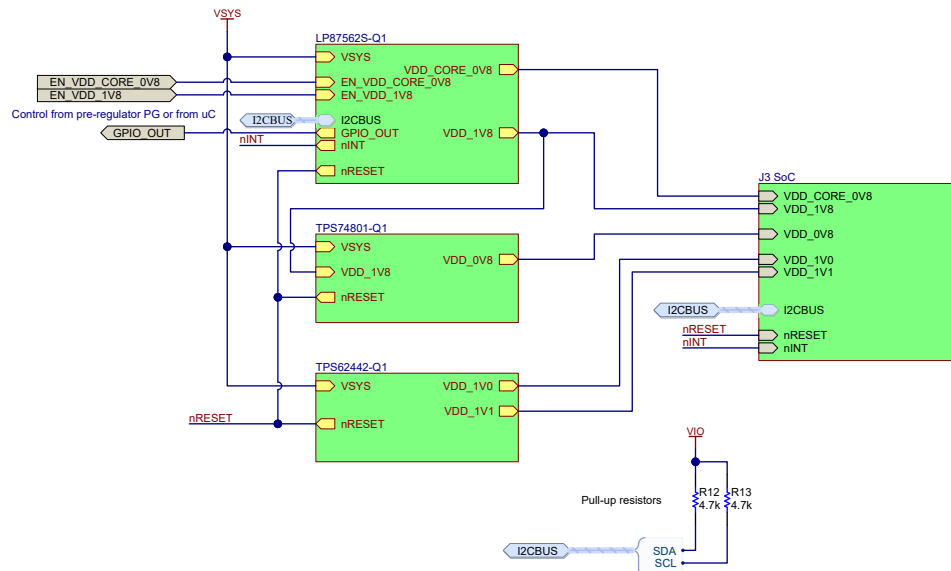


Figure 4-1. J3 Top Schematic

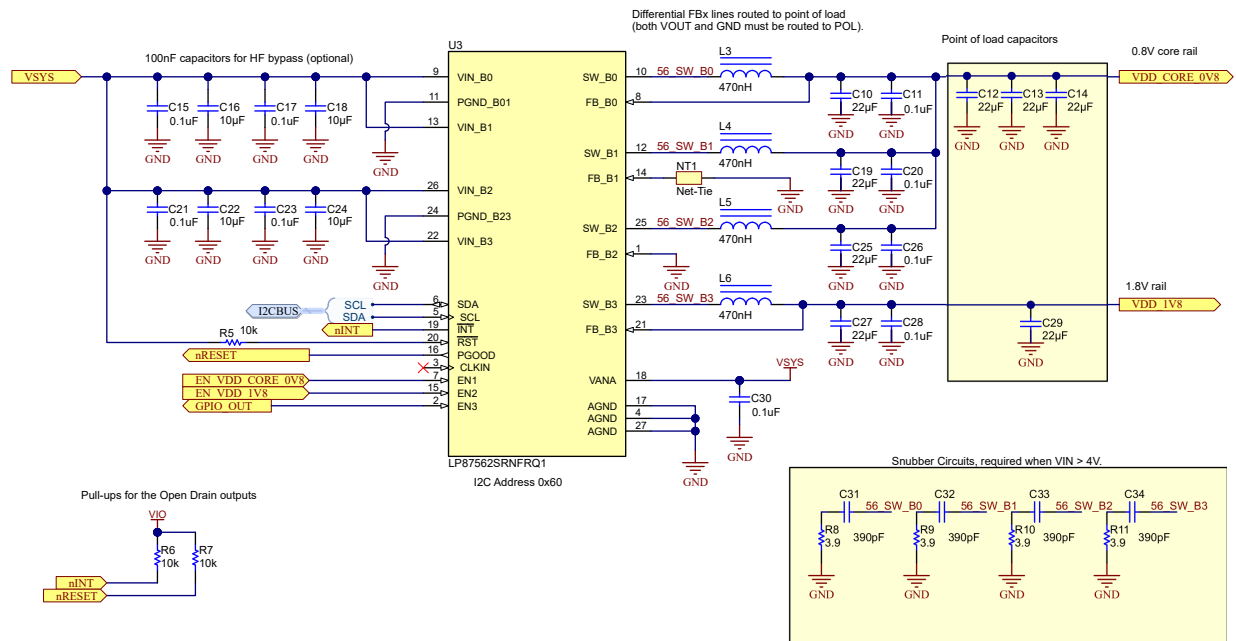
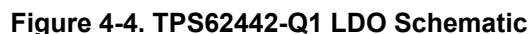
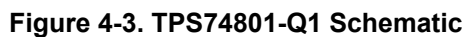


Figure 4-2. LP87562S-Q1 Schematic



Linux drivers for the LP875x are available in public git repository. These can be used to help integrate the LP87562S-Q1 control to system software:

LP8756x

- <https://github.com/torvalds/linux/blob/master/drivers/mfd/lp87565.c>
- <https://github.com/torvalds/linux/blob/master/drivers/regulator/lp87565-regulator.c>
- <https://github.com/torvalds/linux/blob/master/drivers/gpio/gpio-lp87565.c>

Note: Every header file is in the *include* folder starting from the root directory. So once in *include* folder, the user can navigate to the relevant header file. For example, the LP87565.h file: <https://github.com/torvalds/linux/blob/master/include/linux/mfd/lp87565.h>.

6 Recommended External Components

Table 6-1 shows the recommended external components to use in this solution with the LP87562S-Q1, TPS74801-Q1, and TPS62442-Q1. It also shows the total solution size, including the PMIC device and the external components.

Table 6-1. Bill of Materials

COUNT	VENDOR	PART NUMBER	SYSTEM COMPONENT	W (mm)	L (mm)	H (mm)	UNIT AREA ⁽¹⁾	TOTAL BOARD AREA ⁽¹⁾
1	TI	LP87562S-Q1	Configurable 4-phase Buck	4.00	4.50	0.90	27.50	27.50
4	Murata	DFE252012PD-R47M	LP875x Inductor 0.47 uH, I _{max} 4.0 A, R _{dc} typ 21mOhm	2.50	2.00	1.20	10.50	42.00
4	Murata	GCM21BR71A106KE22	LP875x SMPS Input Capacitor 10 uF, 10 V, 10%	2.00	1.25	1.25	6.75	27.00
8	Murata	GCM21BD70J226ME35	LP875x SMPS Output Capacitor 22 uF, 10 V, 10%	2.00	1.25	1.25	6.75	54.00
1	Murata	GCM155R71C104KA55D	LP875x Input Capacitor 0.1 uF, 16 V, 10%	1.00	0.50	0.50	3.00	3.00
4	TDK	CGA2B2C0G1H391J050BA	LP875x Snubber capacitor, 390 pF	1.00	0.50	0.50	3.00	12.00
4	Vishay-Dale	CRCW04023R90JNED	LP875x Snubber resistor, 3R9	1.00	0.50	0.50	3.00	12.00
1	TI	TPS62442-Q1	Dual buck 2 A buck	2.30	2.70	0.90	12.21	12.21
2	Murata	DFE252012PD-R47M	Inductor 0.47 uH, I _{max} 4.0 A, R _{dc} typ 21 mOhm	2.50	2.00	1.20	10.50	21.00
2	TDK	CGA4J3X7R1C475K125AE	Input Capacitor 4.7 uF, 10 V, 10%	2.00	1.25	1.25	6.75	13.50
2	Murata	GCM21BD70J226ME35	Output Capacitor 22 uF, 10 V, 10%	2.00	1.25	1.25	6.75	13.50
2	Murata	GRM155C1H100JA01D	Feedforward Capacitor, 10 pF, 50 V	1.00	0.50	0.50	3.00	6.00
4			Set resistors	1.00	0.50	0.50	3.00	12.00
1	TI	TPS74801-Q1	Low Dropout Regulator	3.00	3.00	1.00	16.00	16.00
2	Murata	GCM188R71C105KA64D	Input Capacitor 1 uF	1.00	0.50	0.50	3.00	6.00
1	Murata	GRT155C71A225KE13	Output Capacitor 2.2 uF, 6.3 V, 10%	1.00	0.50	0.50	3.00	3.00
TOTAL								280.71 mm ²
Routing area calculated with 0.3 routing factor								120.30 mm ²
Total area								401.01 mm ²

(1) Assuming 1 mm keep-out around each component, and multiplying by component count

7 Measurements

Test data can be found in the Application Curves section of the following data sheets:

- [LP8756x-Q1 16A Buck Converter With Integrated Switches](#) data sheet.
- [1.5 A Low-Dropout Linear Regulator with Programmable Soft-Start](#) data sheet.
- [TPS6244x-Q1 2.75-V to 6-V Dual Step-Down Converter with Adjustable Frequency in a QFN Package](#) data sheet.

TI PMIC Efficiency Estimation Tool (PEET) can also be used for calculating efficiency and thermal performance: [PEET-GUI](#).

8 Summary

With this presented solution with the LP87562S-Q1, TPS74801-Q1, and TPS62442-Q1 ICs, it is possible to meet power requirements for Horizon Robotics Journey 3 SoC while maintaining good efficiency. Solution is compact due to minimum number of external components. I²C control allows diagnostic and control for the LP87562S-Q1.

9 References

See these references for additional information:

1. Texas Instruments, [LP8756x-Q1 16A Buck Converter With Integrated Switches](#) data sheet.
2. Texas Instruments, [LP87562S-Q1 Technical Reference Manual](#).
3. Texas Instruments, [1.5 A Low-Dropout Linear Regulator with Programmable Soft-Start](#).
4. Texas Instruments, [TPS6244x-Q1 2.75-V to 6-V Dual Step-Down Converter with Adjustable Frequency in a QFN Package](#).

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