

Answers to Common Sigma-Delta ADC Questions on MSP MCUs



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ABSTRACT

Sigma-Delta (also referred to as Delta-Sigma) analog-to-digital converters (ADCs) are typically used in analog sensing and measurement applications where a high resolution is preferred over a fast sampling frequency. However, these ADCs are not as well-known as successive approximation register (SAR) ADCs, so designers may face more challenges using them. While TI offers various discrete ADCs, several MSP430™ microcontrollers (MCUs) feature integrated Sigma-Delta ADCs. This application report demystifies these Sigma-Delta ADCs by briefly explaining how they work in real-world applications, comparing their key features and addressing common challenges. To learn more about these ADCs in general, watch the [Designing with Delta-Sigma ADCs training series](#). For more information, see the device-specific data sheet and user's guide.

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1 Introduction: MSP Sigma-Delta ADCs and Common Applications

Several MSP430™ MCU families such as MSP430AFE2xx, MSP430F67xxA and MSP430i20xx feature integrated 24-bit Sigma-Delta (SD) ADC modules whereas other legacy families such as MSP430F42x, MSP430F47x and MSP430F20x3 feature 16-bit SD ADC modules with lower performance and fewer features. This document focuses mainly on the devices with 24-bit SD ADC modules, but it can also be used as a reference for the legacy devices.

Compared to a discrete solution, these MSP430 MCUs enable high-accuracy applications such as passive infrared (PIR) motion detectors with single sensors or small arrays, infrared (IR) thermometers, revenue-grade electricity meters and solar inverters by combining high-performance analog with digital modules as a system-on-chip (SoC) solution that requires fewer external components and less board space.

2 MSP Sigma-Delta ADC Portfolio

Table 2-1 compares the key features of the SD ADC modules available on MSP430 MCUs.

Table 2-1. MSP Sigma-Delta ADC Feature Comparison

Parameter	SD16	SD16_A	CTSD16	SD24_A	SD24_B	SD24	SDHS
MSP430 device families	F(E)42x(A)	F20x3 F(G)42x0 F(G)47x F47(1)xx	FG6x2x	AFE2xx	F67xx(1)(A)	i20xx	FR50xx FR60xx
Number of independent ADCs (referred to as channels) ⁽¹⁾	1, 3	1, 3, 4, 6, 7	1	1, 2, 3	2, 3, 4, 6, 7	2, 3, 4	1
Modulator frequency range	0.5 to 1 MHz	0.03 to 1.1 MHz	1.024 MHz	0.03 to 1.1 MHz	0.03 to 2.3 MHz	1.024 MHz	68 to 80 MHz
Oversampling rate (OSR) range	32 to 256	32 to 1024	32 to 256	32 to 1024	1 to 1024	32 to 256	10 to 160
Maximum ADC sampling frequency (data rate)	31.25 kHz	34.375 kHz	32 kHz	34.375 kHz	2.3 MHz ⁽²⁾	32 kHz	8 MHz
Maximum full-scale range (FSR)	±500 mV	±500 mV	±928 mV	±500 mV	±930 mV	±928 mV	±500 mV
Programmable gain amplifier (PGA) range	1 to 32	1 to 32	1 to 16	1 to 32	1 to 128	1 to 16	0.5 to 34.5
Internal short for PGA offset measurement	YES	YES	YES	YES	YES	NO	NO
Integrated buffer(s)	NO	YES ⁽³⁾	YES	NO	NO	NO	NO
Grouped ADC channels	YES	YES ⁽³⁾	YES	YES	YES	YES	NO
Synchronization with external modules (for example, SAR ADC)	NO	NO	NO	NO	YES	NO	NO
Modulator order	Second-order	Second-order	Second-order	Second-order	Second-order	Second-order	Third-order
Type of digital filter(s)	SINC ³	SINC ³	SINC ³	SINC ³	SINC ³	SINC ³	CIC ⁷ (stage 1) CIC ¹ (stage 2)

Table 2-1. MSP Sigma-Delta ADC Feature Comparison (continued)

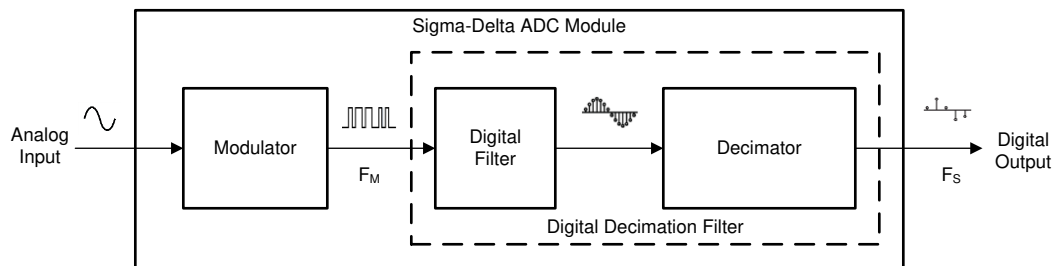
Parameter	SD16	SD16_A	CTSD16	SD24_A	SD24_B	SD24	SDHS
Architecture	Discrete-Time	Discrete-Time	Continuous-Time	Discrete-Time	Discrete-Time	Continuous-Time	Discrete-Time

- (1) Number of ADC channels is device dependent.
- (2) This sampling frequency is a theoretical maximum and will probably not generate meaningful results.
- (3) Not implemented on all devices. For more information, see the device-specific data sheet.

3 Sigma-Delta ADC Overview

Analog-to-digital converters do just that: they convert real-world signals into an abstract representation for digital processing. There are several different ADC architectures including slope, pipeline, SAR and SD. Each architecture has its advantages and disadvantages. For example, SAR ADCs typically support higher throughput but lower resolution than SD ADCs. Also, SD ADCs support negative input voltages whereas most SAR ADCs do not. While this application report focuses on SD ADCs, watch [Part 1](#) of the [Choosing the Best ADC Architecture for Your Application training series](#) to learn more about different ADC architectures.

A typical Sigma-Delta (also referred to as Delta-Sigma) ADC is shown in [Figure 3-1](#) and includes two main components: the modulator and the decimation filter. At a high level, the modulator functions as the analog front end that samples the analog input signal and then converts it into a modulated digital bit stream which gets fed into the decimation filter. The decimation filter includes a digital filter that converts the bit stream into an oversampled digital representation of the analog signal and a decimator that undersamples that result to produce the digital output.

**Figure 3-1. Typical Sigma-Delta ADC Block Diagram**

To learn more about how SD ADCs work, watch [Part 3](#) and [Part 4](#) of the [Choosing the Best ADC Architecture for Your Application training series](#). Also, see the device-specific data sheet and user's guide.

4 MSP Sigma-Delta ADC Features

4.1 ADC Inputs: Differential or Single-Ended

A differential input measures the voltage difference between a positive pin and a negative pin whereas a single-ended input measures the voltage difference between a positive pin and ground. SD ADCs and some SAR ADCs feature differential inputs, but most SAR ADCs feature single-ended inputs. The main advantage of differential inputs is the removal of common-mode noise - if the noise is present on each input, the voltage difference is just the signal without the noise. Differential inputs can be used as single-ended inputs, but the dynamic range is halved.

4.2 Input Channels: Independent or Multiplexed

Depending on the device, the SD16, CTSD16 and SDHS modules in [Table 2-1](#) feature a single ADC channel with multiplexed inputs. These modules may fit most applications, but each input is measured sequentially, not simultaneously. Switching between inputs may cause synchronization issues and also noise if the decimation filter still contains samples from the previous input. However, the other SD ADC modules in [Table 2-1](#) support simultaneous sampling across their independent ADC channels.

4.3 Integrated Buffers

Depending on the device, the SD16_A and CTSD16 modules in [Table 2-1](#) feature integrated buffers. In applications that require high-impedance external circuits (for example, high-order passive filters), these buffers help prevent the external circuit from impacting the ADC's minimum settling time.

4.4 Integrated PGAs

The SD ADC modules in [Table 2-1](#) feature integrated PGAs with various ranges. The PGAs amplify low-amplitude signals without requiring external op-amps. Note that the FSR decreases as the PGA gain setting increases for each channel.

4.5 Offset Calibration: Internal or External

The SD ADC modules in [Table 2-1](#) except SD24 and SDHS include a feature that simplifies the PGA offset calibration. Rather than shorting the ADC inputs together externally, an internal short can be enabled via software to easily measure this offset, even if an external circuit is connected. After calibration, the positive or negative offset would be manually subtracted to or added from the digital output, respectively.

4.6 Voltage Reference: Internal or External

The SD ADC modules in [Table 2-1](#) all support internal or external voltage references. To learn more about the supported voltage ranges, see the device-specific data sheet.

4.7 ADC Modulator Clock Frequency: Fixed or Adjustable

The CTSD16 and SD24 modules in [Table 2-1](#) feature fixed-frequency modulator clocks whereas the other modules feature adjustable modulator clocks that support a wider range of sampling frequencies. Adjustable modulator clocks can help enable applications that may require a specific sampling frequency or coherent sampling; a scenario where the sampling frequency tracks the frequency of the input signal to ensure a fixed number of samples per input cycle for post-processing.

4.8 Sampling Rate versus Data Rate

The SD ADC modules in [Table 2-1](#) feature different OSR ranges and resolutions. The oversampling rate (OSR) is the decimation ratio of the sampling rate of the analog input signal to the data rate of the digital output. In MSP documentation (including data sheets and user's guides), the sampling rate is commonly referred to as the modulation frequency and the data rate is commonly referred to as the sampling frequency.

4.9 Conversion Mode: Single or Continuous

The SD ADC modules in [Table 2-1](#) all support either single or continuous conversions. Single conversions are helpful for applications that require lower sampling frequencies, but each conversion must be triggered manually by setting a register bit in software or using a timer. Continuous conversions are started manually but then

triggered automatically. This approach is simpler plus more CPU bandwidth is available to perform other tasks because CPU intervention is not required for the trigger.

4.10 Groups of ADC Channels

The SD ADC modules in [Table 2-1](#) with more than one channel support groups of channels. There can be multiple groups with different sampling modes. Groups are helpful for synchronization across multiple channels.

4.11 Preload

Preload represents a fractional-sample delay between ADC conversions. When the preload value for each channel is applied, the next ADC conversion is delayed by a specific number of modulator clock cycles that can range from zero (no delay) to OSR minus one (nearly a whole-sample delay). Also, the delay is cumulative - the initial preload value and any subsequent preload values add up creating a total delay. When that value exceeds OSR minus one, the total delay rolls over. Whole-sample delays must be implemented in software. For a group of channels that are started simultaneously, the preload for each channel can be adjusted independently to align periodic (AC) signals. However, it is easier to stop the conversions, update the preload values and then restart the conversions rather than tracking the preload applied to each channel. Note that preload is not necessary for aperiodic (DC) signals. For more details about how to use preload, see the device-specific user's guide.

4.12 Output Format: Unipolar or Bipolar Data

The SD16_A and SD24_A modules in [Table 2-1](#) support unipolar and bipolar formats whereas the other SD ADC modules only support bipolar formats. Unipolar format ignores negative input signals, but bipolar format supports both positive and negative inputs. Two bipolar formats are offset binary (output values range from zero to FSR) and two's complement (output values range from -FSR to +FSR).

4.13 Module Synchronization

The SD24_B module in [Table 2-1](#) features a trigger generator that behaves like another channel but triggers other modules like the SAR ADC to synchronize the ADC conversions.

4.14 Architecture: Discrete-Time versus Continuous-Time

The CTSD16 and SD24 modules feature a continuous-time architecture, whereas, the other modules feature a discrete-time architecture. The main difference between these architectures is where the input signal is sampled. Discrete-time SD ADC modules sample the input signal using a switched-capacitor input stage. Continuous-time SD ADC modules sample the input signal near the modulator output. To learn more about these architectures, see the [Continuous-Time Sigma-Delta ADCs](#).

5 Solutions to Common MSP Sigma-Delta ADC Configuration Issues

Designers may not be as familiar with the SD ADC modules, so they may encounter issues such as higher-than-expected noise or lower-than-expected performance during the evaluation, development or even production stages of their designs. This section is intended to be a guide for quickly resolving common SD ADC configuration issues.

5.1 ADC Input Configuration

5.1.1 Settling Time Exceeds Recommended Minimum

For discrete-time SD ADC modules without integrated buffers, the source resistance of the external circuitry, the sampling capacitance (typically varies with the PGA gain setting) and the specified modulation frequency all impact the ADC settling time due to the switched-capacitor input stage. Figure 5-1 shows an analog equivalent circuit for the input stage of the SD24_B module and can be found in the *Analog Input Characteristics* section in the *MSP430x5xx and MSP430x6xx Family User's Guide*.

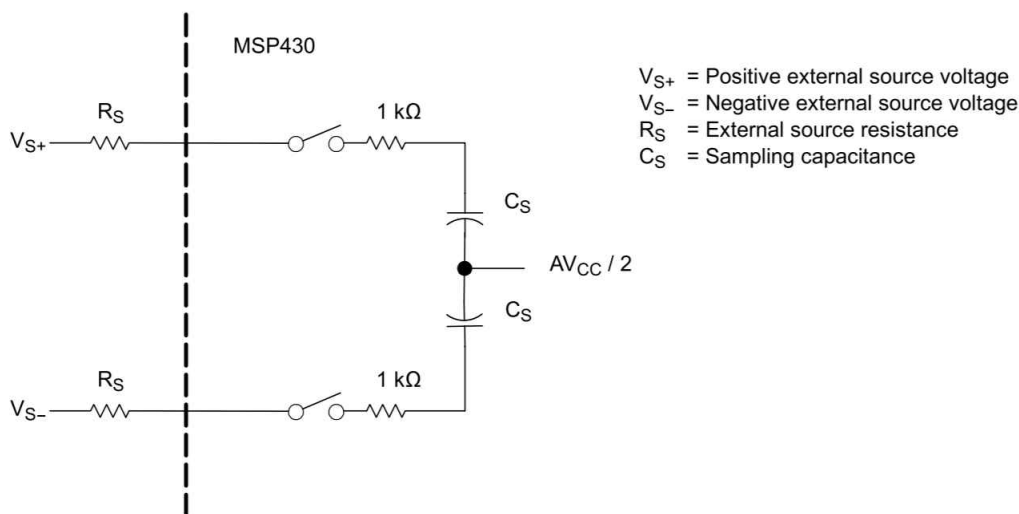


Figure 5-1. Analog Input Equivalent Circuit Example

If the actual settling time exceeds the minimum settling time for the specified modulation frequency, you may observe more noise in the digital output because the input signal does not settle completely before the next sample. The equations to calculate the minimum settling time can be found in the device-specific user's guide. For example, the minimum settling time equations for the SD24_B module are shown in Equation 1 and Equation 2 and can be found in the *Analog Input Characteristics* section in the *MSP430x5xx and MSP430x6xx Family User's Guide*.

$$t_{\text{Settling}} \geq (R_S + 1 \text{ k}\Omega) \times C_S \times \ln\left(\frac{\text{Gain} \times 2^{17} \times V_{Ax}}{V_{\text{REF}}}\right) \quad (1)$$

where

$$f_M = \left(\frac{1}{2 \times t_{\text{settling}}}\right) \text{ and } V_{Ax} = \max\left(\left|\frac{AV_{CC}}{2} - V_{S+}\right|, \left|\frac{AV_{CC}}{2} - V_{S-}\right|\right) \quad (2)$$

The resistance of the external circuit is called source resistance in MSP documentation. However, the external circuit in most designs will probably include a network of resistors, capacitors and inductors. This can cause the source resistance to vary significantly across different input frequencies, so it is referred to as source impedance in this application report.

Lowering the source impedance of the external circuitry is a change that can reduce the settling time, but this may not be feasible (for example, the design is already in production). Ideally, the impact of the external circuit on the settling time is understood during initial development. TINA-TI™ can be used to simulate the external circuit and calculate the maximum source impedance.

Lowering the sampling capacitance (reducing the PGA gain setting) is another change that can reduce the settling time, but this may not be feasible either (for example, the amplitude of the input signal is small). The sampling capacitors represent impedance because they are not purely resistive.

Lowering the modulation frequency (remember that this is the actual sampling rate of the analog signal) would be the easiest change to reduce the settling time, but this would also lower the sampling frequency (data rate).

For continuous-time SD ADC modules such as CTSD16 and SD24, the architecture does not feature a switched-capacitor input stage, so the minimum settling time does not apply. However, this does not imply that the source impedance can be infinite.

5.1.2 Amplitude of the Input Signal Exceeds FSR

The FSR is the maximum recommended amplitude of the input signal. It depends on the specified PGA gain and reference voltage settings and varies across the different SD ADC modules. Exceeding FSR can drastically increase noise in the digital output because the PGAs become saturated. When using the internal voltage reference, the FSR values are provided in the device-specific data sheet for various PGA gain settings. If you're using an external voltage reference instead, the device-specific data sheet also includes an equation to recalculate the FSR values.

Ideally, the maximum amplitude of the input signal should be slightly less than FSR for the minimum PGA gain allowed by your application. There are two reasons for this approach: 1) the signal-to-noise plus distortion (SINAD) performance increases as the amplitude of the input signal approaches FSR, and 2) the SINAD performance decreases as the PGA gain increases. However, some applications may require sensors that output low-amplitude signals which would require a high PGA gain. For example, in some metering applications, low-resistance shunts measure current but output low-amplitude signals, so a high PGA gain would be required.

For root-mean-square (RMS) inputs, make sure you convert from RMS to peak amplitudes before comparing them to the peak values in the device-specific data sheet. Equation 3 shows how to convert sinusoidal RMS amplitudes to peak, but other waveforms may use a different formula.

$$V_{\text{Peak}} = \sqrt{2} \times V_{\text{RMS}} \quad (3)$$

5.1.3 Missing Anti-Aliasing Filters

The frequency content of the input signal can repeat itself around multiples of the ADC sampling rate - the duplicates are aliases of the original signal. If the anti-aliasing filters are missing, these aliases can increase noise in the digital output because their frequency exceeds the Nyquist rate. Remember that the sampling rate is actually the modulation frequency, so the recommended cut-off frequency of the anti-aliasing filters is typically 100 times less than the modulation frequency. Typically, the anti-aliasing filters are implemented using external first- or second-order resistor-capacitor (RC) filters that are connected to each differential input. [Figure 5-2](#) shows how anti-aliasing filters are connected to the differential ADC inputs in a PIR motion detector design. To learn more, watch the [Aliasing and Anti-Aliasing Filters training video](#).

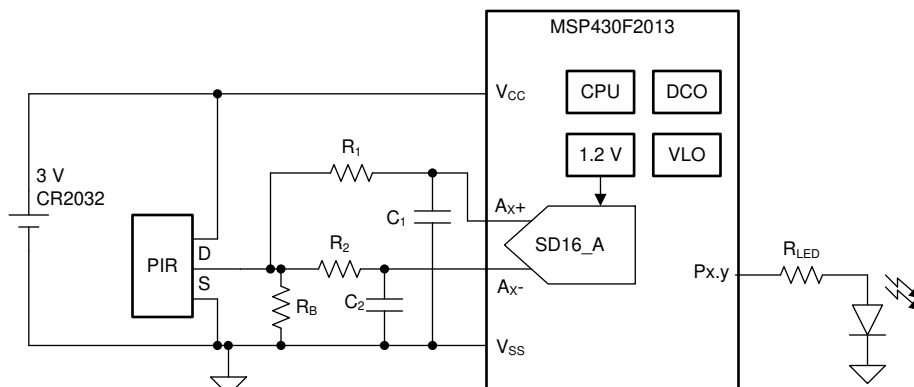


Figure 5-2. Anti-Aliasing Filters Example

5.2 ADC Clocking Configuration

5.2.1 Incorrect Sampling Frequency

If you think the sampling frequency is incorrect, make sure you are measuring the sampling frequency accurately. The most common method includes toggling a general-purpose input/output (GPIO) at the beginning and end of the SD ADC interrupt service routine (ISR) and measuring the frequency of the GPIO pulses with a logic analyzer or oscilloscope. Remember that the sampling frequency is equivalent to the data rate of the digital output. In MSP documentation, the modulator clock is referred to as F_{SD} or F_M and the sampling frequency is referred to as F_S . As shown in [Equation 4](#), the sampling frequency is determined by the ratio of modulation frequency (sampling rate) to OSR. For example, if the modulation frequency is 1.024 MHz and the OSR is 256, then the sampling frequency (data rate) is 4 kHz.

$$F_S = \frac{F_M}{OSR} \quad (4)$$

If the sampling frequency is incorrect, check that the modulator clock settings such as the clock source, dividers and mode are correct for each channel. Next, check the OSR settings. For the MSP430i20xx devices, make sure to include the startup code that calibrates the REF, DCO and SD ADC modules. Otherwise, the sampling frequency may not be correct.

Also, check the interrupt delay settings for the decimation filter of each channel. If you forget about this delay, you may think that the sampling frequency is incorrect when it's not. The interrupt delay allows the decimation filter to settle (or fill up) before triggering the first SD ADC interrupt request, and it can be up to seven conversions depending on the module. In single sampling mode, the delay occurs after each conversion is started. In continuous sampling mode, the delay occurs after the first conversion is started but not after subsequent conversions since the decimation filter has already settled. If the input signal changes drastically and the filter has not settled properly, the digital output may be invalid.

5.3 ADC Results

5.3.1 Unexpected Output Data Format

If the format of the digital output is unexpected, check the format settings for each channel. The format options and register settings can be found in the device-specific user's guide. For example, see the *Output Data Format* section in the *MSP430i2xx Family User's Guide* for the SD24 module.

5.3.2 Low Resolution

If you're using the SD24_A, SD24_B and SD24 modules, perhaps you're only seeing 16-bit digital outputs rather than 24-bit. Each module handles the digital output from the decimation filter differently. The SD24_B module features two independent result registers for the upper and lower conversion results. The SD24_A and SD24 modules feature a single result register that must be toggled to read the complete digital output. For all of these modules, those results must be combined manually. In general, the total number of bits output by the decimation filter depends on the OSR setting for each channel, and the mapping of the digital output to the result registers depends on the alignment setting.

5.3.3 Data Interpretation

The digital output represents the input signal within +/-FSR (depending on the format). However, the output will probably be converted into a real-world value with understandable units such as degrees or amps. Typically, this process includes applying a known input signal representing a known condition (for example, 25°C), then multiplying the related digital output with a scaling factor and then adding or subtracting an offset if necessary. The scaling factor can also help avoid using decimals in the final results (for example, 2500°C for 25.00°C). The offset may include both the unit conversion offset and the PGA offset.

5.4 Reference Module (REF) Configuration

5.4.1 Choosing Between an Internal or External Reference

Remember that the SD ADC modules all support internal or external voltage references. Typically, the internal reference will meet the accuracy requirements for most applications, so an external reference would not be needed. That frees up board space, simplifies the board layout and lowers the overall system cost. However, external references usually offer better accuracy and flexible voltage options that can support differential input signals with slightly larger amplitudes.

5.4.2 Connecting the Recommended Capacitors

The recommended capacitors depend on whether the internal reference or an external reference is used. Some capacitors act as a buffer while others filter out noise. The device-specific data sheet and user's guide describe what capacitors should be connected to various pins and what capacitance they should be. Excessive noise or other unintended behaviors may occur if these capacitors are not connected properly.

5.4.3 Delaying Conversions Until the Reference Settles

After turning on the internal or external reference, make sure to start the conversions after the reference has settled completely. Otherwise, the reference may not stabilize which could introduce noise in the digital output. The reference can be left on continuously or manually toggled off and on between conversions to save power. Some modules such as the SD24_B automatically power down the internal reference between conversions. The device-specific data sheet should specify the reference turn-on or settling time. The reference voltage can be measured externally using an oscilloscope during start up or during conversions to detect instability. Note that the oscilloscope probe may impact the capacitance observed on the reference pin and affect the conversions.

5.5 Hardware Recommendations

- Follow all recommendations in the device-specific data sheet for unused pins, required external connections (VDSYS, VASYS) and capacitor values (CVCORE, CVREF)
- Follow grounding and noise considerations in the device-specific user's guide for the ADC and REF modules
- Place a 0-Ω resistor between AVCC and DVCC in case you need to filter out digital noise later by adding a different resistor (for example, 10-Ω)
- Add 0.1 μF decoupling capacitors in parallel with the recommended CDVCC and CAVCC capacitors, and keep them close to the device to filter out more noise
- Route symmetrical PCB traces for ADC inputs to help match trace lengths and impedances

6 Frequently Asked Questions

How do I calculate the effective number of bits (ENOB)?

For AC inputs, the ENOB can be calculated using [Equation 5](#) and the SINAD values provided in the device-specific data sheet. For DC inputs, the ENOB equivalent is called the effective resolution and is not provided in the data sheet. The effective resolution can be calculated using the standard deviation from several samples of a known DC input. Other important performance parameters for DC inputs include integral nonlinearity (INL) and differential nonlinearity (DNL). For more details about the effective resolution, see the [A bone of contention: ENOB or effective resolution? blog](#).

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02} \quad (5)$$

Why can't I find the Sigma-Delta ADC sampling frequency in the data sheet?

The sampling frequency is typically not provided because it depends on the modulator frequency and the OSR. For some SD ADC modules, the modulator frequency and OSR are adjustable, so a pair of modulator frequency and OSR combinations can result in the same sampling frequency with different performance.

Can I use the differential ADC inputs as a single-ended ADC input?

Yes, but remember that this configuration halves the dynamic range. To learn more about dynamic range, see [A Glossary of Analog-to-Digital Specifications and Performance Characteristics](#).

What's the difference between common-mode and differential input voltages?

Common-mode means the same voltage is applied to both the positive and negative ADC pins. In this case, the differential voltage would be zero (ignoring any noise or offsets) because there's no voltage difference between the pins. Common-mode and differential inputs can be applied simultaneously. For example, a DC bias could be applied to both pins while an AC signal is applied between the pins. See the device-specific data sheet for the absolute maximum ratings.

What type of decimation filter is used?

The SD ADC modules in [Table 2-1](#) except SDHS feature second-order modulators and third-order (SINC³) decimation filters (also referred to as comb filters due to the shape of their frequency response). The SDHS module features a third-order modulator and multi-stage CIC decimation filters. To learn more about decimation filters, see [Digital Filter Types in Delta-Sigma ADCs](#) and the device-specific user's guide.

What does the frequency response of the decimation filter in the user's guide tell me?

The frequency response in the device-specific user's guide illustrates the level of attenuation at various input frequencies. Notches attenuate the input signal completely and occur at multiples of the sampling frequency (data rate). Typically, the minimum sampling frequency is based on the Nyquist rate, but a higher sampling frequency can be used to shift the first notch and reduce the roll-off attenuation of the input signal. Increasing the sampling frequency may reduce performance due to a lower OSR and will capture more harmonic content which may be desirable or not depending on the application. To learn more about roll-off attenuation, read the [Quantifying harmonic distortion - Effect of sinc3 filter roll off blog](#).

If you decide to use a discrete ADC in your design, remember that some ADCs feature decimation filters with notches at 50 or 60 Hz to intentionally filter out noise from power supplies sourced by AC mains, so those ADCs should not be used in metering applications to measure AC power or energy.

Can I use external modulators with the internal decimation filters?

Yes, the SD24_B module supports external modulators. To learn more about this configuration, see the [Multi-phase Energy Measurement with Isolated Shunt Sensors Reference Design \(TIDA-00601\)](#).

7 References

- Texas Instruments: [Measuring Single-Ended 0- to 5-V Signals With Differential Delta-Sigma ADCs](#)
- Texas Instruments: [How delta-sigma ADCs work, Part 1](#)
- Texas Instruments: [MSP430F677xA, MSP430F676xA, MSP430F674xA Polyphase Metering SoCs Data Sheet](#)
- Texas Instruments: [Ultra-Low-Power Motion Detection Using the MSP430F2013](#)
- Texas Instruments: [A Glossary of Analog-to-Digital Specifications and Performance Characteristics](#)
- Texas Instruments: [MSP430i2xx Family User's Guide](#)
- Texas Instruments: [MSP430x2xx Family User's Guide](#)
- Texas Instruments: [MSP430x4xx Family User's Guide](#)
- Texas Instruments: [MSP430x5xx and MSP430x6xx Family User's Guide](#)
- Texas Instruments: [Continuous-Time Sigma-Delta ADCs](#)
- [Aliasing in ADCs: Not all signals are what they appear to be](#)
- [Designing with Delta-Sigma ADCs: System design considerations to optimize performance](#)
- [Understanding Sampling rate vs Data rate](#)
- [What's The Difference Between Continuous-Time And Discrete-Time Delta-Sigma ADCs?](#)

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