Application Report
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Code Porting From MSP430FR2000 to MSP430FR2311 MCUs

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ABSTRACT

This guide is intended to help developers who are interested in testing code written for the MSP430FR2000 MCU by loading it onto the MSP430FR2311 MCU. Running the code on the MSP430FR2311 LaunchPad™ Development Kit may help to reduce test costs, because the LaunchPad development kit with built-in eZ-FET emulation is less expensive than purchasing the MSP-TS430PW20 Target Development Board and MSP-FET Flash Emulation Tool.

Key differences between the two MCUs are outlined in this guide. These differences may require a change in code when porting from the MSP430FR2000 MCU to the MSP430FR2311 MCU.

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Trademarks

1 GPIO Multiplexing

1.1 eUSCI_A0 UART and SPI Communication

If the MSP430FR2000 code configures P1.0, P1.1, P1.2, or P1.3 for UART or SPI communication, the code must be changed to instead use P1.4, P1.5, P1.6, or P1.7, respectively (see Figure 1). This is achieved by removing SYSCFG3 code and changing the selection bits.

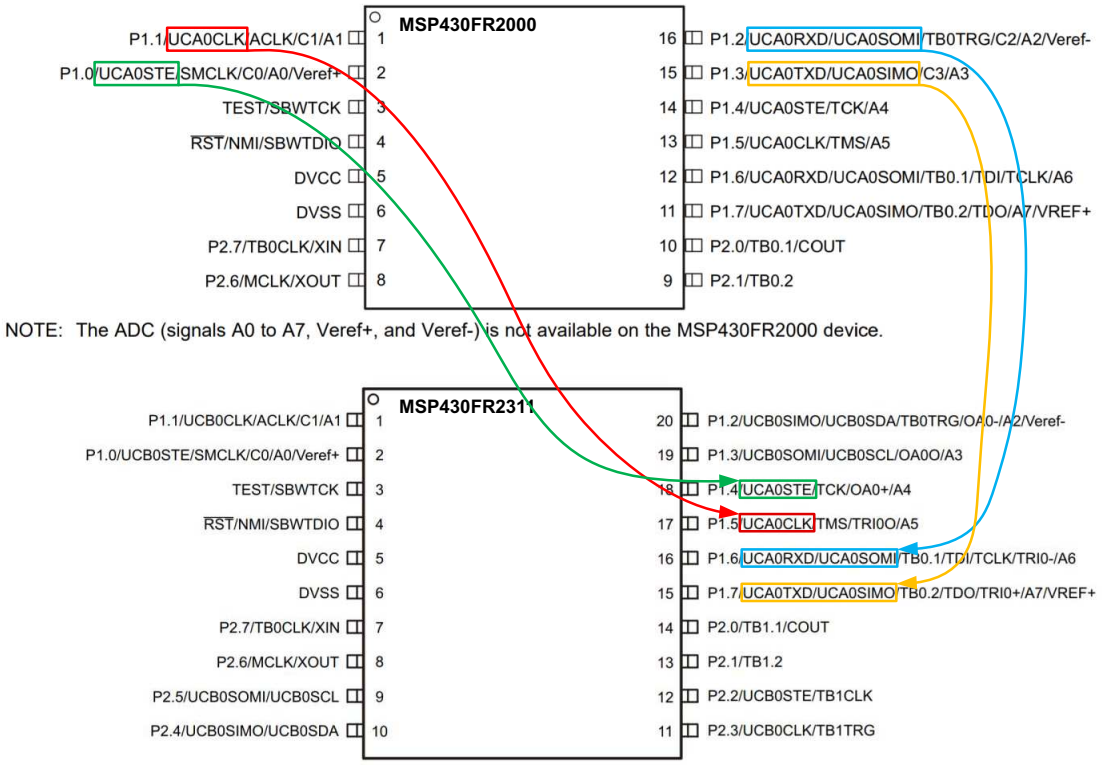

Figure 1. UART and SPI Signals

MSP430FR2000		MSP430FR2311
All Serial Communication		
`SYSCFG3 |= USCIARMP_1;`	→	`//SYSCFG3 |= USCIARMP_1;`
UART		
`P1SEL0 |= BIT2 | BIT3;`	→	`P1SEL0 |= BIT6 | BIT7;`
3-Wire SPI		
`P1SEL0 |= BIT1 | BIT2 | BIT3;`	→	`P1SEL0 |= BIT5 | BIT6 | BIT7;`
4-Wire SPI		
`P1SEL0 |= BIT0 | BIT1 | BIT2 | BIT3;`	→	`P1SEL0 |= BIT4 | BIT5 | BIT6 | BIT7;`

See Chapter 21 and Chapter 22 of the MSP430FR4xx and MSP430FR2xx Family User's Guide for more details about the Enhanced Universal Serial Communication Interface (eUSCI) UART and SPI modes.

1.2 Timer0_B3

If the MSP430FR2000 code sets Timer0_B3 to use the capture input functionality on P2.0 or P2.1 (CCIS in TB0CCTL0 is set to 00b or 01b and TBRMP in SYSCFG3 is set to 1), the input pins must be changed to P1.6 or P1.7.

Additionally, if the MSP430FR2000 code sets Timer0_B3 to output a PWM on P2.0 or P2.1 (P2.0 or P2.1 set to output and P2SEL set to 01b), the outputs must be changed to P1.6 or P1.7.

Alternatively, to keep P2.0 and P2.1 as GPIOs when using the MSP430FR2311, the code can be changed to use Timer1_B3 instead of Timer0_B3 (see Figure 2). This involves changing the register assignments from those for Timer0_B3 to Timer1_B3. In most cases, it is sufficient to perform a find and replace search of "TB0" to "TB1" and to update the interrupt service routine, if present.

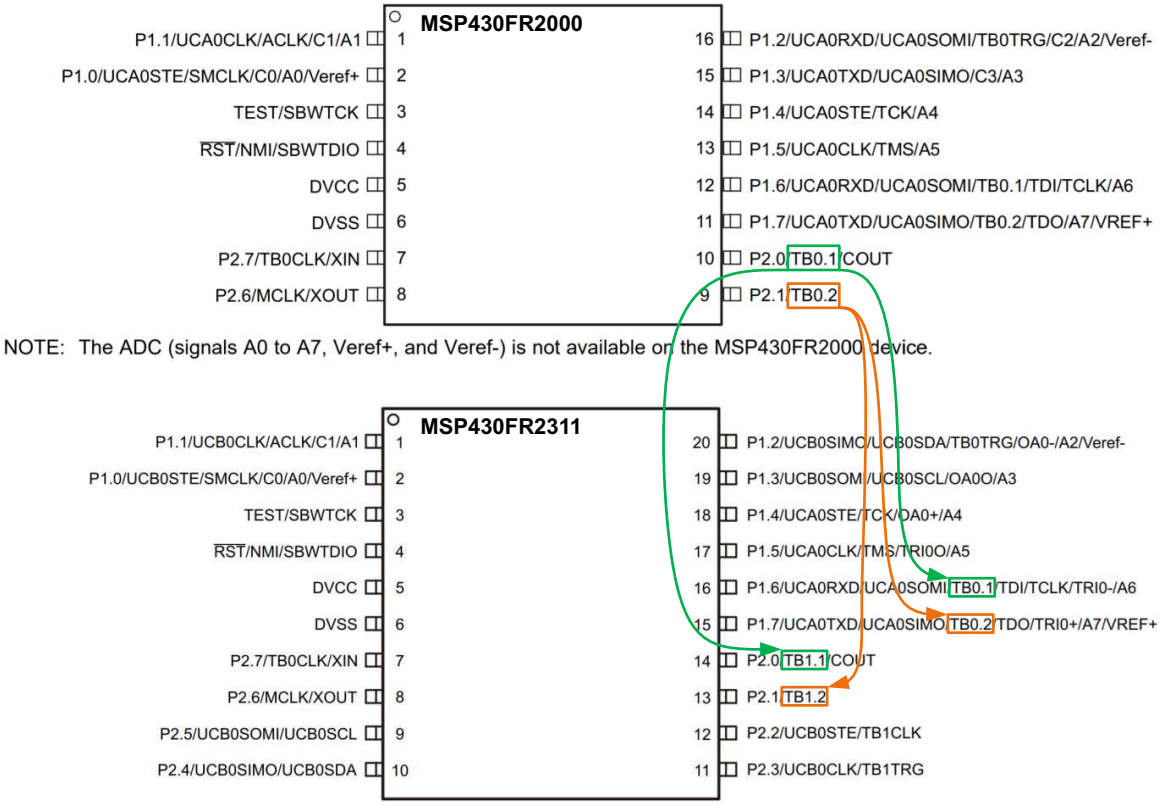

Figure 2. Timer0_B3 Signals

The following comparison summarizes how to update the code to change from using P2.0 and P2.1 to P1.6 and P1.7.

MSP430FR2000		MSP430FR2311
P2.0 set to TB0.CCI1A		**P1.6 set to TB0.CCI1A**

`SYSCFG3 |= TBRMP_1;`
`TB0CCTL0 |= CCIS_0;`
`P2DIR &= ~BIT0`
`P2SEL0 |= BIT0;`
	→	`//SYSCFG3 |= TBRMP_1;`
		`TB0CCTL0 |= CCIS_0;`
		`P1DIR &= ~BIT6`
		`P1SEL1 |= BIT6;`

P2.1 set to TB0.CCI2A		**P1.7 set to TB0.CCI2A**

`SYSCFG3 |= TBRMP_1;`
`TB0CCTL0 |= CCIS_1;`
`P2DIR &= ~BIT1`
`P2SEL0 |= BIT1;`
	→	`//SYSCFG3 |= TBRMP_1;`
		`TB0CCTL0 |= CCIS_1;`
		`P1DIR &= ~BIT7`
		`P1SEL1 |= BIT7;`

P2.0 set to TB0.1		**P1.6 set to TB0.1**
`P2DIR |= BIT0;` `P2SEL0 |= BIT0;`	→	`P1DIR |= BIT6;` `P1SEL1 |= BIT6;`
P2.1 set to TB0.2		**P1.7 set to TB0.2**
`P2DIR |= BIT1;` `P2SEL0 |= BIT1;`	→	`P1DIR |= BIT7;` `P1SEL1 |= BIT7;`

The following comparison summarizes how to update the code to change from using Timer0_B3 to Timer1_B3.

MSP430FR2000

P2.0 set to TB0.CCI1A

```
SYSCFG3 |= TBRMP_1;
TB0CCTL0 |= CCIS_0;
P2DIR &= ~BIT0
P2SEL0 |= BIT0;
```

P2.1 set to TB0.CCI2A

```
SYSCFG3 |= TBRMP_1;
TB0CCTL0 |= CCIS_1;
P2DIR &= ~BIT1
P2SEL0 |= BIT1;
```

Outputting PWM on P2.0 and P2.1

```
P2DIR |= BIT0 | BIT1;
P2SEL0 |= BIT0 | BIT1;
// Setup Timer0_B
TB0CCR0 = 100-1;
TB0CCTL1 = OUTMOD_7;
TB0CCR1 = 75;
TB0CCTL2 = OUTMOD_7;
TB0CCR2 = 25;
TB0CTL = TBSSEL_1 | MC_1 | TBCLR;
```

Timer Interrupt Service Routine

```
#if defined(__TI_COMPILER_VERSION__) ||
defined(__IAR_SYSTEMS_ICC__)
#pragma vector = TIMER0_B1_VECTOR
__interrupt void Timer0_B1_ISR(void)
#elif defined(__GNUC__)
void __attribute__
((interrupt(TIMER0_B1_VECTOR)))
Timer0_B1_ISR (void)
#endif
{

switch(__even_in_range(TB0IV,TB0IV_TBIFG))
    {
        case TB0IV_NONE: break;
        case TB0IV_TBCCR1: break;
        case TB0IV_TBCCR2: break;
        case TB0IV_TBIFG: break;
        default: break;
    }
}
```

→

MSP430FR2311

P2.0 set to TB1.CCI1A

```
//SYSCFG3 |= TBRMP_1;
TB1CCTL0 |= CCIS_0;
P2DIR &= ~BIT0
P2SEL0 |= BIT0;
```

P2.1 set to TB1.CCI2A

```
//SYSCFG3 |= TBRMP_1;
TB1CCTL0 |= CCIS_1;
P2DIR &= ~BIT1
P2SEL0 |= BIT1;
```

```
P2DIR |= BIT0 | BIT1;
P2SEL0 |= BIT0 | BIT1;
// Setup Timer1_B
TB1CCR0 = 100-1;
TB1CCTL1 = OUTMOD_7;
TB1CCR1 = 75;
TB1CCTL2 = OUTMOD_7;
TB1CCR2 = 25;
TB1CTL = TBSSEL_1 | MC_1 | TBCLR;
```

```
#if defined(__TI_COMPILER_VERSION__) ||
defined(__IAR_SYSTEMS_ICC__)
#pragma vector = TIMER1_B1_VECTOR
__interrupt void Timer1_B1_ISR(void)
#elif defined(__GNUC__)
void __attribute__
((interrupt(TIMER1_B1_VECTOR)))
Timer1_B1_ISR (void)
#endif
{

switch(__even_in_range(TB1IV,TB1IV_TBIFG))
    {
        case TB1IV_NONE: break;
        case TB1IV_TBCCR1: break;
        case TB1IV_TBCCR2: break;
        case TB1IV_TBIFG: break;
        default: break;
    }
}
```

See Chapter 12 and Chapter 13 of the MSP430FR4xx and MSP430FR2xx Family User's Guide for more details about Timer_A and Timer_B.

1.3 Comparator

If the MSP430FR2000 code selects P1.2 or P1.3 as an input to the comparator, these pins should be changed to P1.0 or P1.1 (see Figure 3).

MSP430FR2000		MSP430FR2311
P1.2 set to C2 for CPPSEL		**P1.0 set to C0 as CPPSEL**
`P1SEL0 |= BIT2;`		`P1SEL0 |= BIT0;`
`P1SEL1 |= BIT2;`	→	`P1SEL1 |= BIT0;`
`CPCTL0 |= CPPSEL_2;`		`CPCTL0 |= CPPSEL_0;`
P1.3 set to C3 for CPNSEL		**P1.1 set to C1 for CPNSEL**
`P1SEL0 |= BIT3;`		`P1SEL0 |= BIT1;`
`P1SEL1 |= BIT3;`	→	`P1SEL1 |= BIT1;`
`CPCTL0 |= CPNSEL_3;`		`CPCTL0 |= CPNSEL_1;`

Figure 3. Comparator Signals

See Section 6.11.12 eCOMP0 of the MSP430FR231x Mixed-Signal Microcontrollers data sheet and Chapter 17 of the MSP430FR4xx and MSP430FR2xx Family User's Guide for more details about using the comparator.

2 Porting from MSP430FR2311 to MSP430FR2000

The MSP430FR2311 MCU has features not available on the MSP430FR2000, so care should be taken if code is developed on the MSP430FR2311 for the MSP430FR2000. Table 1 summarizes differences between the two MCUs.

Table 1. Comparison of MSP430FR2311 and MSP430FR2000 Features

Feature	MSP430FR2311	MSP430FR2000
Nonvolatile memory (KB)	4	0.5
RAM (KB)	1	0.5
GPIO pins	16	12
I^2C	1	0
SPI	2	1
ADC	10-bit ADC (8 channels)	Slope
Comparators	2	4
Timers (16-bit)	2	1
Active power (µA/MHz)	126	120
Approximate price (US$)	0.56 | 1ku	0.29 | 1ku

For more comparisons between these and other MCU architectures, visit MSP430™ ultra-low-power MCUs.

Table 2 summarizes peripherals of the MSP430FR2311 that are not present on the MSP430FR2000.

Table 2. MSP430FR2311 Peripherals Not Available on MSP430FR2000

Function	Signal Name	Pin Name	PxDIR.x	PxSELx	Description
ADC	A0	P1.0	X	11	Analog input A0
	A1	P1.1	X	11	Analog input A1
	A2	P1.2	X	11	Analog input A2
	A3	P1.3	X	11	Analog input A3
	A4	P1.4	X	11	Analog input A4
	A5	P1.5	X	11	Analog input A5
	A6	P1.6	X	11	Analog input A6
	A7	P1.7	X	11	Analog input A7
	Veref+	P1.0	X	11	ADC positive reference
	Veref-	P1.2	X	11	ADC negative reference
TIA0	TRI0+	P1.7	X	11	TIA0 positive input
	TRI0-	P1.6	X	11	TIA0 negative input
	TRI0O	P1.5	X	11	TIA0 output
SAC0	OA0+	P1.4	X	11	SAC0, OA positive input
	OA0-	P1.2	X	11	SAC0, OA negative input
	OA0O	P1.3	X	11	SAC0, OA output
GPIO	P1.4	P1.4	I: 0; O: 1	00	GPIO that can be configured for edge-selectable interrupt and for LPM3.5, LPM4, and LPM4.5 wake-up input capability
	P1.5	P1.5	I: 0; O: 1	00	
	P1.6	P1.6	I: 0; O: 1	00	
	P1.7	P1.7	I: 0; O: 1	00	
	P2.2	P2.2	I: 0; O: 1	00	General-purpose I/O
	P2.3	P2.3	I: 0; O: 1	00	General-purpose I/O
	P2.4	P2.4	I: 0; O: 1	00	General-purpose I/O
	P2.5	P2.5	I: 0; O: 1	00	General-purpose I/O

Table 2. MSP430FR2311 Peripherals Not Available on MSP430FR2000 (continued)

Function	Signal Name	Pin Name	PxDIR.x	PxSELx	Description
I^2C	UCB0SCL	P1.3, P2.5(1)	X	01	eUSCI_B0 I2C clock
	UCB0SDA	P1.2, P2.4(1)	X	01	eUSCI_B0 I2C data
SPI	UCB0STE	P1.0, P2.2(1)	X	01	eUSCI_B0 slave transmit enable
	UCB0CLK	P1.1, P2.3(1)	X	01	eUSCI_B0 clock input/output
	UCB0SIMO	P1.2, P2.4(1)	X	01	eUSCI_B0 SPI slave in/master out
	UCB0SOMI	P1.3, P2.5(1)	X	01	eUSCI_B0 SPI slave out/master in
Timer_B	TB1.CCI1A	P2.0	0	01	Timer TB1 CCR1 capture: CCI1A input, compare: Out1 output
	TB1.1		1		
	TB1.CCI2A	P2.1	0	01	Timer TB1 CCR2 capture: CCI2A input, compare: Out2 output
	TB1.2		1		
	TB1CLK	P2.2	0	10	Timer clock input TBCLK for TB1
	TB1TRG	P2.3	0	10	TB1 external trigger input for TB1OUTH

(1) This is the remapped functionality controlled by the USCIBRMP bit of the SYSCFG2 register. Only one selected port is valid at any time.

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