Programmable Frequency Locked Loop using MSP430™ MCUs

Introduction

The programmable frequency-locked loop (FLL) function uses the MSP430FR2100 microcontroller (MCU) to offer a simple way to generate multiple frequencies from 1 MHz to 16 MHz with or without an external crystal oscillator. These frequencies are achieved using the internal digitally controlled oscillator (DCO) stabilized with an internal FLL. A fixed 32.768-kHz frequency is also output for use with real-time applications. The MSP430™ MCU can receive commands over a SPI or 4800-baud UART interface, and the ferroelectric random access memory (FRAM) allows the device to recover to the last programmed frequency after reset. This type of functionality is useful for systems that need to generate multiple frequencies using a minimum number of components. To get started, download project files and a code example demonstrating this functionality.

Implementation

The clock system in the MSP430FR2100 device features an FLL that can be used to stabilize the internal DCO and achieve clock frequencies up to 16 MHz. Equation 1 calculates the output frequency of the programmable FLL.

$$f_{output} = (FLLN + 1) \times (32768\ Hz / outputDiv) \quad (1)$$

where

- FLLN ≤ 1023

The FLL requires a reference clock that can be sourced from either an internal 32.768-kHz reference oscillator (REFO) or an external crystal of the same frequency. However, TI recommends using a high-accuracy external 32.768-kHz crystal for best performance. Figure 1 shows the inputs and outputs of the programmable clock source.

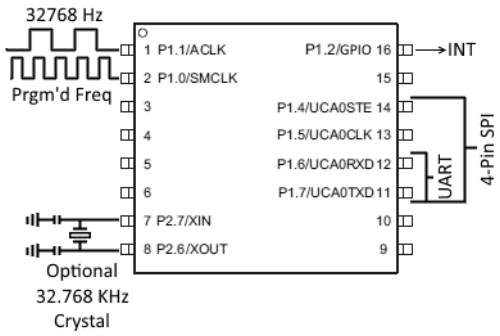

Figure 1. Programmable Clock Source I/Os

The programmable FLL features either a UART interface or SPI, depending on how the user configures the accompanying example code. The UART interface uses P1.6 and P1.7 as receive and transmit, respectively. The SPI uses P1.4 to P1.7, and Table 1 shows the phase and polarity settings required for proper communication.

Additionally, when the programmable FLL needs to alert the host of an event, the INT pin (P1.2) is asserted. Reading from the devices status register described in Table 1 using a get status command shown in Table 2 then deassert the INT pin.

Table 1. 4-Wire SPI Settings

Slave or Master	CLK Phase	CLK Polarity	CS Polarity
Slave	Data changed on first clock edge and captured on second	Inactive state is low	Active low

Either communication interface allows a host processor to set up the FLL using the commands listed in Table 2. To properly set up the FLL, the following commands must be supplied to the MCU:

1. Set the DCO range.
2. Set the FLLN.
3. Set the output divider.
4. Apply the settings.

When programming the FLL, the settings do not take effect until the apply settings command is sent with the exception of the output divider. When an output divider command is sent, its effects are seen immediately at the output. Also, if the user attempts to set a frequency that the FLL cannot achieve using the settings provided, the device reverts to the last known lockable settings.

Table 2. Programmable FLL Command Protocol

Command Description	Command Byte	First Data Byte	Second Data Byte
Apply FLL Settings	0x00	X	X
Set DCO Range	0x01	Data_L	Data_H
Set FLLN	0x02	Data_L	Data_H
Set Output Divider	0x03	Data_L	Data_H
Get Status	0x04	X	X

Table 2 lists two types of commands. The commands that contain *X* for both data bytes are single-byte commands that require only the first byte be sent. The others are multiple-byte commands, and the first byte is the command and the second and third contain data. These two bytes combine to create a 16-bit number with the second byte containing the lower 8 bits (Data_L) and the third byte containing the upper 8 bits (Data_H).

For example, if the user is attempting to set the DCO range to 8 MHz according to Table 3, the following must be sent to the programmable FLL:

1. Command Byte: 0x01
2. Data_L: 0x06
3. Data_H: 0x00

Table 3. DCO Range Settings

Description	Data_L	Data_H
1 MHz	0x00	0x00
2 MHz	0x02	0x00
4 MHz	0x04	0x00
8 MHz	0x06	0x00
12 MHz	0x08	0x00
16 MHz	0x0A	0x00

Additionally, the output divider has a limited number of settings similar to the DCO range. Table 4 lists the available output divider settings and the corresponding data bytes.

Table 4. Output Divider Settings

Description	Data_L	Data_H
Divide by 1	0x00	0x00
Divide by 2	0x01	0x00
Divide by 4	0x02	0x00
Divide by 8	0x03	0x00
Divide by 16	0x04	0x00
Divide by 32	0x05	0x00
Divide by 64	0x06	0x00
Divide by 128	0x07	0x00

For both the output divider and DCO range settings, the Data_H byte is always 0x00. This is so that the FLLN, DCO range, and output divider commands are all 3 bytes in length. This removes the need to process different length commands and reduces code size.

The programmable FLL contains a status register (see Table 2) that can be read using the get status command. This register can be used to monitor several important parameters including the execution status of the last command, if the external crystal is oscillating, and if the FLL is locked.

The status register also signals if the user tried to set a frequency outside the selected DCO range and if a command not specified in Table 2 was sent to the device.

Each bit in the register is active high, meaning if the FLL is currently unlocked, BIT4 is 1. Additionally, the invalid command and DCO range error bits are cleared only when the status register is read using a get status command.

The programmable FLL can achieve frequencies in the range of 1 MHz to 16 MHz with ±2% accuracy using the internal REFO or ±0.5% accuracy using an external crystal. More detailed performance specifications can be found in the clock specifications section of the MSP430FR2100 MCU data sheet. Overall, the accuracy and power consumption is improved when using an external crystal oscillator.

After a device reset, the MSP430 MCU applies the FLL settings stored in FRAM from the last known output frequency before device reset. This frequency is output on P1.0, and the FLL reference is output on P1.1.

The provided code detects both an FLL unlock and an external crystal fault. If an FLL unlock is detected, the device attempts to relock four times before alerting the host processor by asserting the INT pin. If an external crystal fault occurs, the FLL reference switches to REFO, and the INT pin is asserted to alert the host. The device then attempts to use the external crystal only at device reset. The device then times out and uses REFO after 4 seconds if the crystal is still not oscillating correctly.

Finally, to ensure the FLL is always active, the deepest low-power mode (LPM) the MSP430 MCU can enter is LPM0. The current consumption is dependent on the frequency being output and can range anywhere from 157 µA at 1 MHz to 402 µA at 16 MHz. For more information on current consumption, see the MSP430FR2100 MCU data sheet.

Table 5. Programmable FLL Status Register

X (BIT7)	INVALID COMMAND (BIT6)	DCO RANGE ERROR (BIT5)	FLL UNLOCKED (BIT4)	LFXT FAULT (BIT3)	PROCESSING (BIT2)	FAIL (BIT1)	SUCCESS (BIT0)
Don't care	An invalid command was received since the status register was last read.	The user tried to set an invalid DCO range since the status register was last read.	The FLL is currently unlocked.	The LFXT is not oscillating properly and/or REFO is sourcing the FLL reference.	The device is currently processing a command.	The last command failed to execute properly.	The last command executed successfully.

Device Recommendations

The device used in this example is part of the MSP430 Value Line Sensing portfolio of low-cost MCUs, designed for sensing and measurement applications. This example can be used with the devices shown in Table 6 with minimal code changes. For more information on the entire Value Line Sensing MCU portfolio, visit www.ti.com/MSP430ValueLine.

Table 6. Device Recommendations

Part Number	Key Features
MSP430FR2000	0.5KB FRAM, 0.5KB RAM, eComp
MSP430FR2100	1KB FRAM, 0.5KB RAM, 10-bit ADC, eComp
MSP430FR2110	2KB FRAM, 1KB RAM, 10-bit ADC, eComp
MSP430FR2111	3.75KB FRAM, 1KB RAM, 10-bit ADC, eComp

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