Application Report

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Software Glass LCD Driver Based on MSP430 MCU

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ABSTRACT

This application report provides the technique of driving a glass liquid crystal display (LCD) with the MSP430 microcontroller without using any external LCD driver hardware. It also guides for development of an effectively low-cost solution for applications with display requirements.

Project collateral and source code discussed in this application report can be downloaded from the following URL: http://www.ti.com/lit/zip/slaa516.

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1 Introduction

The technique presented in this document can be implemented with any microcontroller of the MSP430 family that does not have an LCD controller peripheral module in the hardware. This technique utilizes only I/O port lines and a standard timer module of the MSP430 microcontroller. The number of microcontroller I/O lines required for driving a given LCD with this method is the same as that required of a microcontroller with a built-in LCD controller peripheral. The number of external components is kept to the lowest possible (two resistors per COM lines).

The basic operation of glass LCD is explained in Section 2.

Various backplane options and their respective waveform implementations in which glass LCD can be driven are explained in Section 3.

A low-cost display solution that can be implemented by interfacing a glass LCD with MSP430G2xx (value line series) is explained in Section 4.

Section 4.1 and Section 4.2 provide an overview of the hardware and software aspects of the demo made on the MSP430G2333 device (value line MSP430 microcontroller). This allows to develop and test applications using an LCD device with the MSP430 microcontroller.

2 Glass LCD Operation

A glass LCD basically has two glass plates joined together with a very small gap in between the plates. This gap contains a liquid crystal fluid. When no potential difference is applied between the plates, the liquid crystal molecules maintain their helical structure and a transparent display is visible. However, if an electric field is applied, the molecules arrange themselves to align with the field direction and a black segment is visible on a clear background. The potential difference has to be applied between the COM and SEG lines of the LCD glass to make the display work.

When a potential difference lower than the LCD threshold voltage (minimum voltage to make a segment molecules polarize) is applied, the LCD segments are OFF and a transparent display is visible. To turn the LCD segments ON (grey color), the potential difference has to be greater than the LCD threshold voltage. The threshold voltage level depends on the nature of liquid used in the LCD and the temperature conditions.

The optical contrast is defined by the difference in transparency of an LCD segment that is ON (dark) and an LCD segment that is OFF (transparent). The optical contrast depends on the difference between the RMS voltage of an ON segment (VON) and the RMS voltage of an OFF segment (VOFF). The higher the difference between VON(rms) and VOFF (rms), the higher the optical contrast.

Note that the LCD voltage applied between the SEG and COM lines should be alternating in nature to give zero dc offset to ensure long LCD lifetime. The DC offset should not typically exceed 100 mV value. (The maximum dc offsect allowed is mostly available in the LCD manufacturer's specifications.)

The frequency range of the alternating signal is also critical for driving the glass LCD (between 30 Hz to 200 Hz). If the frequency of the alternating signal is too low, the LCD flickers and if it is on the high side, power consumption increases.

3 Backplane Options

Common forms of available backplane options in a glass LCD are:

- Single backplane
- Duplex backplane
- Quadruplex backplane

In the case of a *single* backplane drive, each LCD segment is connected to a segment line (SEGx) and a single backplane (COM line). This backplane is common to all LCD segments. The backplane (COM line) is driven between zero and V_{CC} voltage levels with a duty cycle of 50%.

When the segment line (SEGx) signal and COM pin are in opposite polarity, the corresponding display segment is ON. Similarly, if the signal on the segment line (SEGx) and the COM line are in the same polarity, the corresponding display segment is OFF. So, the LCD display can be controlled by toggling the connected MCU I/O lines between logic 0 and 1.

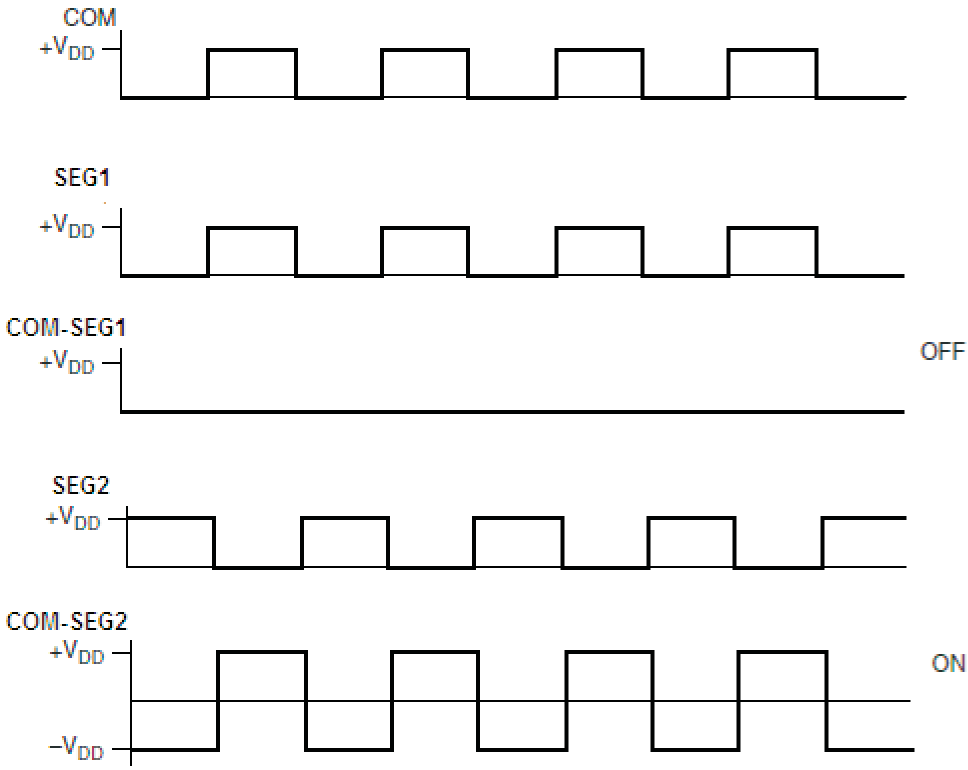


Figure 1. Glass LCD Display Using *n* Segments is Driven With *n*+1 GPIO Lines of MCU

Two backplanes are present in the case of the *duplex* backplane drive: two display segments are connected to each SEGx line on one side and the display segments have different backplanes (COMx lines) connected on the other side. So, two display segments share the same SEGx line with two different backplane (COMx) on the other side.

In this configuration, the SEGx line operates at two voltage levels: zero and V_{DD}. COM lines have to be operated at three different voltage levels: zero, V_{DD} and $V_{DD}/2$. So, driving an MCU I/O line in output mode can operate at zero volts (low-logic level) and V_{DD} volts (high-logic level). The $V_{DD}/2$ level is attained by using two resistors of equal value connected on the COM lines and putting the MCU I/O line in high-impedance input mode. In this backplane configuration, at any instant one COM line is activated, the other one is kept at $V_{DD}/2$ logic level.

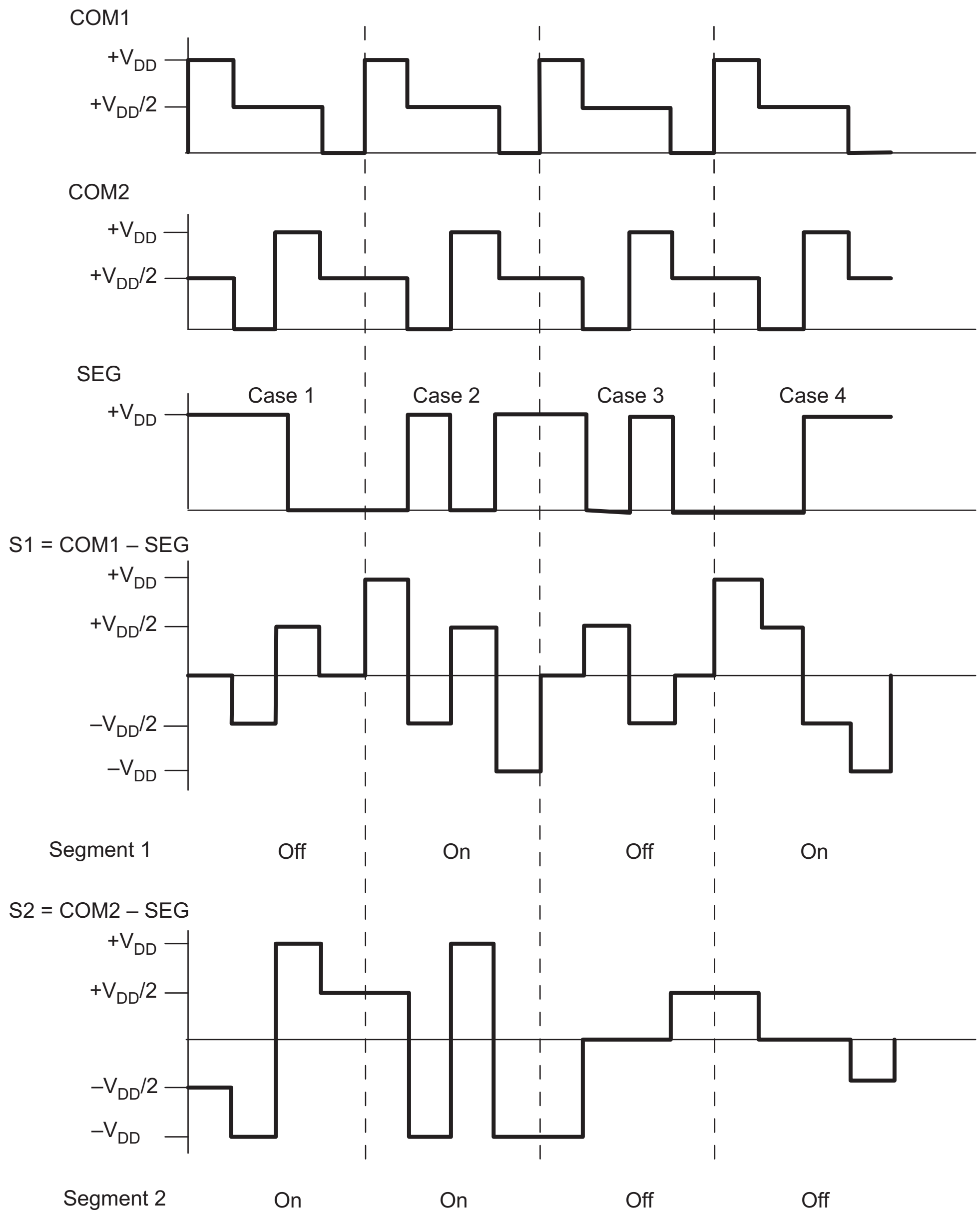


Figure 2. Glass LCD Display Using *n* Segments is Driven With *n*/2+2 GPIO Lines of MCU

Four backplanes are present in the case of the *quadruplex* backplane drive: four display segments are connected to each SEGx line on one side and the display segments have different backplanes (COMx lines) connected on the other side. So, four display segments share the same SEGx line with four different backplane (COMx) on the other side.

The SEGx line operates at two voltage levels: zero and V_{DD}. COM lines have to be operated at three different voltage levels: zero, V_{DD} and $V_{DD}/2$. So, driving an MCU I/O line in output mode can operate at zero volts (low-logic level) and V_{DD} volts (high-logic level). The $V_{DD}/2$ level is attained by using two resistors of equal value connected on the COM lines and putting the MCU I/O line in high-impedance input mode. The instant one COM line is activated, the other COM lines are kept at $V_{DD}/2$ logic level.

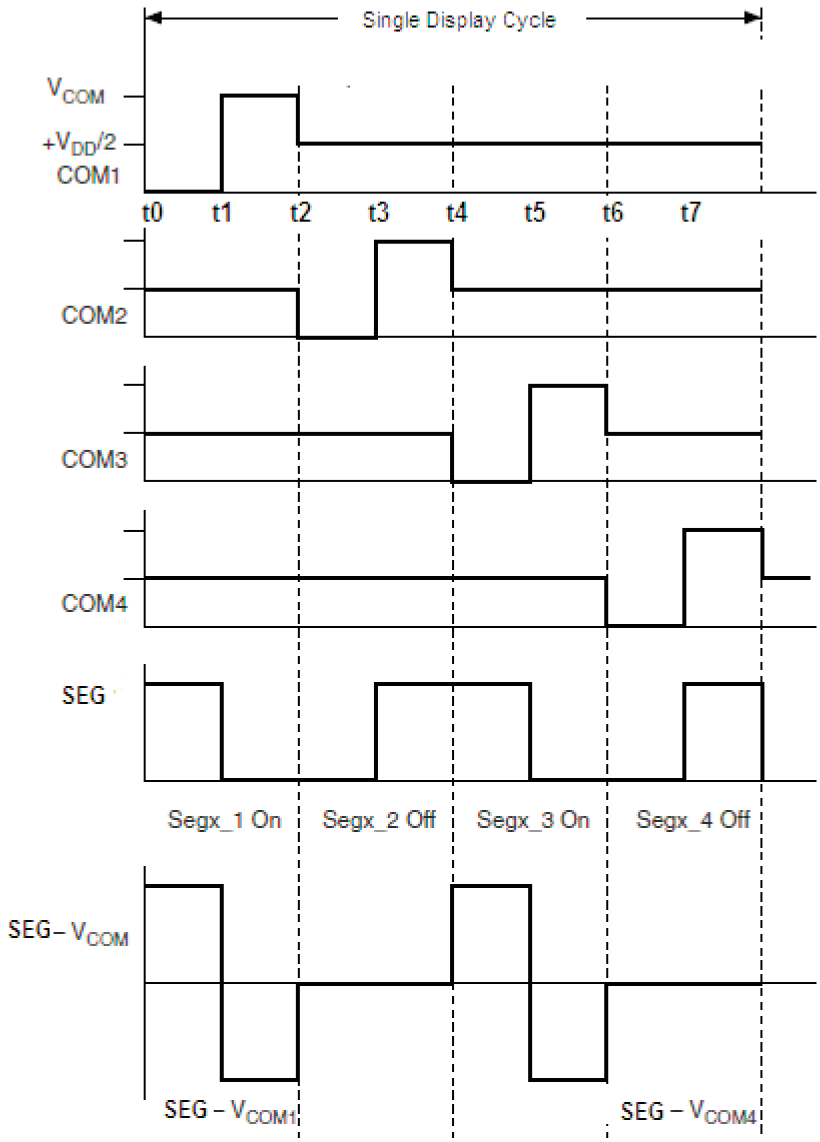


Figure 3. Glass LCD Display Using *n* Segments is Driven With *n*/4+4 GPIO Lines of MCU

4 Implementation of Software Glass Driver on MSP430G2333

The following section provides details about the hardware and software aspects of a display solution based on the software glass driver on the MSP430G2333 microcontroller (MSP430 value line family device). For this project, a glass LCD with *quadruplex* backplane has been interfaced with the MCU. The glass LCD specs are shown in Figure 5.

MSP430G2333 is a ultra low-power MCU based on the MSP430 core targeting low-cost applications. For more details about the the microcontroller, see the following link:

- http://www.ti.com/product/msp430g2333

4.1 Hardware Connections

The glass LCD interfaced in this implementation is used for the first 64 segments only. The 8 SEG lines (Pin 5 to Pin 12) are directly connected to Port 1 of the MSP430 and the COM lines are connected to Port pin 2.0-2.3 with a resistive network as shown in Figure 4.

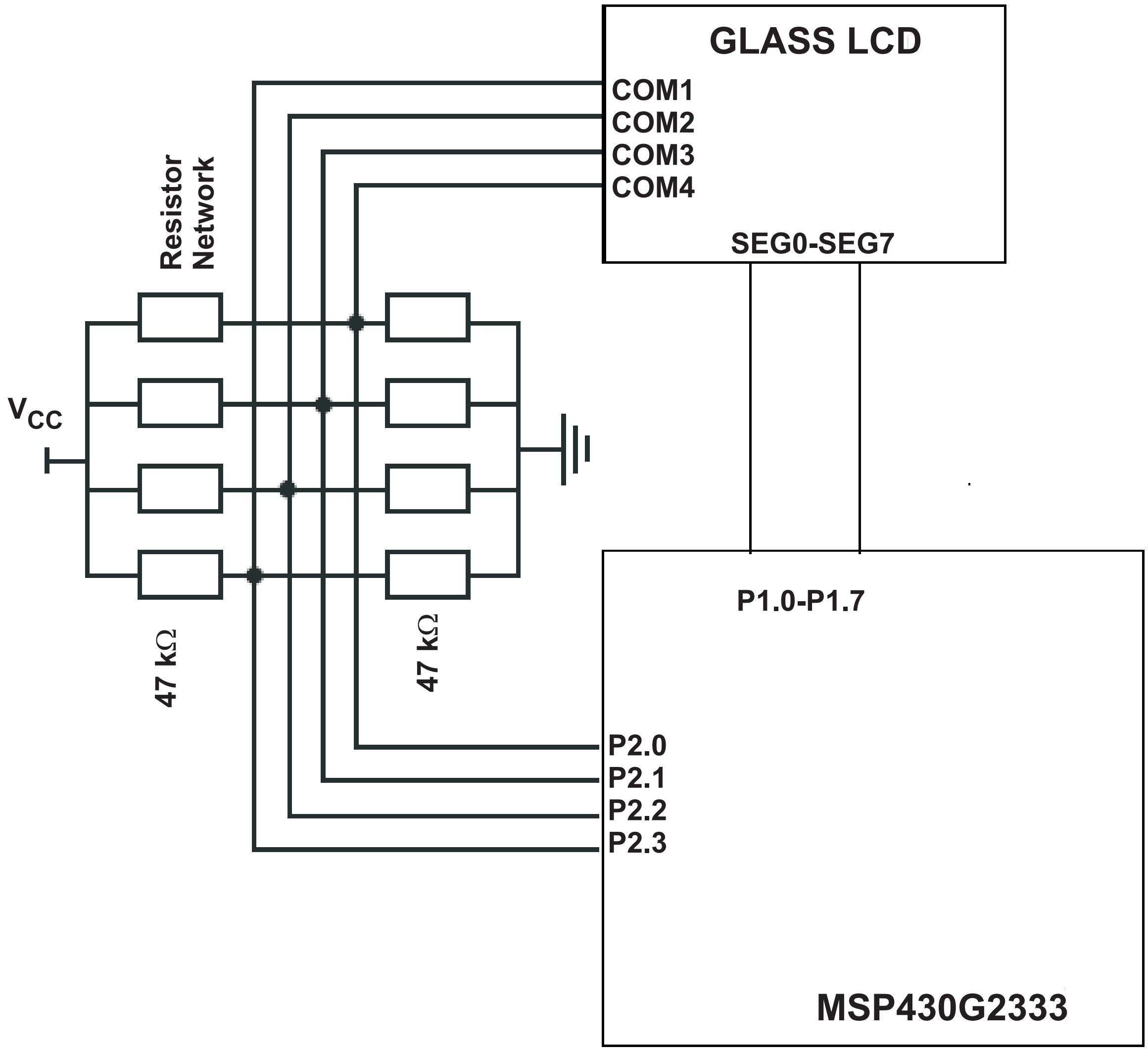
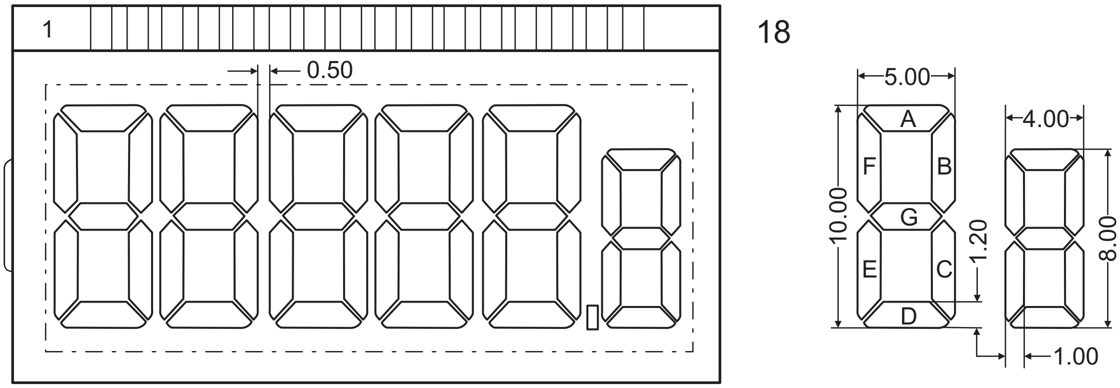


Figure 4. Glass LCD Connections to MSP430G2333 Device

For every glass LCD, the mapping table of each character display segments with SEG and COM lines and is available in the LCD manufacturer's sheet. The LCD used in this demo has the specs given in Figure 5.



PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
COM1				COM1	1F	1A	2F	2A	3F	3A	4F	4A	5F	5A	6F	6A
COM2			COM3		1G	1B	2G	2B	3G	3B	4G	4B	5G	5B	6G	6B
COM3		COM3			1E	1C	2E	2C	3E	3C	4E	4C	5E	5C	6E	6C
COM4	COM4					1D		2D		3D		4D		5D	DOT1	6D

Figure 5. Glass With Mapping Table

The schematic of digital clock implementation is shown in Figure 6.

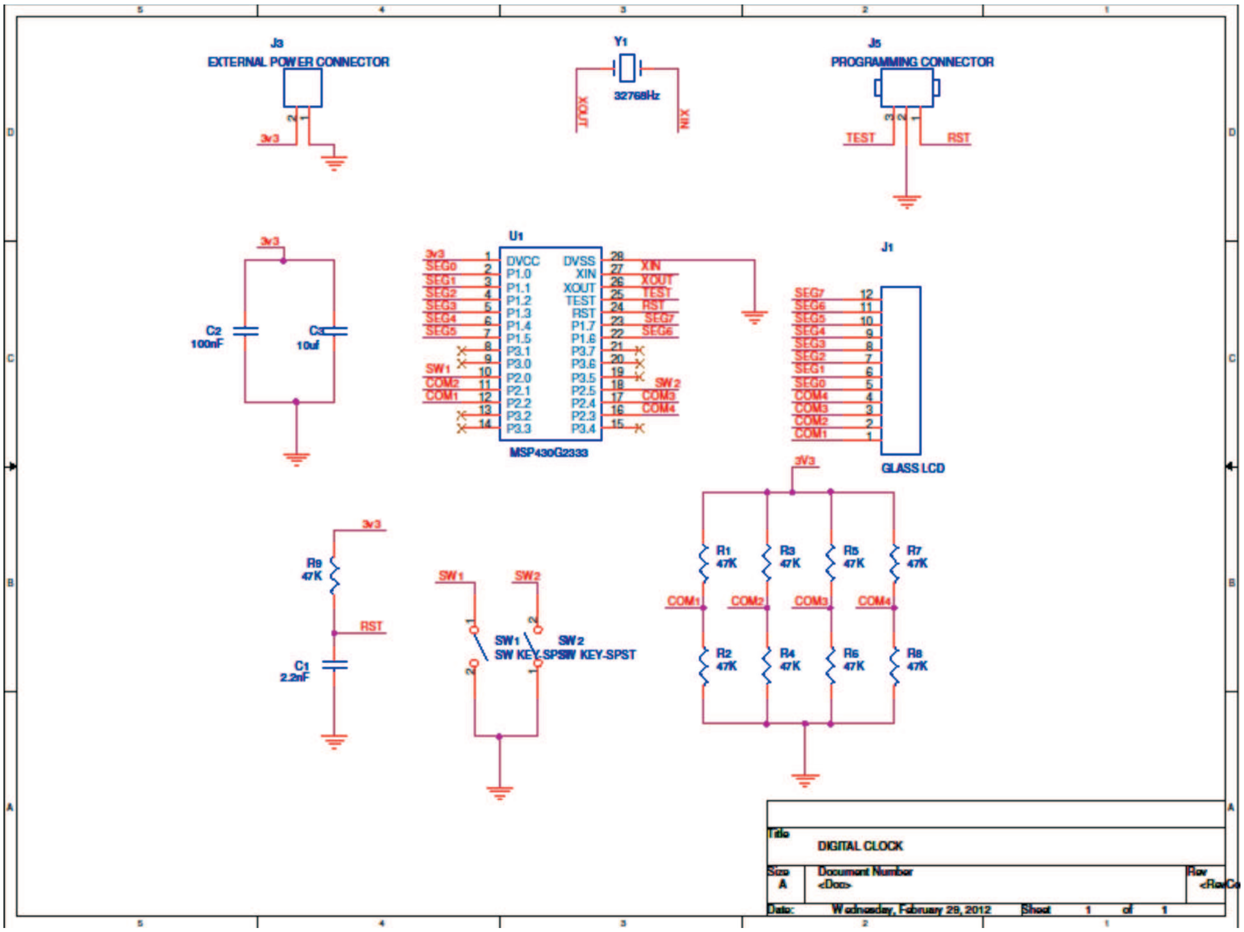


Figure 6. Digital Clock Implemenation Schematic

4.2 Software

The glass LCD is working in *quadruplex* mode; the implementation of waveforms on the COM lines has to be similar to that shown in Figure 3. The watchdog timer of MSP430G233 has been used in timer interval modes to provide interrupts at time periods equal to T/8 as shown in Figure 3. The software code uses the variable MEM[] to set or reset the corresponding segment lines as shown in Figure 7.

The software code for this implementation is available at: http://www.ti.com/lit/zip/slaa516.

This can also be used for implementation of a simple digital clock functionality that updates the time on Glass LCD every 1 second.

		MEM (n)								MEM (n+1)							
n = 0	COM1	1F	1A	2F	2A	3F	3A	4F	4A	5F	5A	6F	6A	7F	7A	8F	8A
n = 1	COM2	1G	1B	2G	2B	3G	3B	4G	4B	5G	5B	6G	6B	7G	7B	8G	8B
n = 2	COM3	1E	1C	2E	2C	3E	3C	4E	4C	5E	5C	6E	6C	7E	7C	8E	8C
n = 3	COM4		1D		2D		3D		4D		5D		6D		7D		8D

Figure 7. Software Handling of Segment Lines

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