Application Report
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Programming With the MSP430AFE2xx Family and the MSP430i20xx Family

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ABSTRACT

This application report enables the easy incorporation of the MSP430AFE2xx family of MCUs, featuring the SD24_A module, as well as the MSP430i20xx family of MCUs, which features the SD24 module, into new designs. It covers programming, system, and peripheral considerations when creating firmware. The intent is to highlight a few key differences between the two families and how to incorporate each into your design. For more information on the use of the MSP430i20xx devices, see the *MSP430i20xx Family User's Guide* (SLAU335). For more information on the use of the MSP430AFE2xx devices, see the *MSP430x2xx Family User's Guide* (SLAU144). Although the MSP430AFE2xx family is used as a base for comparison, similar considerations apply when incorporating MSP430i20xx devices in systems that used devices from the MSP430F2xx, MSP430G2xx, MSP430F1xx, and MSP430F4xx families.

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1 Introduction

The purpose of this application report is to highlight the key differences between the MSP430AFE2xx family and the MSP430i20xx family to ensure a smoother incorporation of the two families into new designs. It is divided into three main parts; (1) system-level considerations and hardware considerations, (2) device calibration and specifications, and (3) peripheral differences. With respect to the instruction set, the MSP430i20xx is completely backward code compatible with all other MSP430™ families. Any code migration is therefore impacted only by register or peripheral feature changes and slight variations in instruction cycle times, while the instruction set remains the same.

For any specific information, refer to the device-specific data sheet.

NOTE: For the purpose of this application report, the term AFE2xx indicates the MSP430AFE2xx family and the term i20xx indicates the MSP430i20xx family.

2 In-System Programming of Nonvolatile Memory

2.1 JTAG and Security

On AFE2xx devices, the JTAG port is secured by blowing a physical fuse on one of the JTAG lines by subjecting it to a high voltage through a special procedure. This action is irreversible, and further access to the device is only possible via the BSL.

On i20xx devices, the physical fuse has been replaced by a programmable JTAG fuse. Securing the device involves writing a specific signature to the SYSJTAGDIS register. This write must take effect within the first 64 MCLK clock cycles after a BOR or POR reset; otherwise the JTAG port is enabled. Any writes to this register after the first 64 MCLK clock cycles are ignored. Reads from this register at any time return the JTAG enable or disable status.

Additionally, the i20xx family of devices does not include a BSL to access the device when JTAG is locked. Instead, application software must include Startup Code to handle device security and peripheral calibration.

NOTE: Application programming the device to any of the low-power modes within the first 64 MCLK cycles after a BOR or POR reset will lock the device for any JTAG or SBW access.

2.1.1 Start-Up Code (SUC) – Device Security Handling

The i20xx device requires start-up code to be run before main application code. The start-up code must be included in the application by the user and is not present on the device by default. Start-up code takes care of device security as well as peripheral calibration functions. This code is executed every time after reset – BOR, POR, or PUC.

JTAG access on the i20xx family of devices is disabled by default after a BOR or POR reset. The SUC must choose to either enable or disable JTAG access within the first 64 MCLK cycles. There are four bytes near the end of the flash code memory (0xFFFF) that are designated for the JTAG disable password. This value should be read and compared to the expected value. If the value read is different than the expected value, then the SUC should write 0xA5A5 into the SYSJTAGDIS register. This disables JTAG access and secures the device. If the value read matches the expected value, no action should be taken and the SUC should immediately enter the peripheral calibration routine. Taking no action enables JTAG access and the device is unsecured automatically.

2.2 Production Programming

MSP-GANG430 does not support the i20xx devices. This production programmer has been superseded by MSPGANG (www.ti.com/tool/msp-gang).

3 Hardware Migration Considerations

- For JTAG and SBW connections on the i20xx devices, see the *MSP430 Hardware Tools User's Guide* (SLAU278).
- The i20xx devices do not support external oscillators and must be clocked either by the internal DCO or via an external 16.384-MHz digital clock signal.

4 Device Calibration Information

Similar to the AFE2xx family of devices, the i20xx family of devices provides a TLV structure that supplies calibration values for selected peripherals. The TLV structure for both is stored within the Information Memory and can be erased by the developer.

NOTE: Certain IDE settings can also erase the Information Memory on the device. To ensure that the Information Memory is not erased, the “Erase main memory only” Erase Option within the Project Properties → Debug → MSP430 Properties window is selected by default.

4.1 Start-up Code (SUC) – Peripheral Calibration Handling

In addition to device security, the SUC also must calibrate the specified peripherals. For the i20xx series of devices, the peripherals that require calibration are the shared reference (REF), the DCO, and the SD24.

Prior to this, the SUC should check for the BORIFG flag to determine if calibration values need to be reloaded. Only when a power cycle occurs will the values in the calibration registers not be retained, and thus when a non-power cycle event resets the part, no re-calibration is required. When the BORIFG is not set, the calibration is skipped; when the BORIFG is set, the SUC continues into the peripheral calibration.

The peripheral calibration values for the specific peripherals are stored within the TLV structure at the end of the Information Memory segment of flash memory. Before loading the values located in these locations, a checksum for the entire TLV contents should be run to ensure the validity of the TLV contents. If the checksum does not match, it is recommended to program the device into LPM4 mode. If the checksum does match, then the SUC proceeds with peripheral calibration.

Peripheral calibration is completed by copying the values from the TLV structure to the corresponding peripheral registers. For more details, refer to the *MSP430i20xx Family User's Guide* (SLAU335).

5 Important Device Specifications

Table 1 shows important differences in device-level electrical specifications.

Table 1. Device Specifications

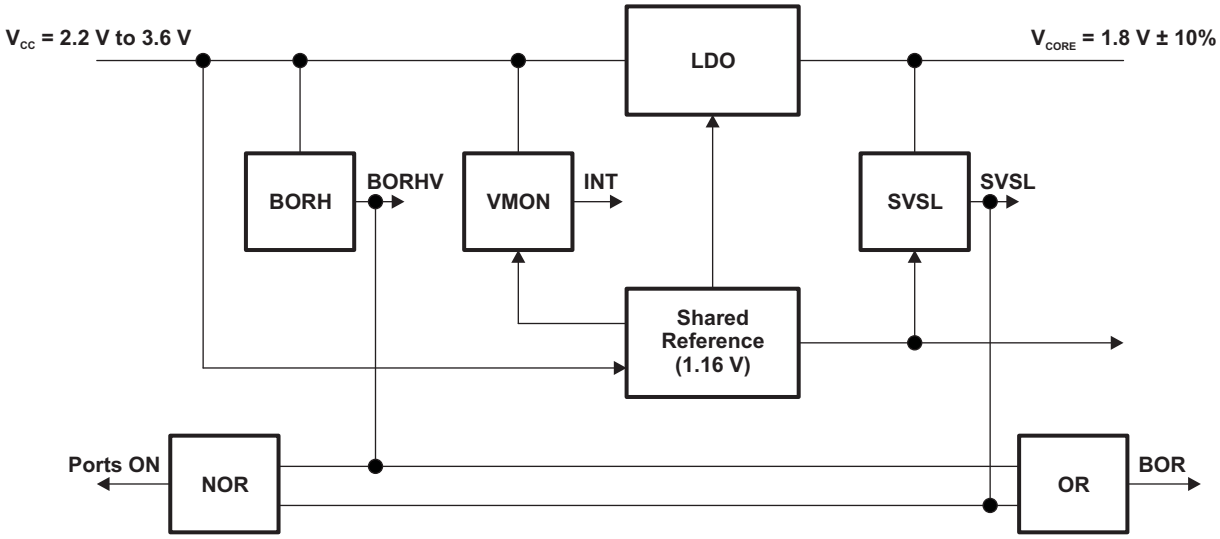
Parameter	i20xx	AFE2xx
Supply voltage range	2.2 V to 3.6 V	1.8 V to 3.6 V
Maximum system frequency, f_{system}	16.384 MHz	12 MHz
Operating free-air temperature	-40°C to 105°C	-40°C to 85°C
Analog front end input clock frequency	1.024 MHz	30 kHz to 1.1 MHz
Minimum analog supply voltage for ADC operation	2.2 V	2.5 V

Note that the most significant impacts in migrating from the AFE2xx family to the i20xx family are the restrictions on the clock system frequencies, as well as the free-air operating temperatures. The i20xx family of devices is specified to use just the 16.384-MHz clock generated by the DCO, or an external digital signal of similar frequency. Additionally, the i20xx series is targeted to a broader operating free-air temperature range, up to 105°C.

6 Core Architecture Considerations

6.1 Power Management Module (PMM)

Similar to the AFE2xx family of devices, the i20xx family of devices uses a single voltage rail to power the chip; that is a single voltage rail supplies both the analog and the digital core on the chip. The external voltage supply on the V_{CC} pin is fed to an internal low-dropout voltage regulator (LDO) that supplies V_{CORE} to the CPU, memories, and digital modules, while V_{CC} supplies the I/Os and analog modules (see Figure 1).



NOTE: BORHV is active-high polarity (1 = V_{CC} domain is in reset). SVSL is active-high polarity (1 = V_{CORE} domain is in reset).

Figure 1. PMM Block Diagram

In addition to providing the voltage rails for the part, the PMM module on the i20xx family of devices also controls the Brownout Reset (BOR) and Supply Voltage Supervisor (SVSL) for power up, a voltage monitor, and the control/calibration of the shared reference.

The BOR circuit shown in Figure 1 is primarily used when the device is powering up. The BOR is functional very early in the power-up ramp and generates a reset to initialize the system. The BOR circuit also functions when a brown out condition occurs after power-up, sustaining the reset until the input voltage is high enough for a proper reset. The SVSL circuit gives an indication on whether or not the V_{CORE} is in the usable range for the digital core and the rest of the circuitry it powers. Early in the power-up ramp, the PMM holds the device in BOR reset. After V_{CC} rises high enough, the LDO is turned on and ramps up V_{CORE}. When V_{CORE} rises above the SVSL level, the BOR is released after a small delay. This process is shown in Figure 2.

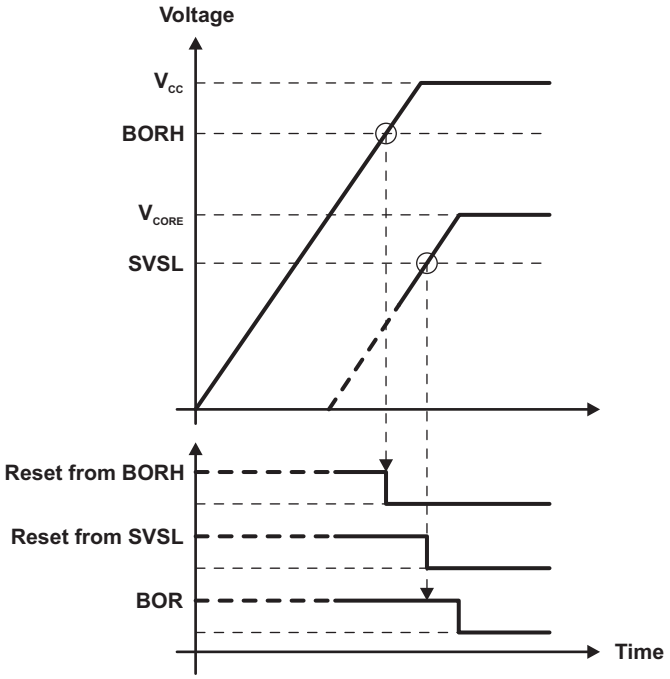


Figure 2. Power-Up Sequence

The PMM's voltage monitor (VMON) compares the voltage applied either to the external VMONIN pin, or the on-chip DVCC to a specified limit. If the monitored voltage falls below the threshold, an interrupt is triggered. By default, the VMON is disabled on power-up but can be enabled and configured using the VMONCTL register.

The final control that the PMM module provides is for the Shared Reference (REF) that is a general-purpose reference system for many other peripherals. On the i20xx family of devices, the reference voltage generated by the REF is fixed at 1.16 V. The calibration for the voltage and current for the specified accuracy should be programmed into the REFCAL0 and REFCAL1 registers. These values can be found in the TLV section of the Information Memory block of flash memory.

For additional details on the PMM and its use, refer to the *MSP430i20xx Family User's Guide* (SLAU335).

6.2 Clock System

The clock system of the i20xx family of devices differs greatly from that of the AFE2xx family of devices, and is much simpler. The clock system (CS) only requires one input, a 16.384-MHz digital clock signal, which can be provided either by the DCO or by an external input, bypassing the DCO entirely. From this 16.384-MHz signal, all of the clock signals on the i20xx devices are derived. Both ACLK and the SD24 clock are automatically divided down by 512 and 16, respectively, while MCLK and SMCLK have selectable dividers as is shown in Figure 3.

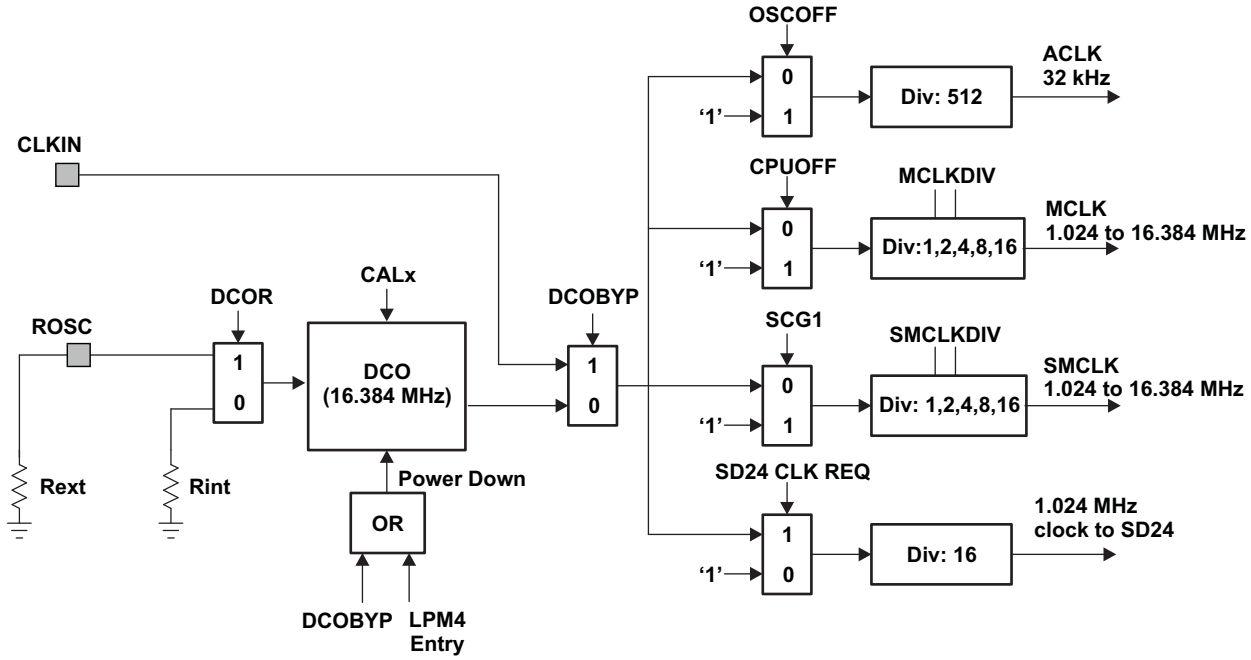


Figure 3. Clock System Block Diagram

When using the DCO to source the CS of the i20xx devices, it may be set up in two ways, either using the internal resistor or by connecting a 20-kΩ 0.1% ±50-ppm/°C external resistor at the ROSC pin of the device. The external resistor mode offers higher clock accuracy in terms of absolute tolerance and temperature drift compared to internal resistor mode. In both cases however, the DCO must be calibrated via the values found in the TLV section of the Information Memory block.

Important differences between the clock systems are shown in Table 2.

Table 2. Comparison of i20xx and AFE2xx Clock Systems

Parameter or Feature	i20xx	AFE2xx
Maximum system frequency, f_{system}	16.384 MHz	12 MHz
DCO range	16.384 MHz	0.06 MHz to 12 MHz
Production calibrated frequencies	16.384 MHz	8 MHz, 12 MHz
Clock sources for ACLK	DCO, CLKIN	VLO
Registers	CSCTL0, CSCTL1, CSIRFCAL, CSIRTCAL, CSERFCAL, CSERTCAL	DCOCTL, BCSCTL1 through BCSCTL3
XT1 oscillator	Not available	Not available
XT2 oscillator	Not available	Supports up to 16 MHz
Internal load capacitors for XT1 oscillator	Not applicable	Available

6.3 Operating Modes, Wakeup, and Reset

The operating modes that are available and the wakeup times from LPMs are compared in Table 3.

Table 3. Comparison of Operating Modes and Wakeup Times

Parameter or Feature	i20xx	AFE2xx
LPM0, LPM1, LPM2, LPM3, LPM4	Available	Available
LPM4.5	Available	Not available
Wakeup time from LPM3(1)	1 µs	1.5 µs
Wakeup time from LPM4(1)	35 µs	1.5 µs
Wakeup time from BOR event(1)	0.75 ms (max)	2 ms (max)

(1) The values in this table are approximations; to find the values for a specific device, see the data sheet.

The code flow for entry into and exit out of low-power modes LPM0 to LPM4 remains the same in the i20xx family as in the AFE2xx family. There are minor differences in functionality between the low-power modes on the AFE2xx compared to the i20xx. These differences are described in the System Resets, Interrupts, and Operating Modes chapter of the *MSP430i20xx Family User's Guide* (SLAU335).

One low-power mode not included in the AFE2xx family is LPM4.5. In this mode, the V_{CORE} LDO is turned off, powering down the digital core, RAM, and peripherals. To wake up from LPM4.5, an active-low event on $\overline{RST}$/NMI pin, a power-on cycle, or specific I/O interrupt is required. See the device-specific data sheet for details on LPM4.5 wakeup capable I/Os. Any exit from LPM4.5 causes a BOR, and program execution continues at the location stored in the system reset vector location 0xFFFE.

6.4 Interrupt Vectors

The i20xx devices use an interrupt vector (IV) structure for any interrupt service routine that is sourced by multiple flags.

For example, in the F2xx family, the USCI TX interrupt sources the RX and TX interrupt flags, and the USCI RX interrupt sources all the status flags. In the case of the i20xx family, all of these interrupt flags are captured using a single interrupt vector UCBxIV. This allows interrupt servicing to be more efficient and ensures the same pre-defined latency for all interrupts.

7 Peripheral Considerations

7.1 Ports

7.1.1 Digital Input/Output

The main differences in the i20xx general-purpose I/O (GPIO) pins are:

- **No** GPIOs have internal configurable pullup or pulldown resistors
- Peripheral function select in the i20xx devices uses two registers: Port x Function Selection Register 0 (PxSEL0) and Port x Function Selection Register 1 (PxSEL1).

Similar to the AFE2xx devices, the i20xx devices have the JTAG pins multiplexed with GPIOs within Port 1 and/or Port 2.

The following code sequence is required to initialize GPIOs on reset and wakeup from LPM4.5:

- Initialize all port pin registers as required for function: Port x Direction Register (PxDIR), Port x Output Register (PxOUT), and Port x Interrupt Edge Select Register (PxIES).
- Clear the LOCKLPM5 bit (only when waking up from LPM4.5).LPM45CTL &= ~LOCKLPM45
- If not waking up from LPM4.5, clear all Port x Interrupt Flag Register (PxIFG) to avoid erroneous port interrupts.
- Enable port interrupts using Interrupt Port x Interrupt Enable Register (PxIE).

For more information, see the I/O Configuration and LPM4.5 Low-Power Mode section of the Digital I/O chapter in the *MSP430i20xx Family User's Guide* (SLAU335).

7.2 Analog to Digital Converters

7.2.1 SD24_A to SD24

Some of the significant differences between the SD24_A (AFE2xx) and the SD24 (i20xx) modules are:

- The SD24 is significantly lower power per channel than the SD24_A. To compare parameters such as supply current, see the device specific data sheet.
- The SD24 operates over the entire voltage range of the device (2.2 V to 3.6 V).
- The SD24 is a continuous-time delta-sigma converter, meaning that its architecture is made for a particular modulation frequency (1.024 MHz), while the SD24_A uses a switched capacitor input stage to have a modifiable modulation frequency.
- The PGA for the SD24 module only provides gain settings of up to 16x, while the SD24_A can provide a gain setting of 32x.
- The SD24 module does not have internal connections to sense V_{CC}. This is implemented in the i20xx VMON within the PMM.
- The input range for the SD24_A is defined as $V_{FSR} = V_{REF} / (2 \times GAIN_{PGA})$, while the input range of the SD24 is defined as $V_{FSR} = V_{REF} / (GAIN_{PGA})$, giving the SD24 twice the full-scale analog input range of the SD24_A.
- The SD24 module only allows for an oversampling ratio (OSR) up to 256, while the SD24_A module allows for an OSR up to 1024.
- The SD24 module only outputs data in bipolar formats but supports both offset binary and twos complement interpretations.

7.3 Communication Modules

7.3.1 USART to eUSCI

One of the major differences between the i20xx devices and the AFE2xx devices is the serial communication module. On the i20xx devices, the eUSCI module is implemented. It is the most up-to-date MSP430 communication module, offering more features and functionality to the user. The USART (AFE2xx devices) and eUSCI modules are not software compatible and, therefore, AFE2xx software using the USART module needs to be adapted to make use of the eUSCI module.

The i20xx features two independent and identical eUSCI modules, both of which provide two communication channels that operate simultaneously. With the i20xx, for example, it is possible to service two SPI communication channels or one I2C plus one UART channels, simultaneously. Note that I2C operation is a mode that was not available on AFE2xx devices.

It is not in the scope of this application report to discuss all possible aspects regarding migrating application code to use the eUSCI interface; however, a few items are outlined to highlight major differences between the devices (and the modules). In general, it is strongly recommended to carefully review both module descriptions in the appropriate device family user's guide, as well as to use the eUSCI code examples provided in the product folders on the MSP430 web page (www.msp430.com) as a starting point for any code that is newly created.

8 Conclusion

This application report describes many key feature changes and new modules in the MSP430i20xx family compared to the MSP430AFE2xx family. While this document is intended to be comprehensive, there may be minor differences between the AFE2xx and the i20xx families that have not been covered here. For details of a given device, the device-specific data sheet is always the best source of information. For module functionality and use, see *MSP430i20xx Family User's Guide* (SLAU335).

For developers working with the i20xx devices, a useful resource for getting started is MSP430Ware™ software (http://www.ti.com/msp430ware).

9 References

1. *MSP430i20xx Family User's Guide* (SLAU335)
2. *MSP430x2xx Family User's Guide* (SLAU144)
3. *MSP430i20xx Mixed-Signal Microcontrollers* (SLAS887)
4. *MSP430AFE2xx Mixed-Signal Microcontrollers* (SLAS701)
5. *Code Composer Studio™ User's Guide for MSP430™ User's Guide* (SLAU157)
6. *MSP430 Hardware Tools User's Guide* (SLAU278)

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