

# **OMAP3530/25/15/03, DM3730/25, AM3715/03 CBB, CBC and CUS reflow profiles**

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*Catalog Processors*

## **ABSTRACT**

Reflow profiles are dependent on numerous factors including package type, number of components, board layers, board size, reflow oven accuracy and process and more.

Because of the number of variables, it is not possible to provide a single reflow profile that is representative of every board using a specific package type. Typically, manufacturing houses have reflow profiles in place and modify them for specific hardware.

The reflow profiles in this application report are provided as a reference to assist customers and manufacturing houses in customizing the reflow profile to specific hardware for the package type indicated. Therefore, the information provided is not considered a final reflow profile.

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## **Contents**

1	Optimized Reflow Profiles .....	2
2	Reference Reflow Profiles .....	3
3	References .....	3

## **Trademarks**

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## 1 Optimized Reflow Profiles

For optimal reflow results in achieving consistent solder joint geometries the reflow profile should be developed in cooperation with the solder paste supplier and with the equipment supplier as needed. The solder paste vendor's datasheet includes recommendation for reflow profiles based on alloy melting temperatures and flux activity. These recommendations must be followed to achieve optimal flux activity resulting in wetting of the lead surface. The flux activity in the solder paste plays an important role in facilitating solder wetting resulting in consistent solder joint geometries.

In the event SnPb or Sn lead finish are compared to NiPdAu solder joint geometries, be aware there are distinct but acceptable different solder joint geometries for NiPdAu lead finish. For more information, see [Evaluation of nickel/palladium/gold-finished surface-mount integrated circuits](#) and [Factors that influence side-wetting performance on IC terminals](#).

### 1.1 Maximum Reflow Temperature

The maximum allowed reflow temperature is stated on the Moisture Sensitivity Label (MSL). The following provides a detailed MSL explanation.

The maximum allowed reflow solder temperature is specified for Pb-free and non Pb-free soldering per the international Standard JEDEC 020D.1. The standard can be downloaded from the [JEDEC Standards & Documents Search](#).

This standard describes the Temperature versus Time maximum for a reflow profile used in Pb-free and non Pb-free soldering. These conditions are used also for the package qualification tests and are intended to be referenced as the allowable reflow profile ranges for device level qualification testing and not a recommendation for solderability. Older packages may have used earlier versions of the JEDEC 020 standard that are grandfathered (considered acceptable). The allowed maximum reflow peak temperature is listed on the device MSL label on the tape and reel. Sometimes multiple values may be given indicating different humidity exposure levels and with associated processing temperature.

## 2 Reference Reflow Profiles

The reflow profiles shown in [Table 1](#) are provided as reference when working with a manufacturing house to generate a final reflow profile specific to the hardware using the specified package type. This information is provided for reference only and should not be used as the final reflow profile. Final reflow profiles must be worked out between the customer and manufacturing house.

**Table 1. Reference Reflow Profiles for CBB and CBC Package Types**

	Pre-Heat Temperature (°C)	Pre-Heat Dwell Time (sec)	Time above Liquid (sec)	Peak Reflow Temperature (°C)	Duration at Peak Reflow Temperature (sec)	Cool Down Rate (°C/sec)	Conveyor Speed (cm/min)
CBB (12x12 mm, 0.4 mm, top - 0.5 mm)/ CBP (12x12 mm, 0.4 mm, top - 0.5 mm) CBP (12x12 mm, 0.4 mm, top - 0.5 mm)/ CBP (12x12 mm, 0.4 mm, top - 0.5 mm)	165-185	60-120	30-60	250	10	8	50
CBC (14x14 mm, 0.5 mm, top - 0.65 mm)	60-120	10	30-60	250	20	8	What ever is required to accomplish desired reflow profile
CUS (16x16 mm, 0.65 mm)	150 ±10	90 ±30	30-60	245-250	10	8	What ever is required to accomplish desired reflow profile

## 3 References

- Texas Instruments: [Evaluation of nickel/palladium/gold-finished surface-mount integrated circuits](#)
- Texas Instruments: [Factors that influence side-wetting performance on IC terminals](#)
- [JEDEC](#)
- [JEDEC Standards & Documents Search](#)
- Texas Instruments: [nFBGA packaging](#)
- Texas Instruments: [Shelf-life evaluation of lead-free component finishes](#)
- Texas Instruments: [A nickel-palladium-gold integrated circuit lead finish and its potential for solder-joint embrittlement](#)
- Texas Instruments: [Evaluation of nickel/palladium-finished ICs with lead-free solder alloys](#)
- Texas Instruments: [MicroStar BGA packaging reference guide](#)
- Texas Instruments: [MSL ratings and reflow profiles](#)

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