Active Output Impedance for ADSL Line Drivers

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ABSTRACT

Signal termination is very common in bidirectional communication systems. Termination allows for receiving signals while transmitting different signals at the same time. With the increasing popularity of asymmetrical digital subscriber lines (ADSL), the requirement for a low power line driver amplifier combined with line termination becomes a very difficult goal. This application note examines the line driver amplifier requirements of an ADSL system and how to utilize active impedance to obtain low power dissipation. Actual lab measurements with a THS6032 line driver are discussed. Additionally, the receiver amplifier circuit requirements and the system's noise requirements are discussed with a THS6062 low-noise amplifier used as an example.

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1 Introduction

The exceptional bidirectional data transmission rates over traditional telephone lines are a major factor for the widespread industry growth of ADSL. Everyone becomes excited at the fact that data can be transmitted at up to 8 MBPS over an existing infrastructure of copper telephone lines with limited costs. There are several key components within the ADSL system, but this paper deals solely with the line driver amplifiers and the line-receiver amplifiers.

The difficult problem is that since ADSL is considered to be a full-duplex system, able to transmit and receive at the same time, a receiver must be incorporated into the design. The most common way of accomplishing this is to use a hybrid network. The hybrid's function is to cancel out the transmit signal while still being capable of receiving the signals from the customer−premise equipment (CPE) end (a.k.a. remote-terminal end—RT). A traditional transmit and receive circuit utilizing a simple resistive hybrid consisting of the R-2R network around the receiver amplifiers (such as the THS6062 low-noise amplifier) is shown in Figure 1.

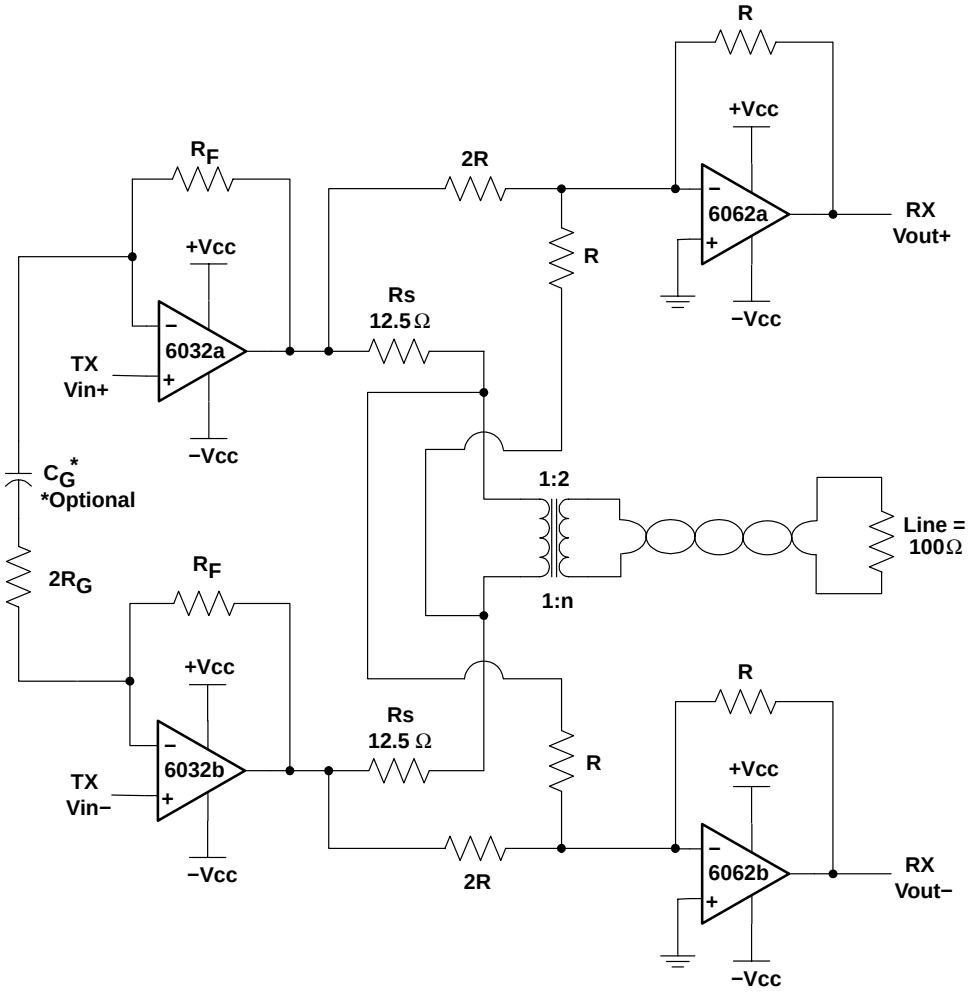

Figure 1. Traditional ADSL Analog Front-End

Each series-matching resistor (R_S) should be equal to one-half the total reflected transmission line impedance to properly match the line (see equation 1).

$$R_S = \frac{R_{LINE}}{2\,n^2} \quad (1)$$

Where n is the transformer ratio indicated as 1:n

Using R_S allows the transmitted signal to be effectively cancelled out by the R−2R matching and out-of-phase signals (discussed in greater detail in Section 4 of this document). The problem with using the series-matching resistor (R_S) is that the voltage appearing at the transformer primary side is one-half the voltage developed at the line driver amplifier output. This problem becomes apparent in Section 2.1 of this document.

2 Traditional Line Driver Requirements

ANSI T1.413 specifies that the Central-Office (CO) can transmit up to nominally –40 dBm/Hz on a 100-Ω telephone line from approximately 25 kHz to 1.104 MHz. This corresponds to roughly 3.16 Vrms (or 20 dBm) being transmitted on the line. Almost any amplifier can easily accomplish this kind of output voltage. But, the problem is that ANSI T1.413 also dictates a bit-error rate (BER) of $1x10^{-7}$. In order to accomplish this feat the ADSL signal must have a peak-to-rms ratio, also known as crest factor (CF), of about 5.6 (15 dB). This number varies from 5.3 to over 6, depending on the manufacturer and the system involved. Taking the crest factor into account, the line voltage must now have a peak voltage of about 17.7 V_{PK} (34.4 V_{PP}).

This is a very large voltage swing that most amplifiers available cannot produce. This is a key reason for using a transformer and two amplifiers configured differentially to drive the line. Differential circuits have several advantages over single-ended configurations. This includes minimizing common mode signals and interference, improvement of power-supply rejection, and the obvious advantage of doubling the voltage swing that appears at the transformer leads. Another advantage of the differential configuration is that even-order harmonics can be reduced by as much as 20 dB, resulting in a low distortion amplifier system.

2.1 Amplifier Output Voltages

In order to meet the line requirements, first calculate the amplifier's output voltages. Take the 17.7 V_{PK} line requirement and transfer it to the primary of the transformer, which is $17.7 \div n = 17.7 \div 2 = 8.85\ V_{PK}$. Because a differential drive configuration is used, each amplifier only needs to produce one-half the voltage, or $8.85\ V_{PK} \div 2 = 4.43\ V_{PK}$. But, due to the voltage drop from the series-matching resistors (R_S), the output voltage must be doubled from 4.43 V_{PK} to 8.85 V_{PK}. Figure 2 illustrates these voltages on the simplified line driver schematic.

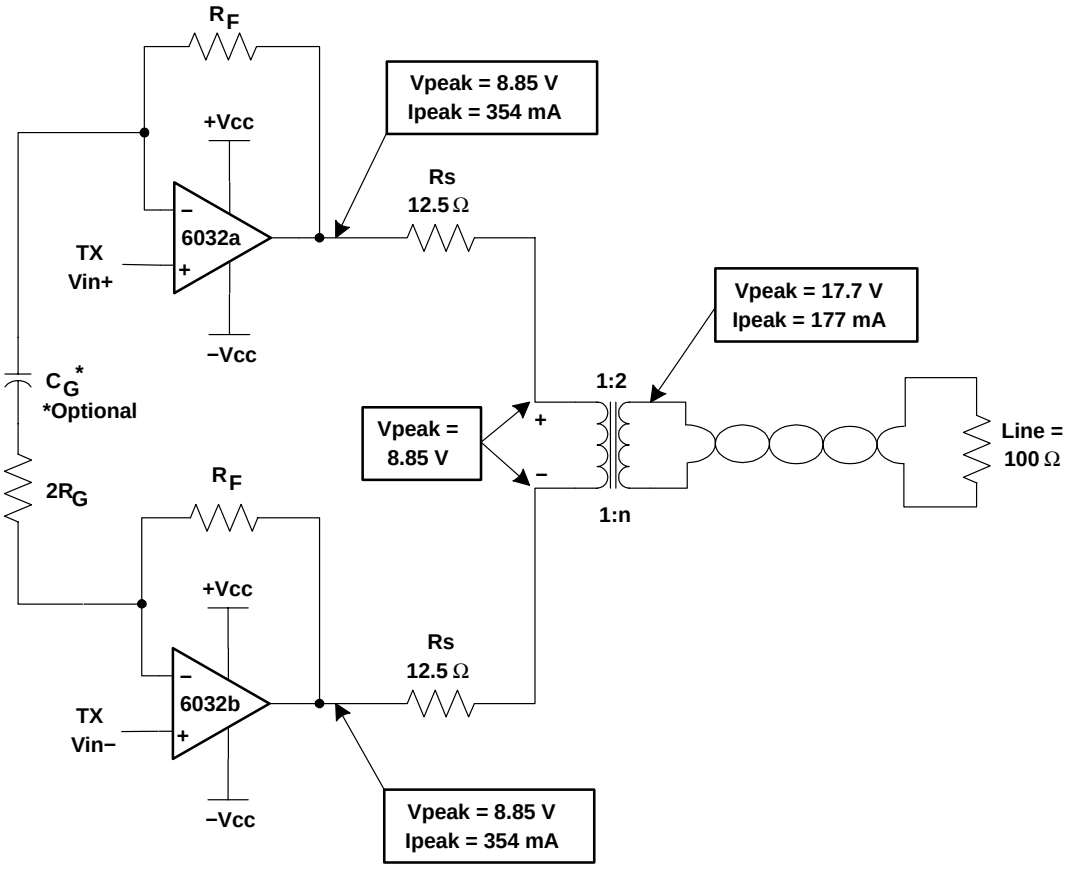

Figure 2. Line Driver Voltage and Current Levels to Meet ANSI T1.413 Requirements

Because R_S forces the amplifier to swing twice the transformer voltage requirement, the power supplies (±Vcc) must be increased accordingly. This increase in power supply voltage leads to the number one issue with ADSL line drivers—power dissipation.

2.2 Line Driver Power Dissipation

Power dissipation in the line driver amplifier dominates CO applications. Take an approximation at the power dissipation levels required for the traditional line driver circuit. Assume that the amplifier requires at least 3 V of power supply voltage headroom (i.e., $Vout_{max}$ = Vcc – 3 V and there is a 10% tolerance on the power supply). Since power is based on the RMS output voltage and the average current consumption of the amplifiers, this leads to the following approximation:

$$P_{DISS} = \left[2 \times \left(Vcc – Vout_{rms}\right) \times Iout_{rms} \times 0.8^{\dagger}\right] + P_{QUIESCENT} \quad (2)$$

† The ADSL signal is considered to have a Gaussian distribution. Because of this, multiplying the amplifier's RMS output current by approximately 0.8 yields the average current drawn from the power supply due to the amplifier's output signal current.

$$P_{QUIESCENT} \approx 4 \times VCC \times ICC \times 0.7 \text{ (see Note)} \quad (3)$$

Let : $Vcc \approx Vout_{max} + V_{HEADROOM} + V_{CC\ TOLERANCE} = 8.85\ V + 3\ V + 1.5\ V$

$= 13.35\ V \rightarrow 15\ V_{DC}$

$Vout_{RMS} = 8.85\ V_{PK} \div 5.6 = 1.58\ V_{RMS}$

$Iout_{RMS} = 354\ mA_{PK} \div 5.6 = 63.2\ mA_{RMS}$

$Icc = 12\ mA_{DC}$

$\therefore P_{DISS} \approx 1.35\ W + 0.5\ W \approx 1.85\ W$

NOTE: This multiplication factor accounts for the fact that part of the quiescent current in a Class-AB amplifier gets diverted to the load when there is a signal appearing at the output of the amplifier driving a load. The number chosen is only an approximation and is only shown as a reference. Typical numbers range from 0.4 to 0.9 and are based on numerous circuit parameters, both internal and external to the amplifier.

This 1.85 W is a lot of power for a single device to dissipate. To compound the problem, there are typically as many as 64 ADSL lines on a single PCB. This is *a lot* of heat to dissipate while trying to maintain proper silicon die temperatures.

Looking at equation 2, there are several items that account for the power dissipation. If there were a way to minimize some of the terms, then the power dissipation problem is reduced. Some things that could lower the power dissipation are lower quiescent currents (Icc) and lower power supply voltages (Vcc). But, in order to meet the distortion characteristics of an ADSL signal, quiescent currents typically cannot be lowered without distortion becoming an issue.

Additionally, a very tight tolerance is specified on the power supply, the power supply voltages cannot be lowered too much—or else clipping and distortion occurs prematurely. This is the key problem with having such a large crest factor. The power supply voltage needs to be high enough to pass the signal's peak voltage without causing distortion, yet the RMS voltage is very small. This creates a large RMS voltage difference in the output stage yielding a lot of power dissipation.

But, what if there was a way to lower the amplifier's output voltage while still meeting all of the line power requirements? Additionally, the customer premise equipment (CPE) signals must be received at the same time. This is a lot to ask for, but it can be done.

2.3 Minimizing Power Dissipation

Power reduction is easily accomplished by reducing the series-matching resistors (R_S) to a much smaller value. The voltage drop across these resistors is then minimized. The amplifier output voltage is reduced by the same amount, and that allows the power supply voltages to be reduced. Because the voltage difference between the power supply voltage and the RMS output voltage is reduced, power dissipation is also reduced. Additionally, the quiescent power is reduced due to the power supply voltages dropping. Using the previous example, the amount of power that is saved by simply utilizing a smaller resistor is:

Let New R_S = 13% of original R_S value

New $Vout_{max}$ = 1.13 X Old $Vout_{max} \div 2 = 5$ V

New Vcc = 5 V + 3 V +0.9 V ≈ 9 V

New $Vout_{rms} = 5\ V \div 5.6 = 0.893$ V

New $Iout_{rms}$ = Old $Iout_{rms}$ = 63.2 mA

$\therefore$New $P_{DISS} \approx 0.82\ W + 0.3\ W \approx 1.12\ W$

This is a savings of 0.73 W, or 40%, per ADSL channel. When there are several channels on a single PCB, this can add up to substantial heat savings. The die temperature is also reduced, allowing for better performance and longer life of the amplifier.

But, what this configuration fails to do is allow for proper line impedance matching. When the load impedance being presented to the line is equal to the line's characteristic impedance, then the maximum amount of power is transferred from the source into the load. The maximum energy transfer occurs when the load impedance is matched perfectly to the characteristic impedance of the line {$Z_{LOAD} = Z_{LINE} = \sqrt{(L/C)}$}. T1.417 issue 2 stipulates that the nominal termination impedance is resistive with a resistance of 100 Ω for an ADSL system. Additionally, the return loss is a minimum of 35 dB from 10-kHz to 2-MHz corresponding to a termination impedance of 100 Ω ± 3.5 Ω.

In reality the transmission line is very complex due to the nature of the existing infrastructure of the plain old telephone system (POTS). But the T1.417 standard does stipulate that the goal for the impedance looking through the transformer into the line driver amplifiers is optimally 100 Ω. To get the best of both worlds, utilizing small series resistors (R_S) and matching the line impedance, an *old* circuit configuration can be utilized—the active termination circuit (a.k.a. synthesized impedance).

2.4 Active Termination

Active termination has been around for several years, references [1][2][3]. The idea is to use a small value resistor for the series resistance (R_S). The circuit then utilizes positive feedback to make the impedance of this resistor, when looking from the line-side, appear much larger. This accomplishes two things:

1. A very small resistance when the line driver amplifier transmits signals to the line.
2. Proper matching impedance when looking from the line to the amplifier.

But, most of the original designs were single-ended applications instead of the differential configuration used in ADSL systems.

Taking the general idea a step further, the signals from each amplifier are 180° out-of-phase from each other in the differential system. These signals are connected to the traditional inverting node on the amplifier (– input) instead of the noninverting node (+ input) used in the single-ended application. The advantages of this are:

1. The positive feedback resistance and voltage gain do not dictate the impedance looking into the noninverting node.
2. Cross coupling of the signals is achieved when creating active impedance. Cross coupling helps minimize differences between the two amplifier output signals. Figure 3 shows the basic circuit for differential positive feedback.

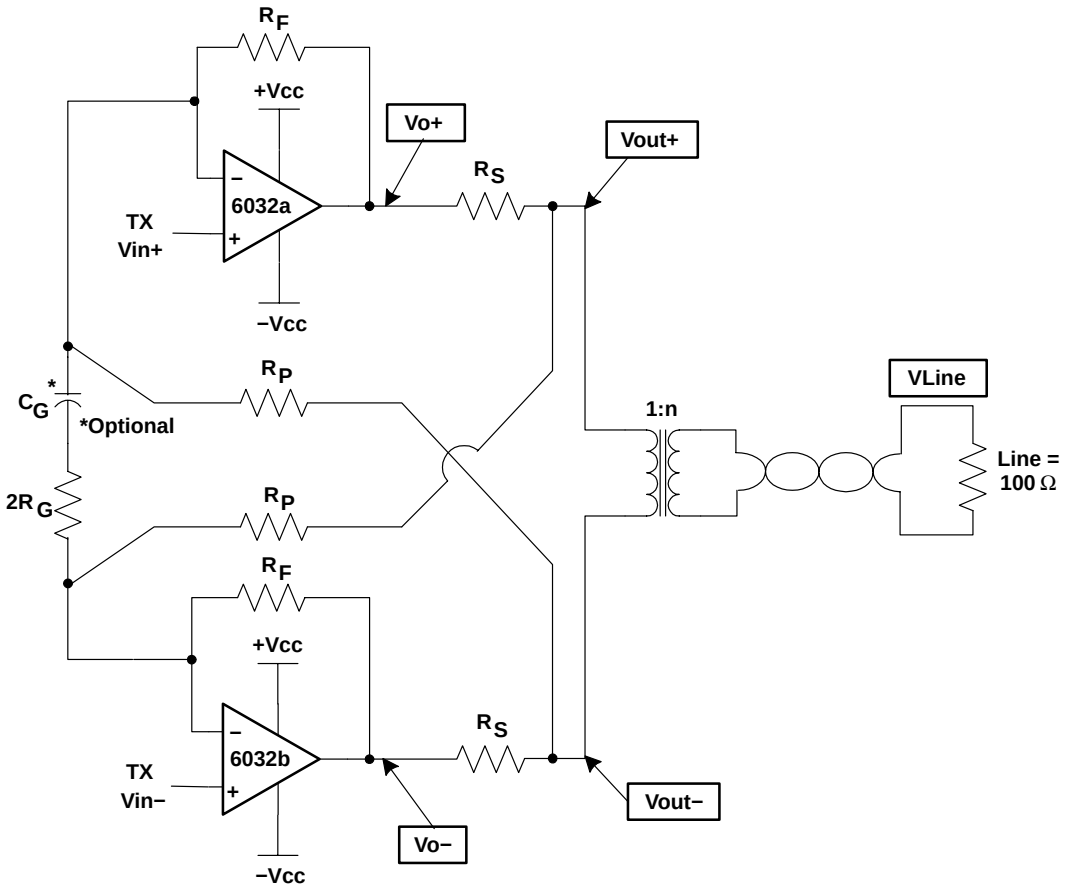

Figure 3. Basic Active Impedance Circuit

The first thing to look at is how the circuit creates a larger impedance than what is actually placed there by the resistor R_S. Assuming the TX inputs are grounded and a voltage is applied at Vout−, this creates a voltage at V_{o+} equal to (Vout− × $-R_F / R_P$). Since the voltage at Vout+ is equal to –Vout−, then V_{o+} = (Vout+ × R_F / R_P). This makes resistor R_S appear to be a larger impedance (Z) by the following formula:

$$Z(\Omega) = \frac{R_S}{1 - \frac{R_F}{R_P}} \tag{4}$$

The important thing to consider is that regardless of the forward gain from Vin to Vo, the active impedance (Z) value remains constant. The drawback to this arrangement is that the impedance changes at frequencies near the amplifier's bandwidth limit. The amplifier must have a high enough bandwidth so as to not alter the impedance at the frequencies of interest. For ADSL, this implies that the amplifier must have good characteristics from 25 kHz to 1.1 MHz. As a rule of thumb, the amplifier must have a minimum bandwidth of 20 times the maximum operating frequency, or at least 22 MHz with the amplifier's intended gain.

2.5 Active Impedance Forward Gain

Now that the return impedance is corrected, the rest of the design parameters need to be considered. The most fundamental is the forward voltage gain from input to output. For simplicity, assume that the amplifier is well within its linear range and bandwidth effects can be ignored. Equation 5 shows the simplified forward gain from Vin to Vo, and equation 6 shows a closer approximation to the actual circuit. For the readers who love circuit analysis, the derivation of these formulas is shown in Appendix A.

$$A_V = \frac{V_O \pm}{V_{in} \pm} = \frac{1 + \left(\frac{R_F}{R_G \| R_P}\right)}{1 - \left(\frac{R_F}{R_P}\right)\left(\frac{R_L}{R_L + R_S}\right)} \text{ iff } R_L << R_P \tag{5}$$

OR

$$A_V = \frac{V_O \pm}{V_{in} \pm} = \frac{1 + \left(\frac{R_F}{R_G \| R_P}\right)}{1 - \left(\frac{R_F}{R_P}\right)\left(\frac{R_L \| R_P}{R_L \| R_P + R_S}\right)} \tag{6}$$

where: (7)

$$R_L = \frac{R_{LINE}}{2\,n^2}$$

A lot of variables are coming into these equations. To reduce the headaches, concentrate on the first approximation shown in equation 5. Appendix B shows the full system equation and its derivation, but is ignored in the main context due to the complexity of the equations. Initially, simplify equation 5 to make it easier to use.

In the original circuit (the classic design shown in Figure 1), R_S equaled the true terminating resistance—R_L. Now, choose R_S as a percentage of R_L in the active termination circuit. Using the variable X as this percentage, where $0<X\leq 1$, and realizing that the term $\frac{R_L}{R_L + R_S}$ is held constant, make several substitutions. The first sets of assumptions are:

$$R_S = R_L X \tag{8}$$

$$\frac{R_L}{R_L + R_S} = \frac{1}{1 + X} \text{ where } 0 < X \leq 1 \tag{9}$$

Assume that the active impedance (Z) is equal to the terminating resistance (R_L). Equation 4 is manipulated to achieve the following:

$$R_P = R_F\left(\frac{1}{1-X}\right) = \frac{R_F}{1-X} \text{ where } 0 < X \leq 1 \tag{10}$$

Equation 10 shows that to properly match the active termination impedance, the value of R_F can be arbitrarily selected. Using the substitutions of equations 8 to 10 into equation 5 leads to the simplified forward voltage gain of:

$$A_V = \frac{R_G[(1 + X)(2 - X)] + R_F(1 + X)}{2R_G X} \text{ where } 0 < X \leq 1 \text{ and } R_L << R_P \quad (11)$$

If the system forward gain is known, equation 11 can be solved for the gain resistance—R_G:

$$R_G = \frac{R_F(1 + X)}{2A_V X - [(1 + X)(2 - X)]} \text{ where } 0 < X \leq 1 \text{ and } R_L << R_P \quad (12)$$

2.6 Minimum Active Impedance Forward Gain Design Constraint

Because active impedance utilizes positive feedback, it is possible to create negative impedance instead of positive impedance. Negative impedance sometimes has its uses, but not within an ADSL circuit. So, there must always be positive impedance. This can only be accomplished by using equation 4 or equation 10. Utilizing these equations along with equation 5, a design constraint is established for the active termination circuit. There must be a minimum forward gain for the system to work properly. Failure to do this results in a system that creates negative impedance and does not work properly.

Because the line must be matched properly, R_F is first chosen arbitrarily. Equation 10 then dictates a specific fixed value for R_P. This leads to R_G solely dictating the forward voltage gain for any given value of X (which is tied to R_S). The minimum forward voltage gain allowed is when R_G is not even in the system. This leads to:

$$AV_{MIN} = \frac{2 + X - X^2}{2X} = \frac{(1 + X)(2 - X)}{2X} \text{ where } 0 < X \leq 1 \text{ and } R_L << R_P \quad (13)$$

Clearly the minimum forward gain is solely dependent on the value chosen for the series resistance (R_S). As R_S (or X) decreases, the minimum gain increases as illustrated in Figure 4.

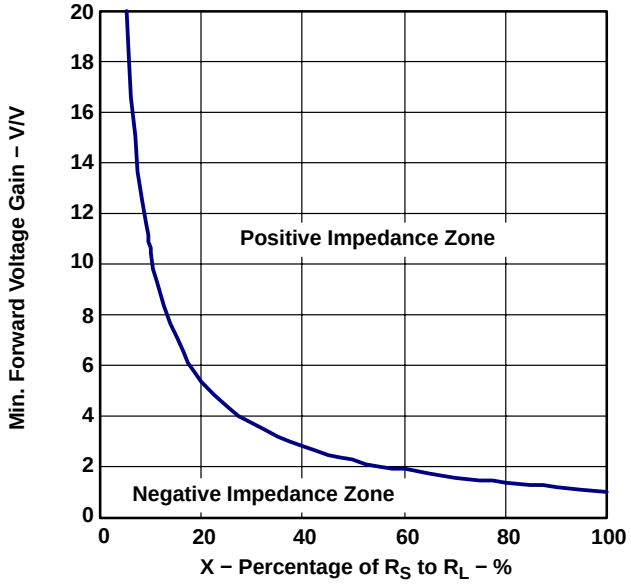

Figure 4. Minimum Forward Voltage Gain

Luckily, for most ADSL systems, the gain of the amplifiers is typically greater than 10 V/V. Meeting the minimum gain requirement is usually not an obstacle as long as the value of X is greater than about 10%. But, there is a possibility that the required gain from Vin to Vout is less than the minimum even without R_G in the system. Under this scenario, there are a few options:

- Place a voltage divider at the amplifier inputs.
- Increase X.

Or

- Decrease the transformer ratio that requires a larger amplifier gain.

As long as the minimum forward gain is met, then the low-power active termination system works properly.

2.7 Line Impedance Changes

Up until now, we have assumed that the line was a fixed value (usually 100 Ω). But in reality, the line impedance is highly complex. Typically the line impedance can range from as low as 50 Ω up to as high as 300 Ω over the ADSL frequency spectrum. This line impedance becomes reflected back through the transformer as dictated by equation 7. Since the positive feedback is placed between the series resistor (R_S) and the line impedance (R_L), then the forward voltage gain is affected. The question is by how much, and does this lead to other issues?

Looking at equation 5, the only reference to the reflected line impedance is in the denominator. Keeping everything else constant and increasing only variable R_L decreases the denominator. An increase in forward voltage gain (A_V) results due to this increase. A top-level assessment shows that this is a good thing because it tries to maintain a proper power level onto the line. Since the impedance increased, the voltage must also increase to try and compensate. But, there is a limit to how much voltage the amplifier can produce based on a given power supply voltage.

To quantify the exact change in forward voltage gain, the variable Y is introduced. Let the variable Y equal the percent change in the reflected line impedance (R_L). This leads to the new forward voltage gain:

$$A_V = \frac{R_G[(2-X)(1+X+Y)] + R_F(1+X+Y)}{R_G X(2+Y)} \quad (14)$$

where $0 < X \leq 1$; $R_L << R_P$; Y is the % change of R_L

Figure 5 illustrates the percent change in forward gain with varying values of X. The forward gain with a 100-Ω line impedance is used as the baseline for comparison.

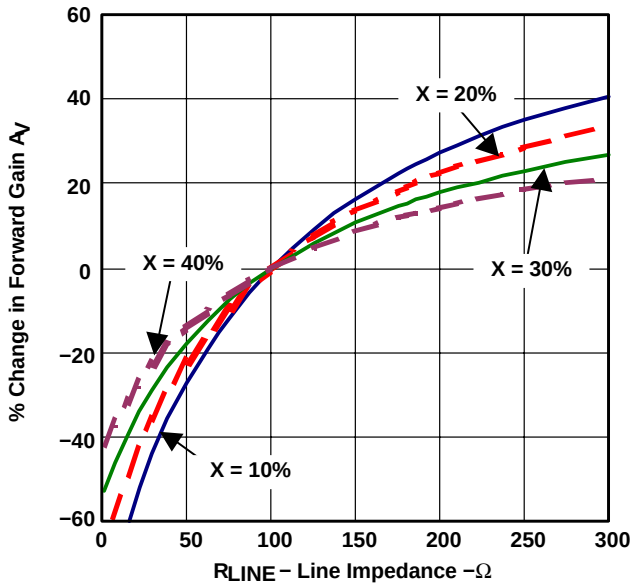

Figure 5. Forward Gain Change With Varying Line Impedance

In general, the change in forward gain is directly proportional to the line impedance (R_L). Depending on the value of X chosen (the series resistance R_S) the forward voltage gain can change quite a lot. It is interesting to note that the change in percentage gain is independent of transformer ratio (n), feedback resistance (R_F), gain resistance (R_G), and the initial amplifier gain (A_V).

The minimum forward gain also varies with the line impedance. Attention must be paid to meet the minimum forward gain or negative impedance may be created. The minimum forward gain becomes:

$$Av_{MIN} = \frac{(2 - X)\,(1 + X + Y)}{X(2 + Y)} \tag{15}$$

where $0 < X \leq 1$; $R_L << R_P$; Y is the % change of R_L

Figure 6 illustrates the minimum forward gain with varying line impedance.

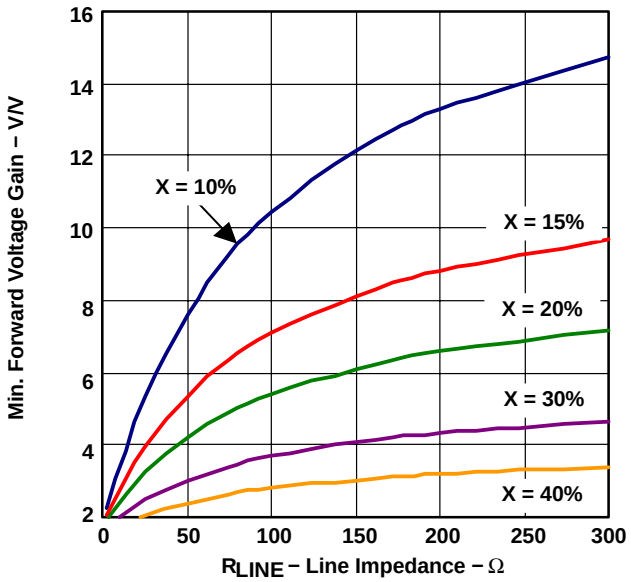

Figure 6. Minimum Forward Gain Change With Varying Line Impedance

Figure 6 tracks the percentage change shown in Figure 5. When designing an active termination system, it does not matter what initial-design line impedance is used. As long as the minimum gain criterion is met, the system should not create negative impedances.

2.8 Line Impedance Changes and the Amplifier Output Voltage

Forward voltage gain changing ±20 % can be quite common in a real system and must be accounted for. If not, the input signal can be amplified too high and clipping could easily occur. Excess distortion, data transfer rate, line reach, and even power dissipation could become worse if the line impedance is not handled properly within the active impedance circuit design.

Examining the circuit of Figure 3 and using equation 7 in calculation, shows how the line impedance changes the amplifier's output voltage. Assume that the series resistance (R_S) is designed for a 100-Ω system and is held constant. Also assume that the power on the line was done with a 100-Ω line impedance and is 20 dBm. This corresponds to a line voltage of 3.162 V_{RMS}. The formula used to find the corresponding amplifier voltages are:

$$Vo_{RMS} = \frac{V_{LINE_{RMS}}\left(R_{LINE} + 2n^2R_S\right)}{2\,nR_{LINE}} \tag{16}$$

$$Vo_{PEAK} = Vo_{RMS} \times \textit{CrestFactor} \tag{17}$$

The important number is the peak output voltage of the amplifier because a given supply voltage determines how much voltage swing can occur. Failure to plan for varying line impedances can cause some serious problems. Figure 7 and Figure 8 illustrate this issue with some common values for X (R_S) and a crest factor of 5.3.

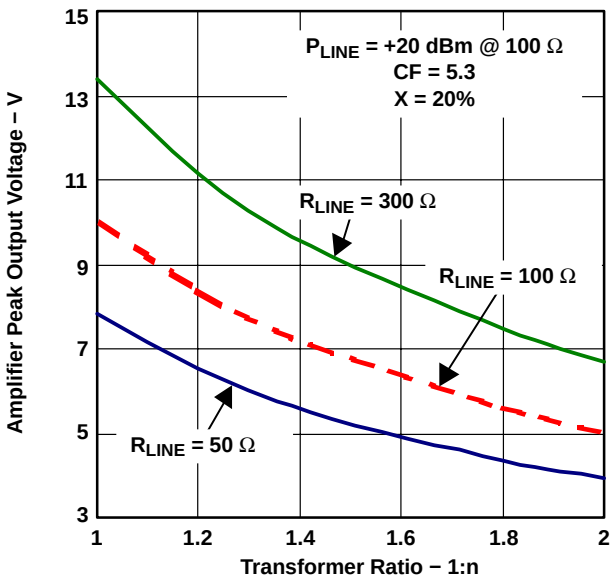

Figure 7. Amplifier Peak Output Voltage With X = 20%

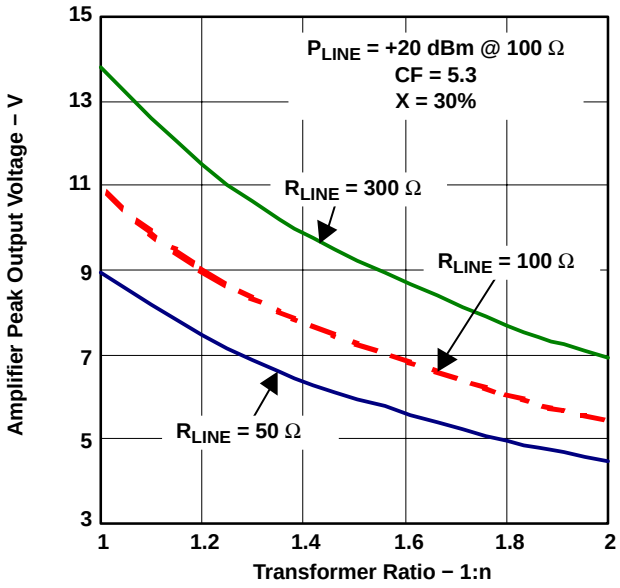

Figure 8. Amplifier Peak Output Voltage With X = 30%

Obviously, as the crest factor increases, the peak output voltage also increases. The other important thing to notice is when the series resistor (R_S) increases, the amplifier output voltage also increases. The obvious question is why not use the smallest resistance possible? There are several reasons for this that are explained in detail in Section 3 of this document.

2.9 Line Impedance Changes and the Power on the Line

If the amplifiers' gain changes and the line impedance changes, how is the power on the line affected? Also, how does it compare to the traditional passive circuit design? This can be answered by using equation 18. As before, assume the circuit was designed for a 100-Ω line impedance and the gain was set such that there is 20 dBm on the line:

$$V_{LINE_{RMS}} = \frac{2nR_{LINE}\, Vo_{RMS}(1 + \%A_V\, Change)}{R_{LINE} + 2n^2 R_S} \quad (18)$$

V_{ORMS} is the amplifier RMS output voltage with 100-Ω line, 20 dBm line power; and $\%A_V$ change is derived from equation 14.

To better understand this, Figure 9 shows the results of equation 18 against the line impedance:

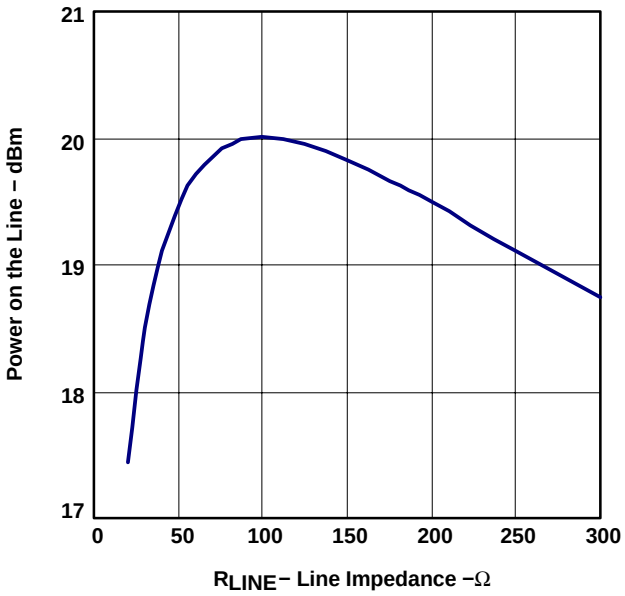

Figure 9. Power on the Line With Varying Line Impedance

The interesting thing to note is that regardless of the series resistor (R_S or X) or the transformer ratio, the power on the line conforms to the same graph. This is also true for the traditional design where there is no active impedance and the amplifier output voltage remains fixed over the line impedance change. The bottom line is that the active impedance design performs exactly the same as the traditional design when it comes to power delivered to the line.

2.10 General Conclusions—Introduction and System Requirements

Meeting the line signal requirements of ANSI T1.413, along with meeting the proper line termination requirements, can cause some serious power dissipation problems. Using active termination gives the designer the capability to reduce power levels by 0.73 W (40%) or more per ADSL port. The use of simplified equations allows for a quick system design as long as the minimum forward voltage gain of the system is met. The other obstacle is that most telephone lines are not considered an optimal medium to transfer high-speed data due to the variable characteristic impedance of the lines. Following the simple formulas and knowledge of the interaction between the line impedance and the line driver output voltage ensures that the active impedance line driver system performs as intended. But, there still remains the question of how do the formulas work in a real system. Section 3 tests the theories and gives some general ideas on how to create a low-power active termination line driver.

3 Lab Tests

All of the equations derived in Section 2 look great on paper. But, does the active impedance system really work in the lab? To help answer this question a THS6032 high-speed amplifier was used to drive a 100-Ω resistive line. An ADSL signal was synthesized with an arbitrary waveform generator. Different transformer ratios were tested along with varying resistor values to help understand the entire active impedance configuration (Appendix C shows the values used in the tests). As a bonus, the THS6032 can be used with the classic Class-AB mode output stage or with a Class-G mode output stage. Power dissipation figures were obtained to see the effects of the more efficient Class-G operation compared to the Class-AB operation.

3.1 Lab Test Setup and the Transformers

The first test examines how the resistor values affect the system. Because the THS6032, like most ADSL line drivers, is a current feedback (CFB) amplifier, the feedback resistance (R_F) dictates the bandwidth and the stability of the amplifier. The THS6032 can easily achieve a bandwidth of over 50 MHz with gains ranging from +6 V/V to +13 V/V (depending on the value of R_S and the transformer ratio).

The issue here is that transformers are very complex circuits consisting of RLGC circuits. Most ADSL transformers exhibit a resonance peak anywhere from 30 MHz to 150 MHz. This resonance can cause serious issues with the system; especially the active impedance configuration where feedback is pulled from the node between R_S and the transformer leads. The traditional configuration may not have such issues due to the *large* series resistance isolating the amplifier from the complex transformer load. Figure 10 shows line reflected impedance of several ADSL transformers with a 100-Ω resistor on the secondary. See Appendix C for the transformers used for the lab tests. The graph simulates the impedance the amplifier must drive into.

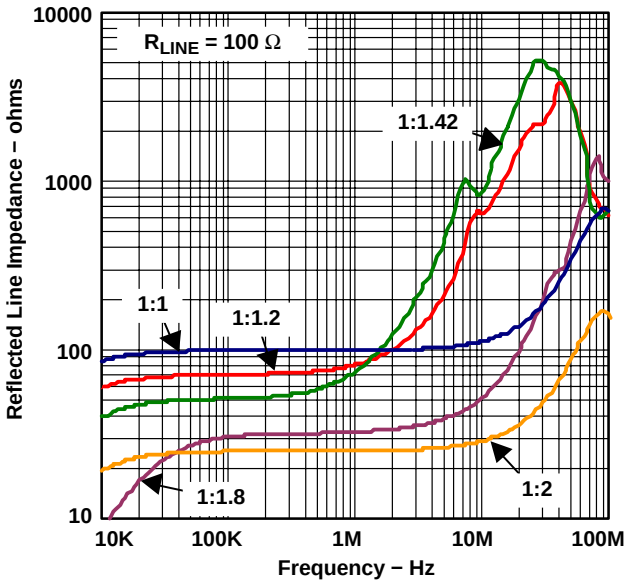

Figure 10. Reflected Line Impedance Load Presented to the Line Driver

This figure (graph) shows that the 1:1.42 transformer has a resonance peak impedance of 5 kΩ occurring at 30-MHz. This is a very complex load for a high-speed amplifier to drive. As Section 2 pointed out, varying the effective line impedance (RL) alters the minimum forward gain requirement. It also affects the forward voltage gain and ultimately the amplifier's output voltage amplitude. The graphs only showed a line up to 300 Ω. Here we see that the impedance can be as much as 5 kΩ. The transformer effects can significantly impact the performance of the line driver system. It is quite easy for the amplifier to exhibit a small oscillation at this resonance frequency. Even though the ADSL system is limited to 1.1-MHz, this high frequency oscillation can cause issues with line reach, increased distortion, and even an increase in power dissipation. The other transformers used may also cause issues with the line driver amplifiers, but probably to a lesser degree than the 1:1.42 transformer.

One way to combat this problem is to add a snubber network, aka zoebel network, consisting of a resistor (R_{SNUB}) and a capacitor ($C_{SNUB)}$ across the transformers' primary leads. At high frequencies, where the transformer's impedance becomes very high at its resonance frequency (ex: 5 kΩ at 30 MHz), the snubber network provides a resistive load to the circuit. The value for R_{SNUB} should initially be set to the impedance presented by the transformer within its pass-band. An example of this would be to use a 100-Ω resistor for a 1:1 transformer or a 25-Ω resistor for a 1:2 transformer. The value for C_{SNUB} should be chosen such that the −3 dB frequency is about 5 times less than the resonance frequency. For example, if the resonance frequency is at 30 MHz, the impedance of C_{SNUB} should be equal to R_{SNUB} at 6 MHz. This leads to a value of $C_{SNUB} = 1/2(2\pi f R_{SNUB})$, or approximately 530 pF. This should only be used as a starting point. The final values will be dictated by actual circuit testing. The lab testing done for this report did not utilize the snubber network to keep the system simple, with as little component count as possible.

Remember that the feedback resistance controls the bandwidth of a CFB amplifier. If the bandwidth of the amplifier is limited by utilizing this control functionality properly, then the effects of the transformer's resonance point are minimized. To see the effects of this control, a test was set up to see how the amount of feedback resistance contributes to power dissipation and distortion. The distortion test used was the multitone power ratio (MTPR) test, otherwise known as the empty bin test. This test causes the amplifier to transmit all tones from 160 kHz to 1104 kHz at equal amplitudes in the frequency domain except for one tone. The amplitude of this missing tone is created by the system's distortion. A perfect system would not show any amplitude in this location. The amplitude of the system was adjusted such that 20 dBm appeared at the line with a 100-Ω load.

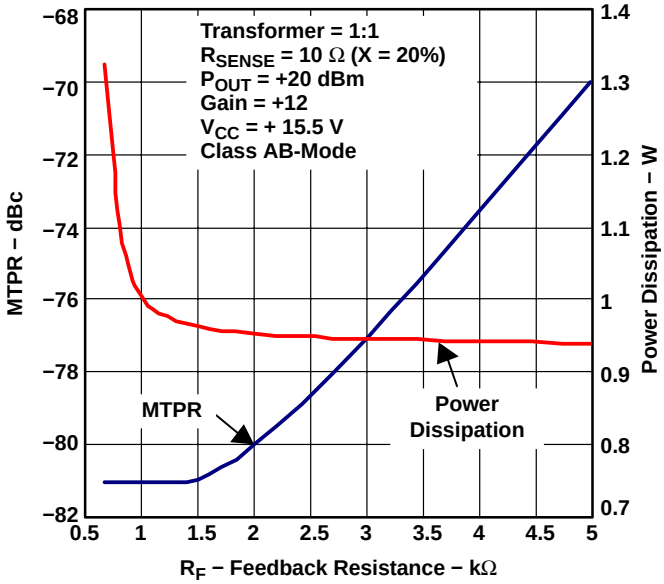

Figure 11. Effects of Feedback Resistance on Power Dissipation and MTPR

Figure 11 clearly shows that increasing the bandwidth (by reducing the feedback resistance) on the THS6032 too much can cause an increase in power dissipation. But, there is very little distortion in the system at the same time. These two issues need to be balanced in the system. For the remainder of the tests, the feedback resistance was kept at 1150 Ω. This appeared to be a reasonable value based on Figure 11. The amount of distortion ANSI−T1.413 allows is equal to (3N + 20), where N is the number of bits. For a 14-bit system, which most ADSL systems are currently utilizing, the distortion needs to be better than –62 dBc. Using 1150 Ω with a MTPR of –81 dBc results in a very clean system with a long line reach.

Now that the feedback resistance is selected, the rest of the system component values are easily calculated with the previous equations from Section 2. The only other variable was that the gain of each amplifier was set to approximately +12 V/V. This allowed the use of testing the X=10% system, where the appropriate minimum gain requirement was about 10.5. As the series resistance (R_S) was increased, the gain also had to be increased to account for the additional voltage drop from the added series resistance.

3.2 Lab Tests—The Active Impedance Test

The first thing examined was the active impedance looking from the line, through the transformer, and into the amplifier. This was done to prove the impedance looking from the line into amplifier was at the proper value. The traditional configuration with a fixed R_S was compared to see the effects of using active termination. As stated earlier, the active termination relies on the amplifier to create the synthesized impedance. As the frequency increases, the amplifier reaches its bandwidth limit and the impedance into the amplifier does not hold true anymore.

The traditional approach has to deal with the fact that it also relies on the amplifier to create the virtual ground. Since the output impedance of an operational amplifier increases with frequency, so too should the impedance of the traditional configuration increase with frequency. Figure 12 shows the impedance looking from the line into the line driver circuitry with a 1:1.2 transformer.

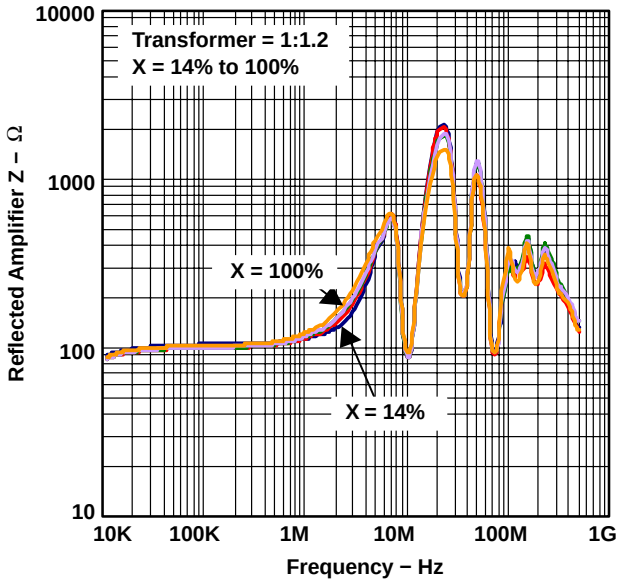

Figure 12. Impedance Looking From the Line Into the Transformer

As Figure 12 indicates, it really does not matter whether there is active impedance or real resistance. The results are essentially the same. Looking at the ADSL frequency spectrum from 25 kHz to 1.1 MHz, the impedance matches the 100-Ω line very well for all cases. This should not present any problems as far as line matching is concerned. This also holds true regardless of the transformer ratio utilized in the system. Each transformer's own high frequency characteristics dominate the apparent input impedance.

Figure 13 shows the impedance looking into R_S after the transformer (from the line side). Because the effects of the amplifier's bandwidth limits were not seen, as far as impedance is concerned, this test should show the amplifier's anticipated impedance results.

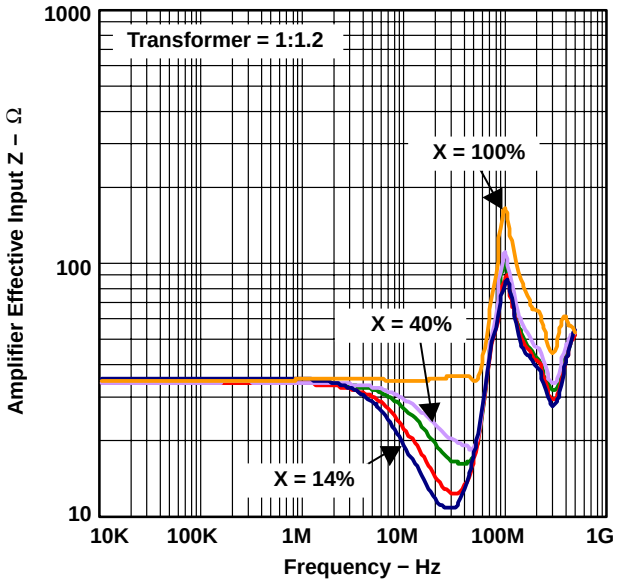

Figure 13. Impedance Looking Into the Sense Resistor—R_S With 1:1.2 Transformer

Figure 13 clearly shows the amplifier's closed-loop bandwidth effects. Remember that the amplifier creates the active impedance based on equation 4. If the amplifier cannot perform properly, the signal at the amplifier's output does not hold true anymore and the impedance starts dropping. As the series resistance (R_S) increases, the effects of the impedance drop should become minimized due to the amount of real resistance used. Eventually the amplifiers own output impedance takes over regardless of the termination system used. It is at this point the impedance is out of the designer's control. Since the ADSL spectrum is well-controlled then the system meets its designated functionality as a low power line driver.

Figure 14 and Figure 15 show us how a change in transformer ratio affects the impedance looking into the amplifier.

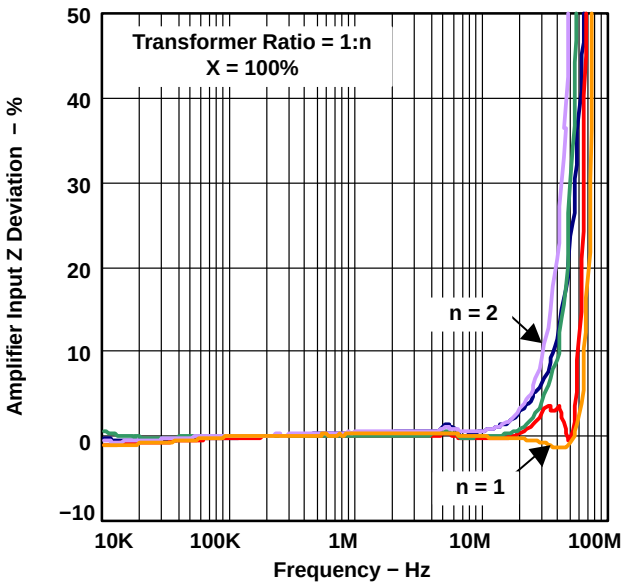

Figure 14. Impedance Deviation Looking Into the Sense Resistor (R_S) With Varying Transformer Ratios—X = 100%

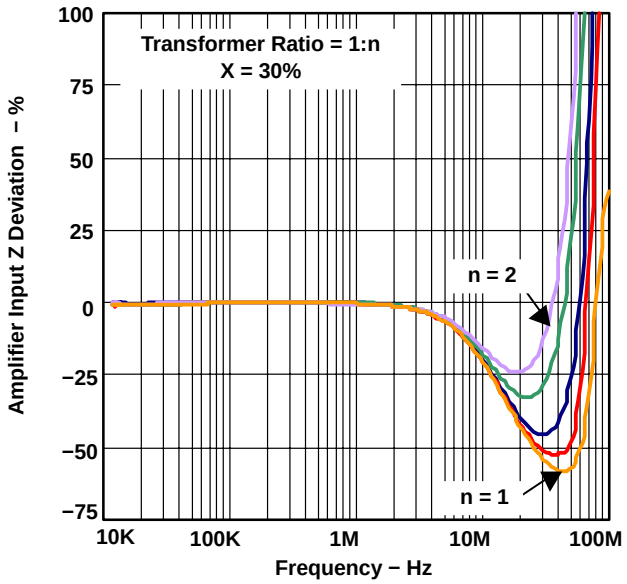

Figure 15. Impedance Deviation Looking Into the Sense Resistor (R_S) With Varying Transformer Ratios—X = 30%

Within the ADSL spectrum, there is no difference in transformer ratios regardless of the system employed. As expected, the X=100% data indicates a very flat response until the amplifiers' bandwidth limits are reached. Additionally, when active impedance is used, the percentage deviation from the expected results also follows the amplifiers' bandwidth limits. There appears to be a larger deviation above 10 MHz when the transformer ratio is decreased. This is attributed mainly due to the fact that R_S increases as the transformer ratio (n) decreases. The frequency where the amplifier's output impedance equals R_S moves higher in frequency as n is decreasing. Thus, more percentage deviation should occur with the lower transformer ratios.

One area of concern with using active impedance is that lightning surge tests could overwhelm the amplifiers' internal circuitry and cause failures due to a decreased real resistance between the amplifier and the transformer. The larger the resistance, the better the chance that no damage will occur within the amplifier. If the active impedance configuration is utilized, then the series resistance (R_S) should be a *respectable value* and not something trivial (example: <5% of R_L). Most systems should strive for a value of 20% to 30% of R_L. This allows for respectable power savings and a decent amount of isolation from surges on the line. Another reason for a respectable series resistor value becomes evident in the following sections.

3.3 Lab Tests—Power Dissipation and Power Supply Voltage

Now comes the most anticipated part of the lab tests, power dissipation. This is the key reason for even considering active termination. Because power dissipation is vitally important to active termination, a lot of data is shown in this area. This is done so that some general conclusions can be drawn on what is considered the best way to set up the active termination circuit.

Figure 3 shows the general circuit configuration used along with fixed 100-Ω line impedance. Because the line impedance is a 100-Ω resistor, the issues with respect to variable line impedance are not a concern. In fact, the power dissipation could be optimized for a given test configuration. As a result, the power dissipation numbers shown should be considered optimum for a particular test setup. When varying line impedance is thrown into the mix, the power supply voltages need to be adjusted accordingly and the power dissipation changes.

The other factor which hampers the power dissipation is that the THS6032 requires 4 V of headroom from the power supplies. This is due to the Class-G architecture requiring multiple series transistors in the output stage. If a very low headroom amplifier were used (such as the THS6132 or THS6182) the power supply voltage could be reduced. But, the reduced efficiency of the Class-AB output stage could offset the benefits of a lower headroom amplifier. Obviously there are trade-offs that need to be addressed in amplifier selection.

Figure 16 shows the minimum power supply ($\pm V_{CC-H}$) required for the THS6032. The figure (graph) also shows the power supply voltage requirements for different crest factor signals.

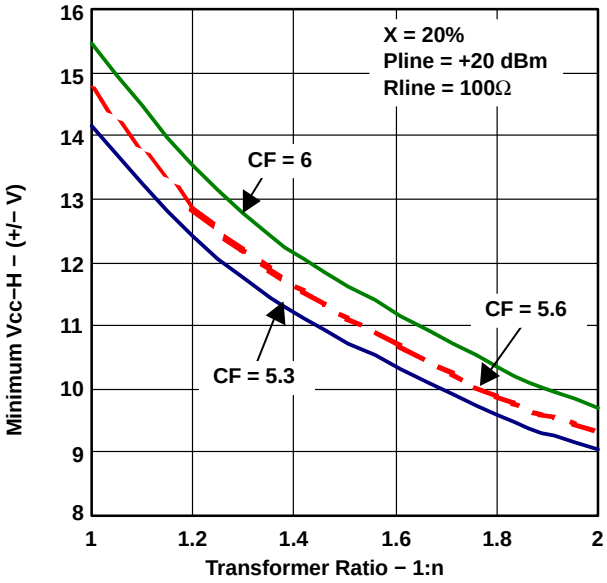

Figure 16. Minimum Power Supply Voltage for Use With the THS6032

The lab testing used fixed line impedance. As such, using a 1:1 transformer could be used with good results if required. But, knowing that the line impedance varies in a real system, using a 1:1.2 transformer with the THS6032 yields a system that can drive a 300−Ω line with a crest factor of 5.3 (based on the results of Figure 7). If a larger crest factor is to be used or a larger series resistance R_S, then using a 1:1.42 transformer may be required due to the power supply limitations of the amplifier.

3.4 Lab Tests—Power Dissipation and Distortion With a 1:1.2 Transformer

As a reference for the active termination testing, a THS6032 was tested using the traditional configuration shown in Figure 1. To really see the effects of the Class-G circuitry in action, Figure 17 shows how changing the V_{CC-L} supply voltages alter the power dissipation. For reference, it also shows the power consumed in each set of supplies. In Class-AB mode, power dissipation is about 1.8 W. But, in Class-G mode operation, the best power achieved is approximately 1.35 W with V_{CC-L} at ±6V. The MTPR numbers were –70 dBc for Class-AB operation and –68 dBc with Class-G operation.

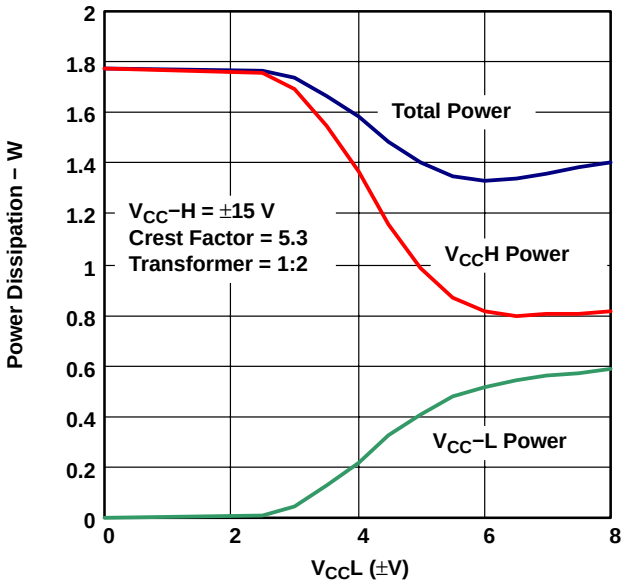

Figure 17. Traditional Circuit Design Power Dissipation Results

The first set of data from the active termination system shows the power dissipation results when using a 1:1.2 transformer. Figure 18 shows how the crest factor affects power dissipation when setting X to 20% (Rs = 6.94 Ω). The power supply voltage was chosen to give additional ±0.5 V headroom for design margin. In the lab, the supplies could be set ±1 V lower before clipping started to occur. But, this is not considered good practice, as power supply tolerances and amplifier tolerances could come into play. Thus, the power dissipation numbers shown are considered to be realistic and within the safe operating area of the system.

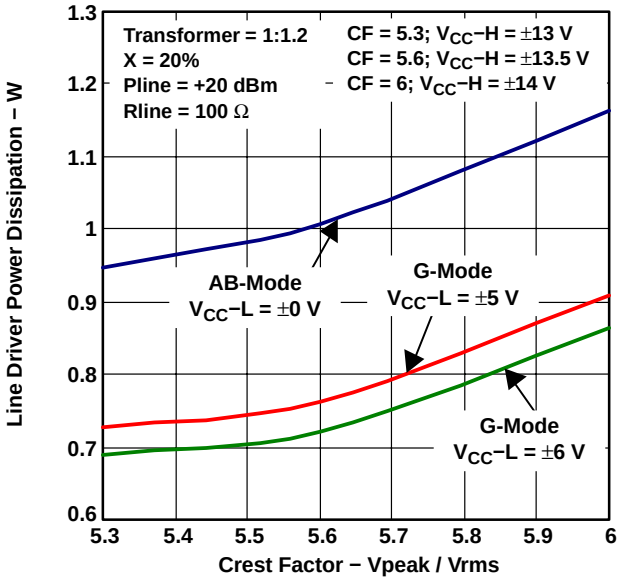

Figure 18. Power Dissipation With 1:1.2 Transformer and DIfferent Crest Factors

When compared to the traditional circuit design, the active termination circuit saves a huge 47% in power dissipation. This is true for both Class-AB operation and Class-G operation. For the active termination data, the use of Class-G operation saves an additional 20% to 25% power dissipation compared to the Class-AB operation. As expected, when the crest factor increases, the power dissipation also increased by as much as 25%. This is mainly due to the increase in power supply voltage required to handle the larger peak voltages.

Figure 19 shows the effects of changing the series resistor (R_S) has on the power dissipation. A common crest factor of 5.3 illustrates the change in the system.

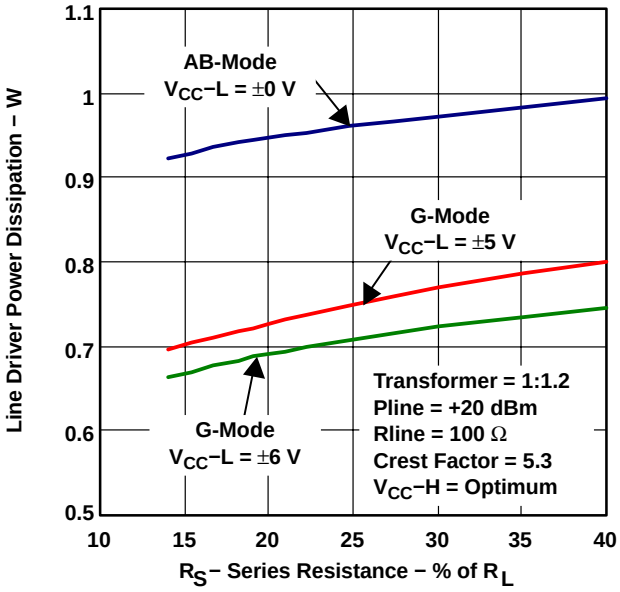

Figure 19. Power Dissipation With 1:1.2 Transformer and Varying R_S

If the power supply voltages were held constant and no clipping occurred, then the power dissipation would have decreased with an increase in R_S. But, the testing was done to show the best possible performance with a given set of component values. Thus, the power supplies were increased as R_S was increased to compensate for the increase in output voltage required from the amplifier. The power supply voltages ranged from ±12.5 V (X = 14%) to ±14 V (X=40%).

The last thing to check was the effect of MTPR distortion on the system. The same conditions used to generate Figure 19 were also used to generate Figure 20.

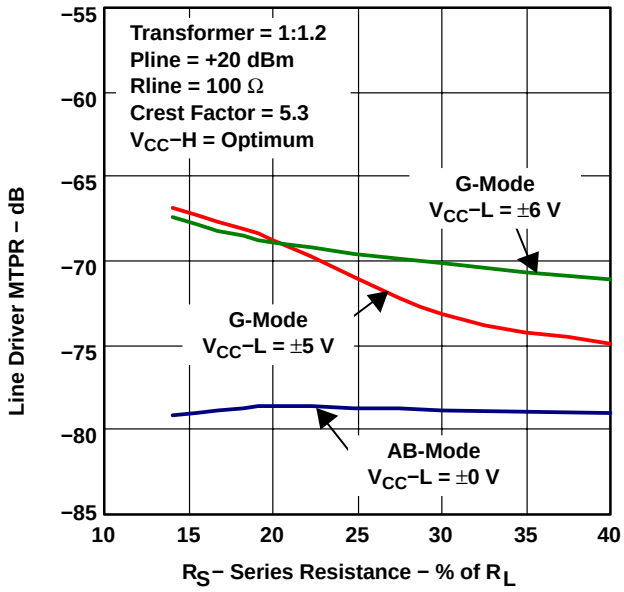

Figure 20. MTPR With 1:1.2 Transformer and Varying R_S

Figure 20 shows us that as the series resistance (R_S) increases, the MTPR distortion improves. The designer has to choose between lower distortion and lower power dissipation. As stated earlier, a series resistance of 20% to 30% should give good results for both requirements.

3.5 Lab Tests—Power Dissipation and Distortion With a 1:1.42 Transformer

The next set of tests utilized a 1:1.42 transformer instead of a 1:1.2 transformer. The test conditions were similar to the 1:1.2 transformer tests. The only difference was the power supply voltages were adjusted to yield the best power dissipation given the change in transformer ratio. Obviously, all of the resistor values needed to be updated to account for the change in the transformer ratio. Figure 21 shows the power dissipation change with crest factor using a fixed series resistor (R_S = 10 Ω).

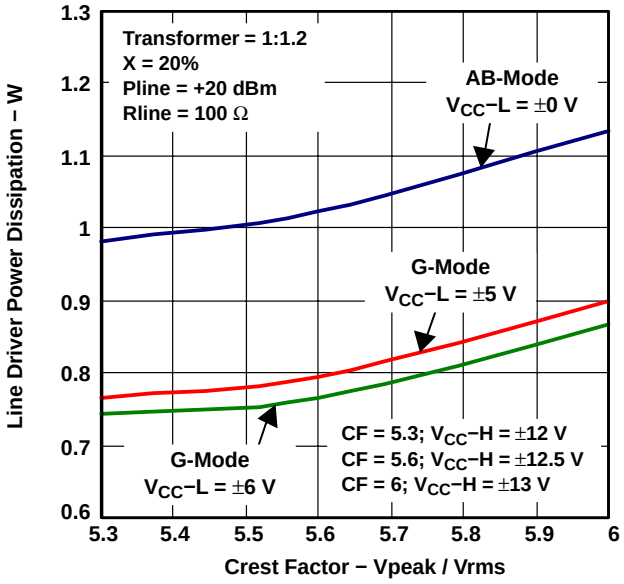

Figure 21. Power Dissipation With 1:1.42 Transformer and Different Crest Factors

Not surprisingly, this follows the same basic shape as the 1:1.2 transformer. But, the power dissipation is generally about 5% higher. Although this test still saves about 44% more power than the traditional circuit design. Does this mean that the higher the transformer ratio, the higher the power dissipation? This is answered in the next section.

Figure 22 shows the power dissipation change with a change in series resistance (R_S). Again, a common crest factor of 5.3 was used to create these results. Figure 23 shows the MTPR performance of the system.

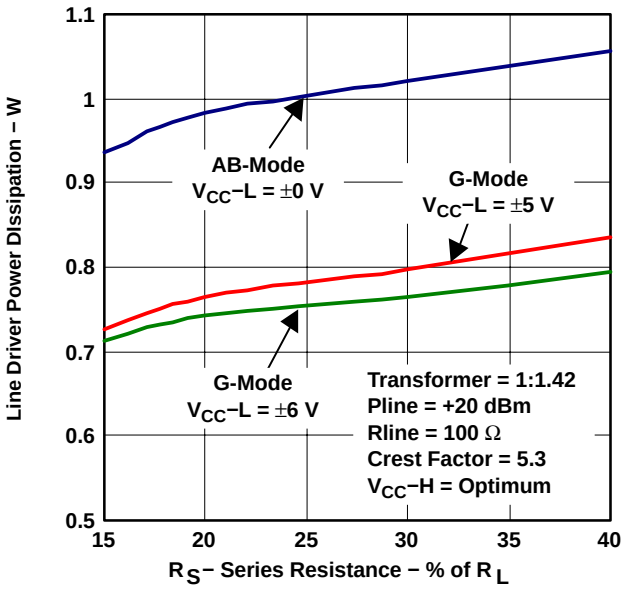

Figure 22. Power Dissipation With 1:1.42 Transformer and Varying R_S

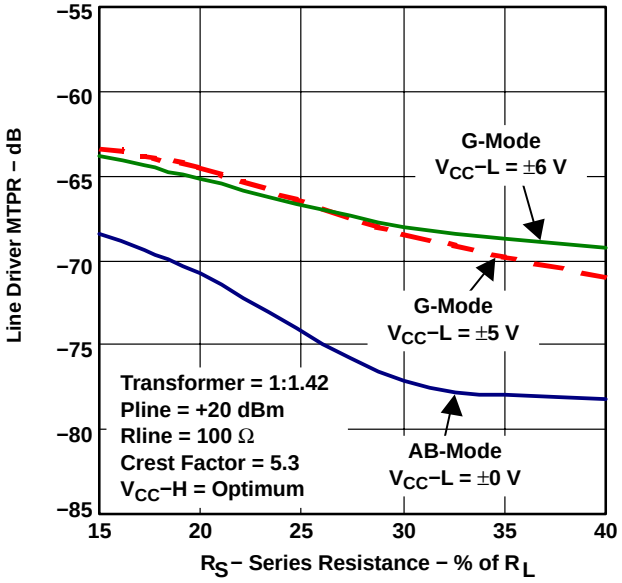

Figure 23. MTPR With 1:1.42 Transformer and Varying R_S

The power dissipation data is very similar to the 1:1.2 transformer data. Again, the power dissipation is about 5% higher than the 1:1.2 ratio system. The MTPR data is also very similar in nature to the 1:1.2 transformer system. But, the effect of a lower series resistance (R_S) shows even more distortion than before. Does this mean that MTPR distortion suffers as we start increasing the transformer ratio? This is also discussed in Section 3.7.

3.6 Lab Tests—Power Dissipation With Multiple Transformer Ratios

Power dissipation increased as the transformer ratio went from 1:1.2 to 1:1.42. The next series of tests tried to find out if there is a general relationship between the transformer ratio and the power dissipation. For each transformer ratio tested, the corresponding resistor values and power supply voltages were changed accordingly.

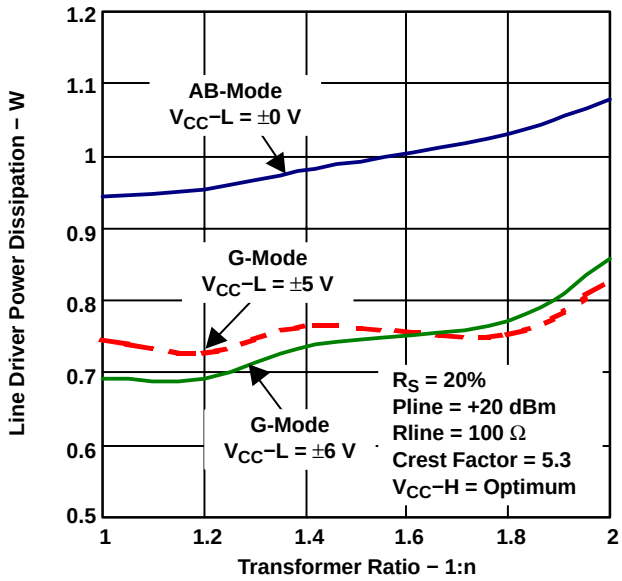

Figure 24. Power Dissipation With Varying Transformer Ratios

Figure 24 shows that in Class-AB mode operation, the power dissipation increases with the transformer ratio. One could state that the main source of power dissipation is the output current demands, but this is only partially true. The main source of power dissipation stems from the amplifier's overhead voltage requirements. Quiescent power is also a key player in the overall power dissipation. Because the THS6032 requires about 4 V of headroom, the power consumption increases as the output current, caused by the lower transformer ratio, increases. If overhead voltage could be reduced, and quiescent current reduced, then power dissipation could be minimized. Utilizing TI's new THS6182 class-AB amplifier, or the new THS6132 class-G amplifier (both of which have been optimized for low overhead voltages, and low quiescent current) power dissipation can be drastically reduced from the levels shown by the THS6032 amplifier.

The other interesting thing to note is how the power dissipation in Class-G mode operation changes. At small transformer ratios, the power dissipation is lower with a V_{CC-L} voltage of±6 V rather than the ±5-V supply. But, at high transformer ratios, a complete reversal occurs. The power dissipation is lower with a V_{CC-L} voltage of ±5 V rather than the ±6 V supply. This is expected considering how Class-G works and how the output voltage of the amplifier changes with a change in transformer ratio.

The THS6032 is a very linear Class-G amplifier. This means that there is a linear current draw transformation from each power supply (V_{CC-L} and V_{CC-H}) as the output voltage swings from 0 V to the maximum output voltage—see the THS6032 data sheet for more information on how this occurs[4]. The drawback to this linearity is a decrease in efficiency. But, low distortion is required in an ADSL line driver amplifier so trade-offs must to be made.

The reason for the Class-G power dissipation reversal occurring is the output voltage of the amplifier is reduced as the transformer ratio increases. With a V_{CC-L} of ± 5 V, the threshold of current draw from the V_{CC-L} supplies is about ± 2.5 V. Once the output voltage reaches about ±2.5 V, the current is being pulled solely from the V_{CC-H} supplies. For a V_{CC-L} of ±6 V, this occurs at about ±3.5 V (see Figure 17 which shows power drawn from V_{CC-L} starts at about ±2.5 V).

With the smaller transformer ratio, the output voltage is very large from the amplifier (±10-V peak with a CF of 5.3, 1:1 transformer, X = 20%, and a 100−Ω line). Thus, the current being pulled out of the ±6-V supplies is greater than using ±5-V supplies. At higher transformer ratios, the output voltage from the amplifier is considerably reduced (±5V peak with a CF of 5.3, 1:2 transformer, X = 20%, and a 100−Ω line). Thus, the amplifier spends more time transmitting smaller voltages. The smaller the voltage, the more the current is pulled from the smaller $V_{CC–L}$ supply. Again, the THS6032 datasheet has more information and should be referenced for further details on this phenomenon.

Figure 24 only shows what happens if the series resistance is 20% of R_L. Figure 25 through Figure 27 shows how changing R_S affects power dissipation with varying transformer ratios.

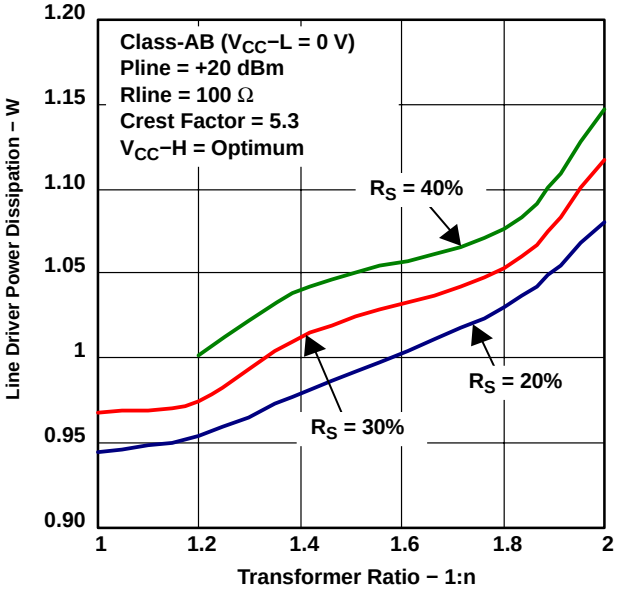

Figure 25. Class-AB Mode Power Dissipation With Varying Transformer Ratios

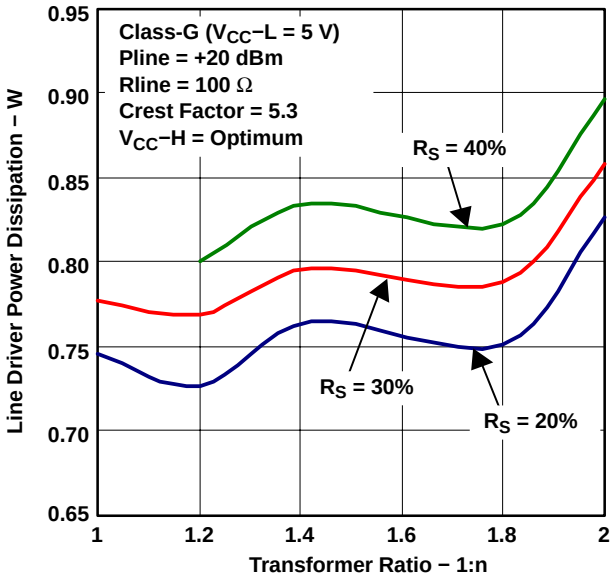

Figure 26. Class-G Mode (V_{CC-L} = ±5 V) Power Dissipation With Varying Transformer Ratios

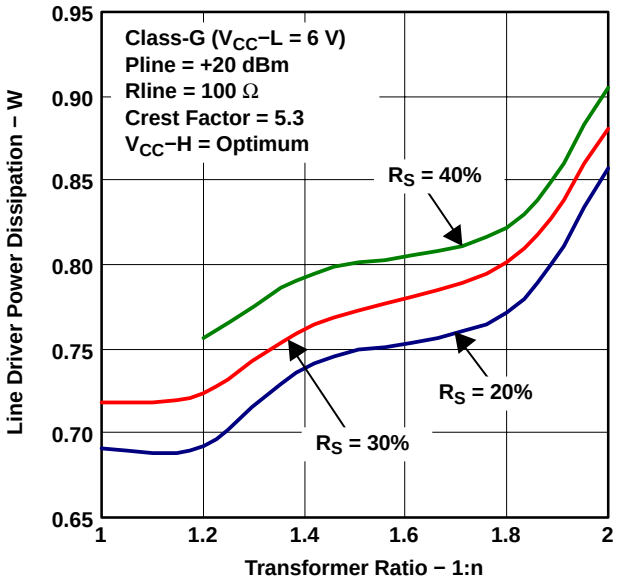

Figure 27. Class-G Mode (V_{CC-L} = ±6 V) Power Dissipation With Varying Transformer Ratios

Regardless of the power supplies and the mode of operation, as the series resistance (R_S) increases, the power dissipation increases. The final test is MTPR distortion and the effects of transformer ratio.

3.7 Lab Tests—MTPR Distortion With Multiple Transformer Ratios

Using the same setup utilized in the previous section, MTPR distortion was also recorded to see how the transformer ratio affects distortion.

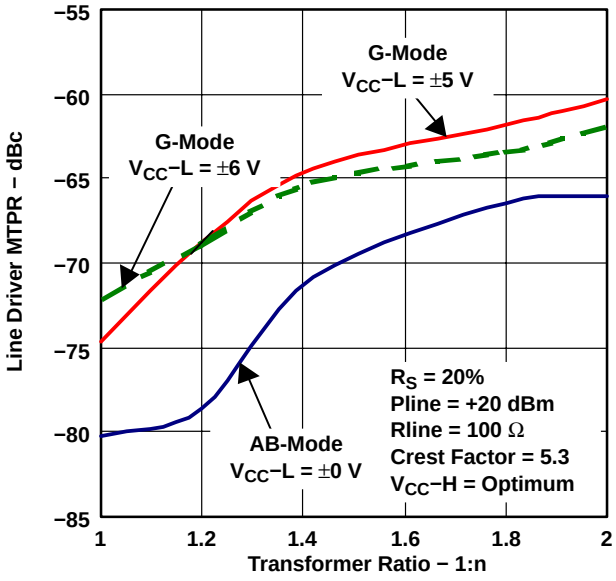

Figure 28. MTPR Distortion With Varying Transformer Ratios

Figure 28 confirms the suspicion that as the transformer ratio increases, the MTPR distortion increases. One variable that was not researched was the effects of the feedback resistance on distortion with a large transformer ratio (i.e., 1:2). It is possible that the distortion could be reduced at the higher transformer ratios using lower feedback resistors (and the corresponding resistors to match it). This increases the amplifier's bandwidth allowing for an increase in excess loop gain that reduces distortion. The drawback is that there is a possibility of an increase in power dissipation. But depending on the system, the risk may very well be worth it.

Figure 29 through Figure 31 shows the effects of the series resistance (R_S) on distortion with a changing transformer ratio.

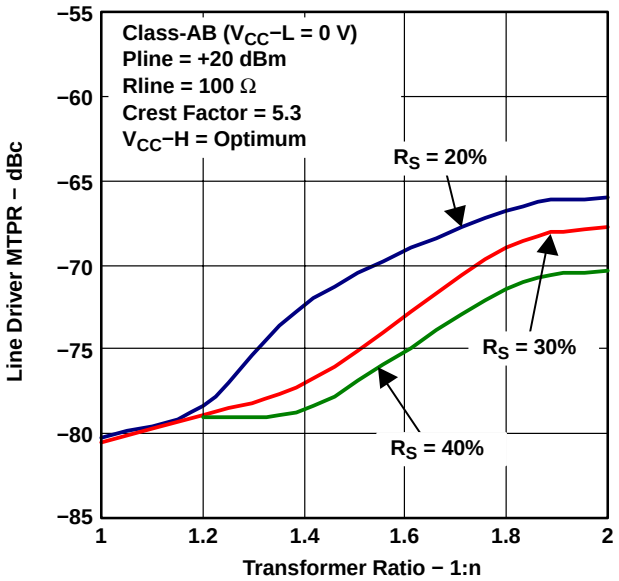

Figure 29. Class-AB Mode MTPR Distortion With Varying Transformer Ratios

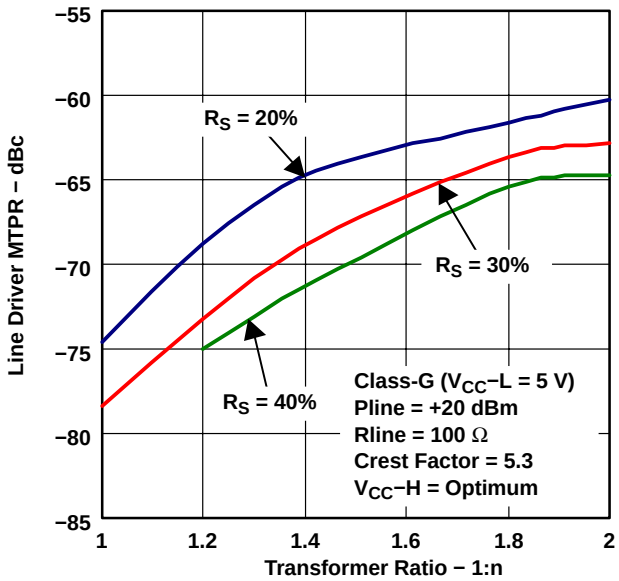

Figure 30. Class-G Mode (V_{CC-L} = ±5 V) MTPR Distortion With Varying Transformer Ratios

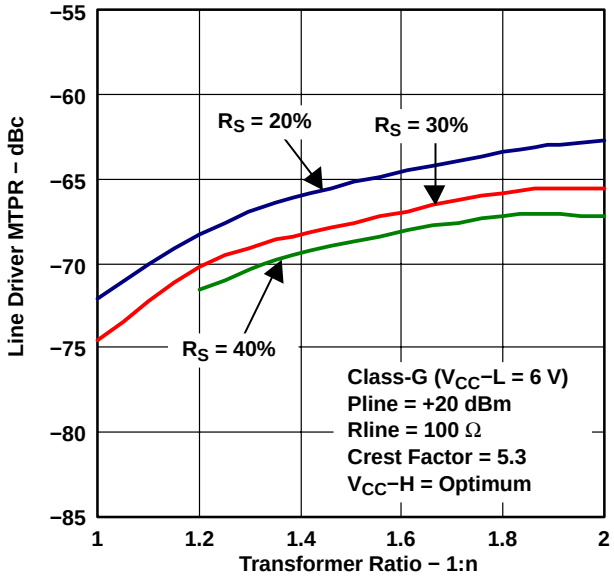

Figure 31. Class-G Mode (V_{CC-L} = ±6 V) MTPR Distortion With Varying Transformer Ratios

The data reveals that having more real physical series resistance (R_S) lowers MTPR distortion. This is because distortion in any operational amplifier gets better with an increase in load resistance. Plus, in the case of the ADSL configuration, it helps isolate the complex loading the transformer places on the amplifier. Class-AB mode typically has about 5 dB lower distortion than the Class-G modes of operation. This is due to the added transition stages internal to the THS6032 in Class-G mode operation. In Class-AB mode, there is only a transition around 0-V while Class-G has a transition around 0-V, and the $\pm(V_{CC-L} – 2.5V)$ transition area. Comparing the 1:2 transformer data with the traditional circuit design shows that MTPR performance did degrade by 4 to 5 dB. But, this also supports the idea that more real resistance between the amplifier and the transformer helps MTPR performance, but increases power dissipation.

3.8 General Conclusions—Section 3—Lab Tests

The first thing examined was the effects of the transformer on the system. Transformers are not perfect and have their own issues such as resonances and a limited frequency response. One critical area, line termination, is maintained regardless of the use of active termination or traditional termination. But, from the line driver's perspective, the transformer's resonance can cause issues and must be dealt with appropriately. As far as the impedance looking directly into the line driver, the expected results hold true as long as the frequency of operation is within the amplifier's bandwidth. Go beyond the amplifier's maximum bandwidth and the results are unpredictable.

Reduced power dissipation is the main goal for using active termination in ADSL systems. Using a 1:1.2 transformer saves 47% of power regardless of which mode the THS6032 is used in. This translates to a savings of 0.85 W with Class-AB operation and 0.63 W with optimum Class-G operation. Increasing the transformer ratio from 1:1.2 to 1:1.42 reduces the power savings, but only by a few percentage points. The data suggests that to save the most amount of power, use the smallest ratio transformer the design allows for. But, the designer must keep the output voltage requirements of the amplifier within the expected range of the line impedance variations. This is probably the key in selecting the proper transformer ratio and the power supply voltages used in the design.

The other parameter of the active termination design is the value for X (or R_S). The data suggests that the higher the real resistance placed between the amplifier and the transformer, the better the MTPR performance. Power dissipation rules also suggest using small transformer ratios. Together this translates to using the smallest transformer ratio possible with a fairly large value for X. The data shows that picking a value for X of about 0.25 gives just about everything required for the system. Again, this is also based on the variable line impedances of the intended application, the power supply voltages and the amplifier voltage headroom. Careful weighting of all these variables results in a low distortion, low power ADSL line driver. But, one important trait of the ADSL system, the receivers and noise has yet to be examined.

4 The Receiver and Noise

Everything up to this point has been primarily concerned with the transmit amplifiers and finding ways to reduce power dissipation and minimize distortion. But, one aspect that has been missing is the effect on the receiver circuitry. One can conclude that the proper line termination can be created by synthesizing larger impedance from a small resistor. But that conclusion neglects the consideration of how this would alter the signals going to the receiver amplifiers.

4.1 The Receive Signal Path—Summing Node Configuration

To help figure out how the receiver amps are affected, we must analyze the hybrid network. The purpose of the hybrid network is to eliminate (or reduce) the large signals being transmitted from the line drivers (a.k.a. line driver echo cancellation). Yet, it needs to allow reception and amplification of the very small signals from the line (which the source can be as much as 18,000 feet away). The first circuit analyzed is the summing node receiver circuit shown in Figure 32 usng the traditional termination scheme.

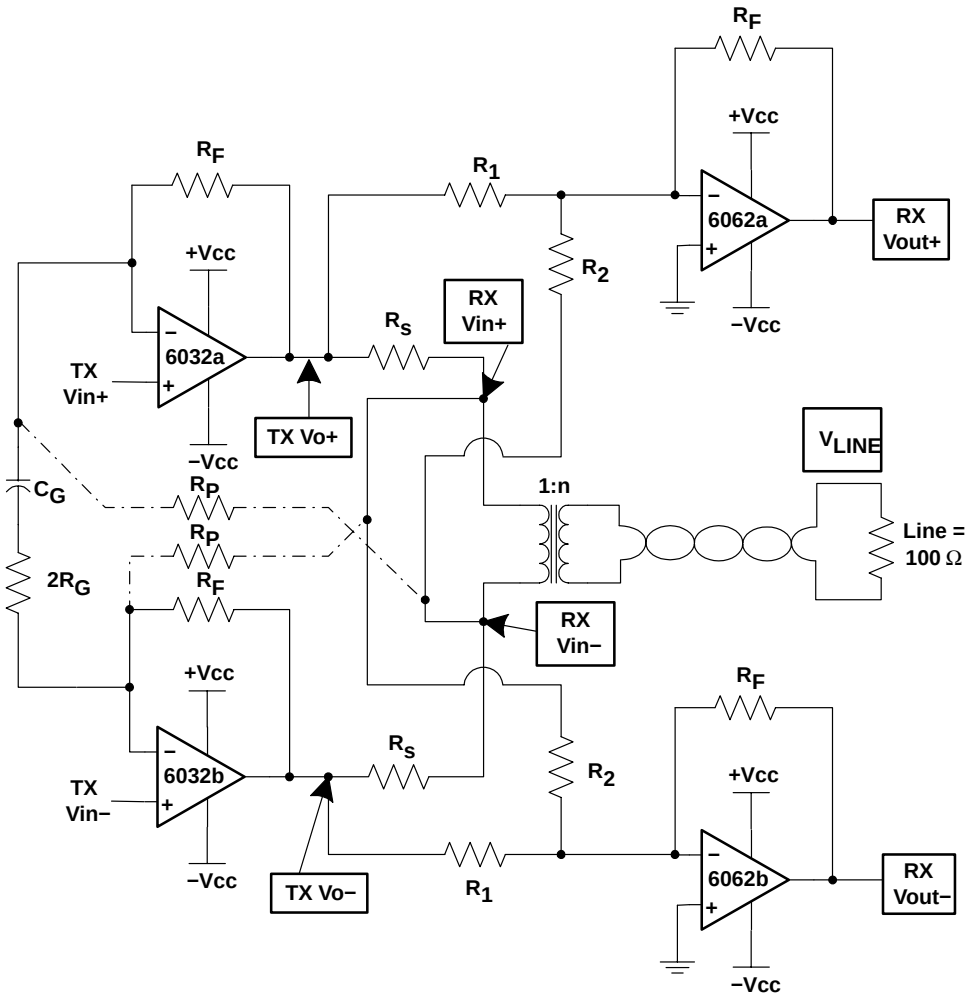

Figure 32. Summing Node Resistive Hybrid Circuit

The only concern is with one of the receiver amplifiers because the other receiver has the same results, just shifted in phase 180° from the first receiver. The first thing to do is prove that the signals from the line drivers are cancelled out. Using superposition, set the voltage on the line (V_{LINE}) to zero. If it is assumed that R_S equals the reflected line impedance (R_L), and (TX Vo+) = −(TX Vo−), then simple analysis shows:

$$\text{RX Vout+} = (\text{TX Vo+})\left(\frac{-R_F}{R_1}\right) + \frac{(\text{TX Vo}-)}{2}\left(\frac{-R_F}{R_2}\right) = 0 \text{ iff } R_1 = 2R_2 \tag{19}$$

Obviously the amount of rejection is based on the matching of the resistors and the matching of R_S to R_L. Realistic values of rejection typically range from 6dB to 20dB. Now that the line driver signals are eliminated, analyze the signals coming from the line. Again, by using superposition, assume the TX signals are zero and only analyze the line voltage coming through the transformer.

$$\text{RX Vout}+ = (\text{RX Vin}-)\left(\frac{-R_F}{R_2}\right) = (\text{RX Vin}+)\left(\frac{R_F}{R_2}\right) = \frac{V_{LINE}}{2n}\left(\frac{R_F}{R_2}\right) \tag{20}$$

These equations show how the simple hybrid works. The R_F to R_2 relationship easily controls the gain and the amount of rejection is controlled by the R_1 to R_2 relationship. In a real system, the line is complex and the transformer is also complex. In order to get good hybrid rejection, the signal appearing at resistor R_2 must be cancelled out by the signal appearing at resistor R_1. To make this happen, the hybrid tries to *simply* model the line impedance (R_L) reflected through the transformer (along with the transformer's own characteristics) by several passive components. The end result is the hybrid can become very complicated and is considered beyond the scope of this document. Instead, discussion is limited to the simple resistor hybrid.

4.2 The Receive Signal Path With Active Termination—Summing Node

So how does the active termination circuit affect the receive path? Using the same analysis above should prove helpful in answering this question. Again, using superposition we first set the line voltage signal to zero and analyze the transmit signal. Here we realize that R_S does not equal R_L. To account for this equation 19 has to be adjusted to:

$$\text{RX Vout}+ = (\text{TX Vo}+)\left(\frac{-R_F}{R_1}\right) + \frac{(\text{TX Vo}-)}{\left(R_L + R_S\right)}\left(\frac{-R_F}{R_2}\right) \tag{21}$$

Substituting equation 19 into equation 21 and knowing that (TX Vo+) = −(TX Vo−) gives:

$$\text{RX Vout}+ = \frac{(\text{TX Vo}+)}{(1 + X)}\left(\frac{R_F}{R_2}\right) - (\text{TX Vo}+)\left(\frac{R_F}{R_1}\right) \tag{22}$$

Setting equation 22 to zero yields $R_1 = [R_2 (1+X)]$ for the transmit signal rejection to occur. Using this knowledge, analyzing the line signal portion of the circuit needs to be accomplished. Using superposition set (TX Vin+) equal to zero. Due of the active termination scheme, the signal appearing at (TX Vo+) is not zero. The output of the line driver amplifier becomes:

$$\text{TX Vo}+ = \frac{V_{LINE}(1–X)}{2n} = (\text{RX Vin}+)\,(1–X) \tag{23}$$

Using the fact that R_1 must equal $[R_2 (1+X)]$ to cancel out the transmit signal and using symmetry around the active impedance circuit leads to (RX Vout+) becoming:

$$\text{RX Vout}+ = \left(\frac{V_{LINE}}{2n}\right)\left(\frac{R_F}{R_2}\right)\left(\frac{2X}{1 + X}\right) = (\text{RX Vin}+)\left(\frac{R_F}{R_2}\right)\left(\frac{2X}{1 + X}\right) \tag{24}$$

Just as before, the gain is essentially controlled by the R_F to R_2 relationship and the amount of rejection is controlled by the R_1 to R_2 relationship. But, because X is typically much less than 1 (such as 25%), the output of the receiver is considerably reduced. To overcome this disadvantage, the value of R_F must be increased by [(1+X) / 2X] to be equal to the traditional configuration voltage gain without active termination. Making the feedback resistor (R_F) higher is easy to do, but there are disadvantages to this that are covered in detail in Sections 4.4 and 4.5 of this application note.

4.3 The Receive Signal Path—Common Mode Configuration

The drawback to the summing node configuration is that it relies on the *virtual ground* to sum the currents flowing through the input resistors to cancel out. But, to keep noise minimized, the resistors must be made fairly low in impedance. The point where each resistor taps into the transmit circuit is also resistively loaded down. This can cause problems, such as altering the active feedback node voltage (especially with low transformer ratios—see Appendix B for details) and increasing the load on the line driver.

The common mode configuration helps alleviate these loading problems. This is accomplished by using the receiver amplifier in a differential configuration where the amplifier's common mode rejection minimizes the transmit signals. The added advantage of this circuit is the overall impedance of the receiver circuitry appears much higher than the impedance of the summing node configuration while using small resistors. Figure 33 shows the simple common mode configuration.

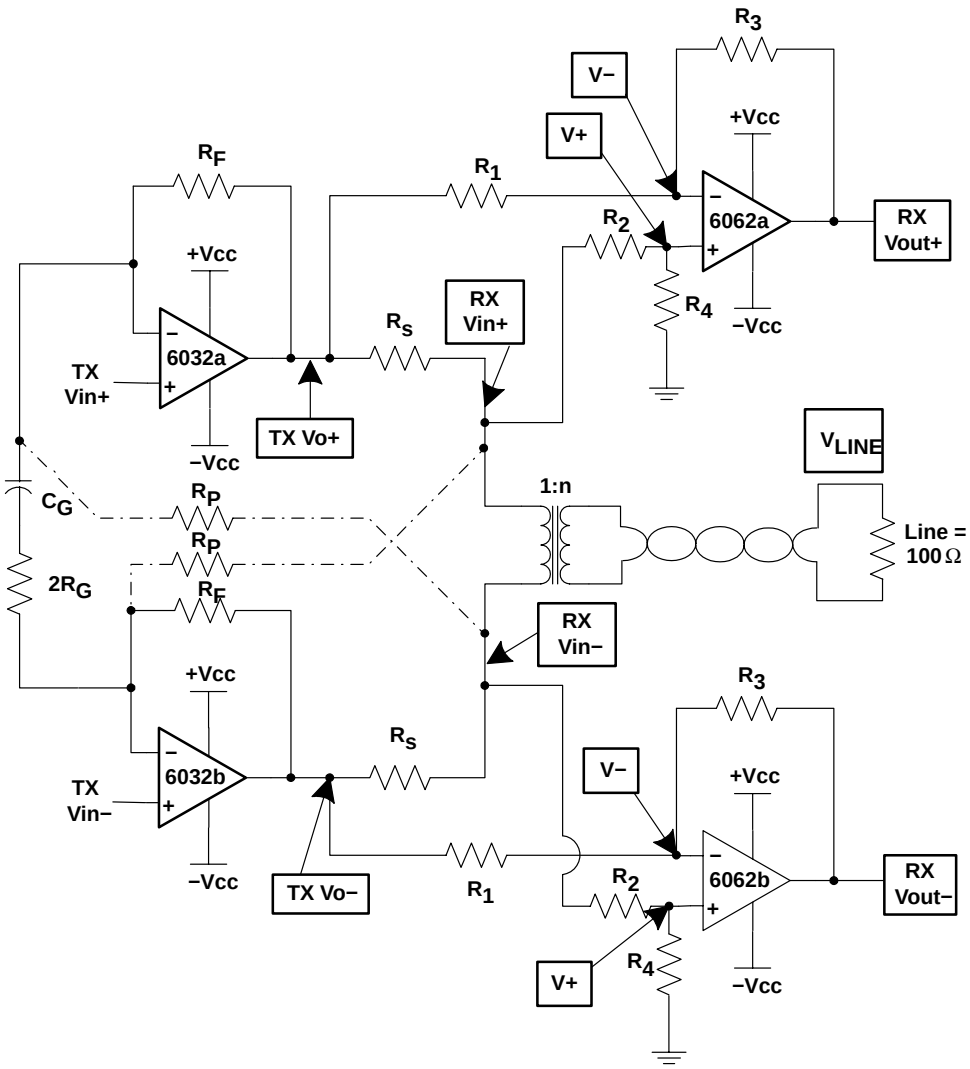

Figure 33. Common Mode Resistive Hybrid Circuit

Analysis is done as before, with superposition. Assume that (RX Vin+) = –(RX Vin−), (TX Vin+) = –(TX Vin−), and (TX Vo+) = –(TX Vo−). Under normal operating conditions, the noninverting node (+ input) of the receiver amplifier has very high input impedance, typically much greater than the resistors connected to this node. Therefore let the voltage at this node be equal to a fixed ratio of (RX Vin+) by the following relationship:

$$V+ = (\text{RX Vin}+)\left(\frac{R_4}{R_2 + R_4}\right) = \alpha\,(\text{RX Vin}+) \text{ where } \{0 \le \alpha \le 1\} \tag{25}$$

Using superposition, find a way to ensure that the output of the receiver is zero when the line driver amplifier creates a signal. The fundamental equation for the receive channel is:

$$\text{RX Vout}+ = (\text{TX Vo}+)\left(\frac{-R_3}{R_1}\right) + \alpha\,(\text{RX Vin}+)\left(\frac{R_1 + R_3}{R_1}\right) \tag{26}$$

Setting equation 26 to zero and using various substitutions, the proper value for R_1 to cancel out the transmit signal is:

$$R_1 = R_3\left(\frac{1 + X-\alpha}{\alpha}\right) \tag{27}$$

Using equation 27 allows the receiver to fully cancel out the transmitted signal. Setting X equal to 1 yields the proper equation required for the nonactive termination system case. Now examine the output of the receiver amplifier with a line signal applied. Using the substitutions of equations 26 and 27 leads to:

$$\text{RX Vout}+ = (\text{RX Vin}+)\left(\frac{2\,\alpha\,X}{1 + X-\alpha}\right) = \frac{V_{LINE}}{2n}\left(\frac{2\,\alpha\,X}{1 + X-\alpha}\right) \tag{28}$$

Where $0 \le \alpha \le 1$ and $0 < X \le 1$

Again, setting X equal to 1 gives the proper equation for the nonactive termination circuit. The interesting thing to note about equation 28 is that unlike the summing node configuration, there is no independent resistor that dictates the gain of the receiver. The gain is tied primarily to α and, to a lesser degree, the amount of active termination used (X). The maximum gain occurs when α is set to 1. Under this condition the variable X is canceled out and the maximum gain becomes V_{LINE}/n or 2 (RX Vin+).

The only way to increase the gain of the receiver amplifier is by increasing control on the (TX Vo+) signal. In a complex hybrid circuit, the (TX Vo+) signal may have some attenuation before interacting with the receiver circuitry and resistor R_1. With additional control of this attenuation, it is possible to make the gain even greater than 2. However, the analysis is left to the designer and is beyond the scope of this report.

Another advantage of the common mode configuration is the input impedance can be very high. The noninverting input impedance equals $R_2 + R_4$. If R_4 is not utilized, then the impedance becomes extremely high and is dictated by the noninverting input impedance of the amplifier. The impedance looking into the noninverting node of an amplifier is very high (>1 MΩ at low frequencies) as long as the amplifier is working within its linear range of operation. It is still a good idea to place a resistor R_2 in series with the amplifier to minimize surge voltages (and currents) appearing at the amplifier's input node. But to minimize noise, the resistance should be kept reasonably small (100 Ω should work well for starters).

The impedance looking into R_1 is a little more complex to analyze. But, it works on the same principle as the transmit amplifier's active termination scheme. For simplification, assume the two amplifier nodal voltages are equal in our analysis (V+ = V−). Using the same style of analysis previously, examine the input impedance looking into R_1. It is known that the voltage on the transmit side of R_1 is (TX Vo+). It is also known that the voltage appearing at the noninverting node (V+) is based on equation 25. Using the relationship of (TX Vo+) and (RX Vin+) of the signals and the relationship of R_S and R_L gives:

$$I_{R1} = \frac{(\text{TX Vo}+) - (V-)}{R_1} = \frac{(\text{TX Vo}+) - (\text{TX Vo}+)\left(\frac{\alpha}{1+X}\right)}{R_1} \tag{29}$$

$$Z_{R1}(\Omega) = \frac{R_1}{1-\left(\frac{\alpha}{1+X}\right)} \tag{30}$$

where $0 \le \alpha \le 1$ and $0 < X \le 1$

Even under the nonactive termination scenario, the impedance looking into R_1 is increased significantly when α is kept high. When active termination is used, the impedance looking into R_1 becomes very high, even though the resistance value is kept constant. This concept is very valuable in Section 4.6, where receiver noise for this circuit topology is discussed.

4.4 Noise With the Traditional Summing Node

The receivers amplify very small signals coming from the line. These signals can be very close to the noise floor of the entire system. Currently the minimum noise requirement of an ADSL system is –140 dBm/Hz. This translates to 31.6 nV/√Hz of noise at the line side. If a transformer ratio of 1:n is used then the noise requirement becomes 31.6 nV/√Hz ÷ n. This is a fairly forgiving number to strive for, but most designs stipulate that a *quiet* line noise of –150 dBm/Hz be used. This translates to 10 nV/√Hz at the line side. As before, this becomes reduced even further by the transformer ratio. This is why the receiver amplifier design must have a low noise or else performance suffers.

The lowest noise operational amplifiers on the market today typically come from voltage-feedback amplifiers (VFB). VFB amplifiers exhibit the typical gain-bandwidth product (GBWP) phenomenon where the bandwidth of the amplifier is reduced by the closed loop gain of the amplifier. If the gain of the amplifier needs to be increased from 2 to 10 (with X = 11%) in order to maintain the same output signal from the receiver, then the bandwidth is reduced by a factor of 5. Because most receiver amplifiers are high-speed amps with GBWPs greater than 100 MHz, the active impedance design is acceptable, as far as bandwidth is concerned.

Since the gain has been increased, the excess open-loop gain is reduced. This leads to an increase in distortion by the same factor as the gain increased. Again, since the amplifiers are high-speed and the ADSL signals are below 1.1 MHz, this is typically not an issue.

The real design constraint is due to the output noise of the receivers. To really examine how the output noise changes, look at the fundamental noise equations. Equation 31 shows the output spot noise of the traditional summing node amplifier configuration examined in Section 4.1.[5]

$$E_{OUT-RMS} = \sqrt{4kTR_1\left(\frac{R_F}{R_1}\right)^2 + 4kTR_2\left(\frac{R_F}{R_2}\right)^2 + 4kTR_F + \left(e_nNG\right)^2 + \left(i_{nn}R_F\right)^2} \tag{31}$$

where:

T = Temperature in degrees Kelvin (Typ. 300 K)
k = Boltzmann's Constant (1.380658 X 10^{-23} J/K)

$$NG = \text{Noise gain of the system} = 1 + \left(\frac{R_F}{R_1 \| R_2}\right)$$

e_n = Amplifier's voltage noise (nV/√Hz)
i_{nn} = Amplifier's inverting current noise (pA/√Hz)

Using the traditional approach as a reference with $R_1 = 2\ R_2$ for transmit rejection, setting the voltage gain such that $R_F = A_V\ R_2$, and letting $R = R_2$ produces:

$$E_{OUT-RMS} = \sqrt{2A_V kTR(2 + 3\ A_V) + \left(e_n(1 + 1.5\ A_V)\right)^2 + \left(i_{nn}\ A_V R\right)^2} \tag{32}$$

If the CPE is very close to the CO system, the voltage levels generated by the CPE system is not attenuated by the telephone line characteristics. Under this scenario, the receiver gain must not be too high or else clipping may occur. Of course this is dependant on the transformer ratio, power supply voltages, and the receiver configuration. At longer telephone line lengths, the line attenuates the CPE signal and the receiver gain may want to be increased to enhance the receiver signal level. Typical receiver voltage gains are 1 V/V and 2 V/V. To see this translated into equation 32 results in:

$$E_{OUT-RMS} = \sqrt{10\ kTR + 6.25\ e_n^2 + i_{nn}^2\ R^2} \quad \text{if } A_V = 1 \tag{33}$$

$$E_{OUT-RMS} = \sqrt{32\ kTR + 16\ e_n^2 + 4i_{nn}^2\ R^2} \quad \text{if } A_V = 2 \tag{34}$$

Both of these equations tell us that the receiver's voltage noise is a critical element of the total output noise of the receiver. Additionally, as the gain is increased from 1 V/V to 2 V/V, the resistor values used become vitally important in the output noise performance of the system. To keep noise minimized, a low-noise amplifier must be used along with low value resistors. But, the trade-offs of loading on the rest of the circuit must be dealt with appropriately.

4.5 Noise With the Active Impedance Summing Node

With the traditional noise parameters set up as a reference, attention is now turned to the active impedance summing node circuit explained in section 4.2. Using the design rules of $R_1 = R_2$ (1+X) to cancel out the transmit signal, the voltage gain defined by $R_F = R_2$ [(1+X) / 2], and letting $R = R_2$ results in:

$$E_{OUT-RMS} = \sqrt{\frac{A_V kTR}{X^2}\left[2A_V + X\left(2 + 3A_V\right) + X^2\left(2 + A_V\right)\right] + \left(e_n\left[\frac{2X + A_V(2 + X)}{2X}\right]\right)^2 + \left(i_{nn}\frac{A_V R(1+X)}{2X}\right)^2} \tag{35}$$

Using the same examples as before with setting A_V to 1 V/V and 2 V/V with a typical value for X of 0.25 results in:

$$E_{OUT-RMS} = \sqrt{55\ kTR + 30.25\ e_n^2 + 6.25\ i_{nn}^2\ R^2} \quad \text{if } A_V = 1;\ X = 0.25 \tag{36}$$

$$E_{OUT-RMS} = \sqrt{200\ kTR + 100\ e_n^2 + 25\ i_{nn}^2\ R^2} \quad \text{if } A_V = 2;\ X = 0.25 \tag{37}$$

There is a big noise disadvantage by using active termination when comparing these results to the traditional summing node receiver equations (equations 33 and 34). If a THS6062 amplifier is used (e_n = 1.6 nV/$\sqrt{Hz}$ and i_{nn} = 1.2 pA/$\sqrt{Hz}$) and varied the value for R, the output spot noise of the active termination circuit is increased considerably as shown in Figure 34 and Figure 35.

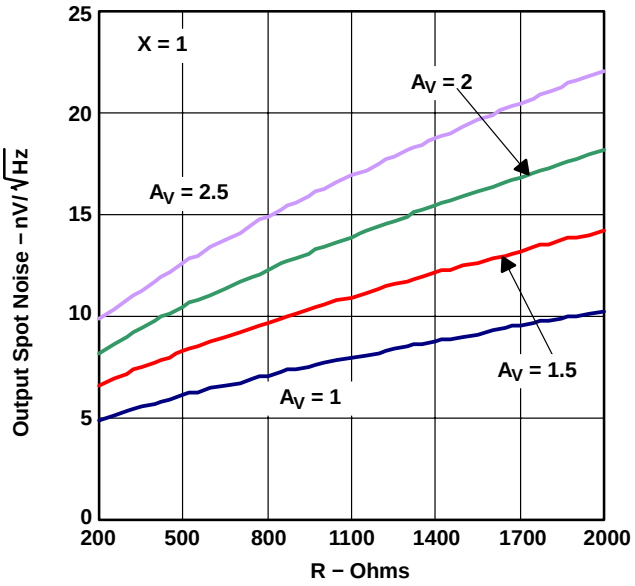

Figure 34. Traditional Circuit Summing Node Output Spot Noise

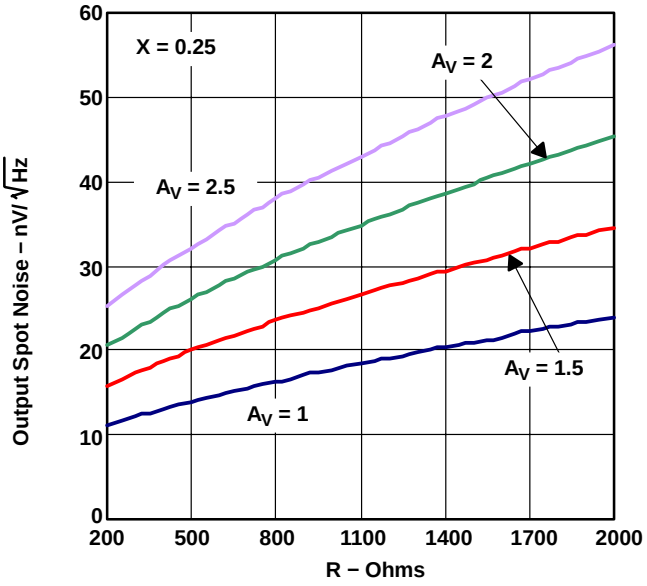

Figure 35. Active Impedance Summing Node Output Spot Noise With X = 0.25

Figure 34 and Figure 35 (graphs) indicate that the active termination circuit has approximately 2.5 times more output noise than the traditional design. To counteract this issue the active termination design requires reducing the resistor values by about a factor of 10. This places a burden on the noise allowance of the system when noise is a concern.

The summing node configuration shows additional design constraints. Because the receiver amplifier is used in a summing configuration, the inverting node (− input) is held at a virtual ground. Thus, the load presented to the rest of the circuitry is equal to the resistor values of R_1 and R_2 accordingly. But, if the active impedance circuit is used, the gain of the receiver must be increased to yield the desired output signal. This results in either a high value feedback resistor or small values for R_1 and R_2. In the case where a complex hybrid is used, the impedance of R_1 should be kept fairly high so as not to load down the hybrid circuitry. The compromise between all of these factors is one of the main drawbacks to the active impedance system.

4.6 Noise With the Traditional Common Mode Configuration

The next step is to examine the output noise of the common mode configuration. Using equation 31 as a basis for the common mode noise equation and modifying it based on Figure 33 results in:

$$E_{OUT-RMS} = \sqrt{4kTR_1\left(\frac{R_3}{R_1}\right)^2 + 4kT\left(R_2 + R_4\right)(NG)^2 + 4kTR_3 + \left(e_nNG\right)^2 + \left(i_{nn}R_3\right)^2 + \left(i_{np}\,NG\left(R_2 \| R_4\right)\right)^2} \quad (38)$$

Where:

$$NG = \text{Noise gain of the system} = 1 + \left(\frac{R_3}{R_1}\right)$$

i_{nn} = Amplifier's inverting current noise (pA/√Hz)

i_{np} = Amplifier's noninverting current noise (pA/√Hz)

Because noise is considered a premium in the ADSL system, it is very common to have as little attenuation as possible in the receive path. Because of this, resistor R_4 is typically not utilized ($\alpha = 1$ for the equations in Section 4.3). R_2 is commonly used with a small value to help minimize line surge effects on the receive amplifiers. One other point to make is VFB amplifiers have the same amount of noninverting current noise (i_{np}) as the inverting current noise (i_{nn}) that may simplify equation 38 slightly. Just as for the summing node case, it is easier to compare the noise equation when common values are substituted into the system. Using $R_1 = R_3 = R$ produces:

$$E_{OUT-RMS} = \sqrt{8kT\left(R + 2R_2\right) + 4\,e_n^2 + i_{nn}^2\left(R^2 + 4R_2^2\right)} \quad \text{if } \alpha = 1;\ A_V = 2 \tag{39}$$

For simplicity, set the value of R_2 to one-half the value of R_1, then equation 39 simplifies to:

$$E_{OUT-RMS} = \sqrt{16\,kTR + 4\,e_n^2 + 2i_{nn}^2\,R^2} \quad \text{if } A_V = 2;\ \alpha = 1;\ R_2 = \frac{R}{2} \tag{40}$$

As in Section 4.3, the input impedance of R_1 is increased due to the common mode configuration. If the effective input impedance of R_1 is equal to the input impedance of R_1 from the summing node case, then the value of R in equation 40 can be reduced to R/2 and still achieve the same impedance looking into the receive amplifiers. This results in:

$$E_{OUT-RMS} = \sqrt{8\,kTR + 4\,e_n^2 + 0.5i_{nn}^2\,R^2} \quad \text{if } A_V = 2;\ \alpha = 1;\ R = \frac{R}{2};\ R_2 = \frac{R}{2} \tag{41}$$

Comparing these equations to equation 34 shows that the common mode configuration has a much lower output noise than the summing node configuration. Plus, the input impedance looking into the receivers is no longer equal to the resistor values used in the design. When keeping the input impedance equivalent to the summing node circuit, the output noise is lower than the summing node with a voltage gain of 1. This is very impressive and definitely helps with noise allowances in the design.

4.7 Noise With the Active Impedance Common Mode Configuration

The next step is to look at the same conditions except with active termination. The only difference now is that $R_1 = R_3\,X$ if we assume $\alpha = 1$ as we did before. Using all the substitutions previously used in section 4.6 ($R = R_1$) results in:

$$E_{OUT-RMS} = \sqrt{\frac{4kT}{X^2}(1+X)\left(R + R_2\,(1+X)\right) + e_n^2\left(\frac{1+X}{X}\right)^2 + \frac{i_{nn}^2}{X^2}\left(R^2 + R_2^{\,2}(1+X)^2\right)} \quad \text{if } \alpha = 1;\ A_V = 2 \tag{42}$$

Substituting the same typical value for X as before results in:

$$E_{OUT-RMS} = \sqrt{80kT\left(R + 1.25R_2\right) + 25\,e_n^2 + 16\,i_{nn}^2\left(R^2 + 1.56\,R_2^{\,2}\right)} \quad \text{if } \alpha = 1;\ A_V = 2;\ X = 0.25 \tag{43}$$

Setting R_2 equal to one-half R gives:

$$E_{OUT-RMS} = \sqrt{130kTR + 25\,e_n^2 + 22.3\,i_{nn}^2\,R^2} \quad \text{if } \alpha = 1;\ A_V = 2;\ X = 0.25;\ R_2 = \frac{R}{2} \tag{44}$$

Finally, substituting R = R/2 to keep the same input impedance looking into R_1 yields:

$$E_{OUT-RMS} = \sqrt{65kTR + 25\,e_n^2 + 5.56\,i_{nn}^2\,R^2} \quad \text{if } \alpha = 1;\ A_V = 2;\ X = 0.25;\ R = \frac{R}{2};\ R_2 = \frac{R}{2} \tag{45}$$

Although this is much larger than the non-active impedance circuit noise shown in equation 41, it is much better than the noise equation of the summing node active impedance shown in equation 37. In fact, looking at equation 34 which shows the noise of the traditional summing node circuit without active termination, the output noise is comparable to each other.

Figure 36 (graph) compares the output noise of all four circuits with a voltage gain of 2 while using the THS6062 amplifier.

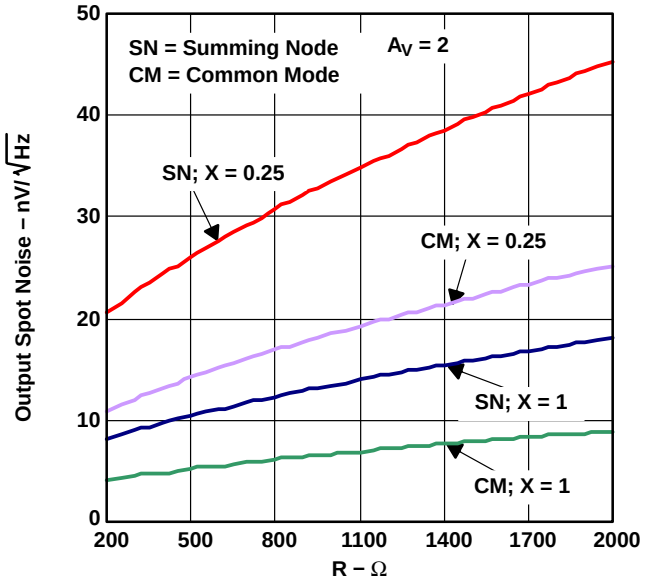

Figure 36. Output Spot Noise Comparison of All Four Receiver Circuits With Gain = +2

The results show that if used properly, the common mode configuration results in lower noise compared to the summing node configuration. The added benefit of increased input impedance indicates that the common mode circuit has many benefits worth considering. One possible drawback to the common mode circuit is the amplifier's common mode rejection ratio (CMRR) over the entire ADSL frequency band must have very good results. Even though the receive band in the CO is from 25 kHz to 138 kHz, the receive amplifier must still reject the transmit signals appearing from 160 kHz to 1.1 MHz. If the CMRR is 40 dB or better up to 1.1 MHz, then the receive amplifier should be acceptable.

One other possible drawback to the common mode circuit is the amplifier must have good linearity over the entire common mode input voltage range (V_{ICR}). This is due to the transmit signal voltage levels appearing at the receive amplifier's input nodes. Usually the common mode voltage is reduced due to R_S and R_L, but what happens if the line is opened up? The full transmit voltage level appears at the +input of the receiver. Thus, the receiver must have enough V_{ICR} to accommodate the expected transmit voltage levels. Plus, the receive amplifier must have power supply voltages at least equal to the transmit amplifier's power supply voltages. Exceeding the V_{ICR} results in distortion at the receiver's output reducing data transmission rates and reach.

4.8 Noise From the Line Drivers—Traditional Design

If the receive amplifier's noise is critical to the ADSL system, then the transmit amplifier's noise on the system must also be examined. Even though the line driver amplifiers only transmit within their respective frequency band, broadband noise from the same amplifiers is in the receiver's frequency band.

The first step in examining the noise is to find the general equation for the line driver amplifier noise. Figure 1 is used for the analysis in this section. It is easier to concentrate initially on one amplifier rather than both amplifiers in the differential configuration. Thus, the gain resistance (R_G) is split and connected directly to a ground reference without the presence of C_G. In reality we know that the noise associated with R_G is $\sqrt{2}$ less, as it is commonly between the two line drivers—discussed later. The input resistance, connected to the noninverting input node, is equal to the variable R_{IN}. This results in:

$$E_{OUT-RMS} = \sqrt{4kTR_{IN}(NG)^2 + 4kTR_G\left(\frac{R_F}{R_G}\right)^2 + 4kTR_F + \left(e_nNG\right)^2 + \left(i_{nn}\,R_F\right)^2 + \left(i_{np}\,NG\,R_{IN}\right)^2} \quad (46)$$

Where:

$$NG = \text{Noise gain of the system} = 1 + \left(\frac{R_F}{R_G}\right)$$

Because most line driver amplifiers are current feedback amplifiers (CFB), the inverting current noise (i_{nn}) and noninverting current noise (i_{np}) values are different and must be kept as separate entities. This equation has a lot of terms and may be confusing. It is sometimes easier to see an example of the noise. Using the THS6032 as the line driver amplifier (e_n = 2.4 nV/$\sqrt{Hz}$, i_{nn} = 15.2 pA/$\sqrt{Hz}$, and i_{np} = 11.3 pA/$\sqrt{Hz}$) with a input impedance of 500 Ω, a voltage gain of 10, and a feedback resistance of 1 kΩ results in:

$$E_{OUT-RMS} = \sqrt{8.28 \times 10^{-16} + 1.49 \times 10^{-16} + 1.66 \times 10^{-17} + 5.76 \times 10^{-16} + 2.31 \times 10^{-16} + 3.19 \times 10^{-15}} \quad (47)$$

Equation 47 shows that the main contributors to the output noise are the input impedance (R_{IN}) and the noninverting current noise (I_{np}) terms. The amplifier's voltage noise (e_n) term should also be considered to be influential to the output noise, but is not to the extent of the (I_{np} NG R_{IN}) term used in this example. This scenario leads to an output spot voltage noise of 70.6 nV/$\sqrt{Hz}$. In the differential configuration, the total line driver system output noise is equal to the single amplifier's noise multiplied by $\sqrt{2}$. Thus, the total line driver output noise would be equal to approximately 100 nV/$\sqrt{Hz}$.

Are there any tricks, other than the obvious reduction of impedances and amplifier gain, to reduce the line drivers' output noise? The answer is a limited yes. First realize that the only concern is with noise within the receive spectrum. This is useful because band limiting filters can be employed within the transmit channel. These filters essentially minimize the gain of the transmit amplifiers outside of their intended frequency band. If the gain is reduced, the output noise is also reduced accordingly as long as the noninverting impedance is not increased too drastically.

This warning is based on the current noise times the impedance creating voltage noise. At the inverting node, the output noise due to the inverting current noise (I_{nn}) is based solely on the feedback impedance. But, at the noninverting node, the noninverting current noise (I_{np}) is multiplied by the impedance to ground. This creates voltage noise that is multiplied by the noise gain of the amplifier. Thus, keeping the noninverting impedance low is very critical to the output noise of the amplifier.

One way to accomplish a lower gain is to use a capacitor (C_G) in series with R_G. This capacitor minimizes the line driver's voltage gain from dc (NG becomes equal to 1) to the –3 dB corner frequency (set by $1/2\pi R_G C_G$). The corner frequency should be set low enough so as not to hinder the performance of the transmit spectrum. This typically means that the corner frequency is approximately a factor of 10 lower than the lowest TX frequency, or 16.3 kHz. If the receive band does not start until about 25 kHz, the benefit of C_G is limited.

One other way to minimize noise is to connect the two gain resistors (R_G) together in series and replace with a single equivalent resistor—see Figure 4 and Figure 5. Although the gain has not been altered or the impedance changed, the noise associated with R_G will be reduced by $\sqrt{2}$ over the original scenario. The other benefit of connecting R_G in this manner is the benefit of cross coupling the amplifiers. Cross coupling will help keep the output signals fully differential and complementary to each other, a key requirement for a differential system. Finally, as long as the individual amplifiers are matched fairly closely, the input offset voltage of each amplifier will be generally close to each other. The resulting output offset voltage—generally set by the gain of the amplifier times the input offset voltage—will have a gain of 1 instead of the signal gain. This is usually not an issue as a series capacitor is typically used in series with the two amplifier outputs to eliminate dc biasing through the transformer and to match the reflected line side capacitor better.

If the line driver amplifiers have 100 nV/$\sqrt{\text{Hz}}$ of noise, then why have a low noise receiver system? The answer is that the hybrid circuit helps eliminate this noise. Remember that the purpose of the hybrid is to reject the signal coming out of the line driver amplifiers while fully passing the line signals. If the hybrid rejects the transmit signals, it also rejects the noise from the line driver. Although the amount of rejection is not perfect, a rejection from 6 dB up to 20 dB is very common. If the hybrid has 20 dB of rejection, then the receiver noise becomes very important in the system.

Since noise is classified as broadband and completely random in nature, cancellation is greatest when connecting the hybrid to one noise source. From looking at Figure 32 and Figure 33, the common mode rejection circuit appears to have better line driver noise rejection than the summing node circuit. The common mode circuit taps into the system on both sides of R_S. Thus, the noise signal is from the same source, not a different source as in the summing node scenario. Although rejection still occurs in the summing node case, it typically is not as good as the common mode circuit.

One last thing to point out is that placing a band pass filter in the receive path does not help with noise from the line driver amplifiers. The line driver noise is in the exact same spectrum as the receive signal and the filters do not have any effect on the elimination of this noise. One thing it does is help eliminate the line driver's ADSL signals. But, the noise elimination must come from the line driver portion of the circuit or the hybrid.

4.9 Noise From the Line Drivers—Active Impedance Design

As far as the hybrid and receiver goes in the active termination design, the same ideas hold true from the previous section. The only thing this section looks at is how the output noise is different from the traditional scenario. Figure 33 is used as the reference design for examining the output noise of the active termination circuit. First, examine the single amplifier and then combine the two amplifiers together to see the differential output noise. The single amplifier output noise becomes:

$$E_{OUT\text{-}RMS} = \sqrt{4kTR_{IN}(NG)^2 + 4kTR_G\left(\frac{R_F}{R_G}\right)^2 + 4kTR_p\left(\frac{R_F}{R_P}\right)^2 + 4kTR_F + \left(e_nNG\right)^2 + \left(i_{nn}\,R_F\right)^2 + \left(i_{np}\,NG\,R_{IN}\right)^2} \quad (48)$$

Where:

$$NG = \text{Noise gain of the system} = 1 + \left(\frac{R_F}{R_G \parallel R_P}\right)$$

Just as before, an example is used to quantify this complex equation so results can be compared. Letting X = 0.25 dictates that $R_P = R_F / (1-X) = 1333\ \Omega$. If the voltage gain equals 10, R_G becomes 444 Ω based on equation 12. This results in:

$$E_{OUT-RMS} = \sqrt{1.33x10^{-16} + 3.73x10^{-17} + 1.24x10^{-17} + 1.66x10^{-17} + 9.22x10^{-17} + 2.31x10^{-16} + 5.11x10^{-16}} \quad (49)$$

These numbers have changed from the traditional case. This is due mainly to the noise gain of the system being drastically reduced. When it comes to noise gain, it is not the same as the signal gain dictated by equation 5 or equation 11. Those equations relied upon the out-of-phase signal increasing the signal gain of the amplifier. The probability is extremely low that the noise signal will be exactly 180° out of phase with the amplifier's noise, since noise from independent sources is random in phase and magnitude.

The main contributor to the noise still remains the (I_{np} NG R_{IN}) term, but the voltage noise contribution (e_n) is considerably reduced from the previous case—due mainly to the reduced noise gain. Because the noise has been considerably reduced, other terms, such as (I_{nn} R_F) , become increasingly more influential to the output noise. Summing the components of equation 49 together results in an output spot noise of 32.1 nV/$\sqrt{Hz}$. Differentially, the output noise is 45.5 nV/$\sqrt{Hz}$ for the two amplifiers, which is less than half the output noise of the traditional design.

But, there is an issue with this computation. The output noise of one amplifier, after being reduced by R_S and R_L by 1/(1+X), gets fed into the other amplifier through R_P. When this is taken into account, the output noise increases by the following relationship:

$$E_{OUT\text{-}RMS'} = \sqrt{E_{OUT\text{-}RMS-1}^2 + E_{OUT\text{-}RMS-2}^2\left(\frac{R_F}{R_P}\right)^2} \quad (50)$$

If it is assumed that the output noise of amplifier 2 is approximately the same as the output noise of amplifier 1, then the equation may be simplified. Using equation 9 and equation 10 substitutions results in:

$$E_{OUT\text{-}RMS'} = \sqrt{E_{OUT\text{-}RMS-1}^{2}\left(\frac{2\left(1 + X^{2}\right)}{(1 + X)^{2}}\right)} \quad (51)$$

If X = 0.25 and the original output noise was 32.1 nV/$\sqrt{\text{Hz}}$, then the resultant output spot noise becomes 37.4 nV/$\sqrt{\text{Hz}}$. The differential output spot noise becomes 52.9 nV/$\sqrt{\text{Hz}}$. Although this is an increase from equation 49, it is still much lower than the 100 nV/$\sqrt{\text{Hz}}$ previously attained from the traditional case. The actual number is different than this due to the fact that the output noise from amplifier 2 is not exactly the same in frequency and phase as the noise from amplifier 1. But, it does give a close approximation such that the noise allowance can be designed within the targeted range.

4.10 General Conclusions—The Receiver and Noise

With any electrical circuit, there are trade-offs to using one configuration over another. The active impedance circuit is no exception. The trade-off to achieving low line driver power dissipation is that the receiver circuitry requires more voltage gain. This is to overcome the reduction in differential voltage appearing at the receiver's inputs. Any time an amplifier's voltage gain is increased, the output noise dramatically increases as seen in the examples. The use of the common mode receiver circuit offers some benefits over the traditional summing node circuit. This includes increased input impedances for small value resistors and an output noise reduction, critical for achieving the *quiet* line requirements of –150 dBm/Hz. As long as the receiver amplifier is chosen with the proper common-mode characteristics, a high CMRR over frequency and a large V_{ICR}, then using this circuit is beneficial to the ADSL system.

No matter how low the receiver circuit's noise is, the line driver amplifier's own output noise may become the main contributor of noise in the system. To help minimize this possibility, the input impedance to the line driver must be kept very low. Controlling the voltage gain over frequency and using common mode resistors helps keep the line driver's noise to a minimum. Additionally, using a small transformer ratio of 1:1.2 or 1:1.42 increases the noise allowance of the system over a traditional 1:2 transformer. The use of the common mode receiver circuit also has the advantage of reducing the transmit amplifier noise by tapping into a single noise source. The summing node circuit requires tapping into two essentially independent noise sources that may limit the amount of noise rejection of the system. Remember that ADSL is a bidirectional data transmission system and analysis of all components, even ones not mentioned in this report, is required. Failure to do so results in a noisy, limited-use system.

4.11 References

1. Victor Koren, *Design Ideas—Line Driver Economically Synthesizes Impedance*, EDN, January 6, 1994
2. Jerry Steele, *Ideas for Design—Positive Feedback Terminates Cables*, Electronic Design, p. 91−2, March 6, 1995
3. Donald Whitney Jr., *Design Ideas—Circuit Adapts Differential Input to Drive Coax*, EDN, p. 132−4, May 8, 1997
4. Texas Instruments data sheet, *THS6032*, (SLOS233)
5. Texas Instruments application report, *Noise Analysis in Operational Amplifier Circuits*, (SLVA043)

Appendix A Simplified Active Termination Circuit Derivations

To derive the simplified active termination circuit, first assume that the amplifier is operating well within its frequency range and it has linear operation. Also assume that the inputs are fully balanced and complement each other. Additionally, the line impedance is transferred to across the transformer and is considered symmetric. The parasitics of the transformer (RLGC) and the line characteristics are also ignored. The first thing is to examine the active termination circuit shown in Figure A−1.

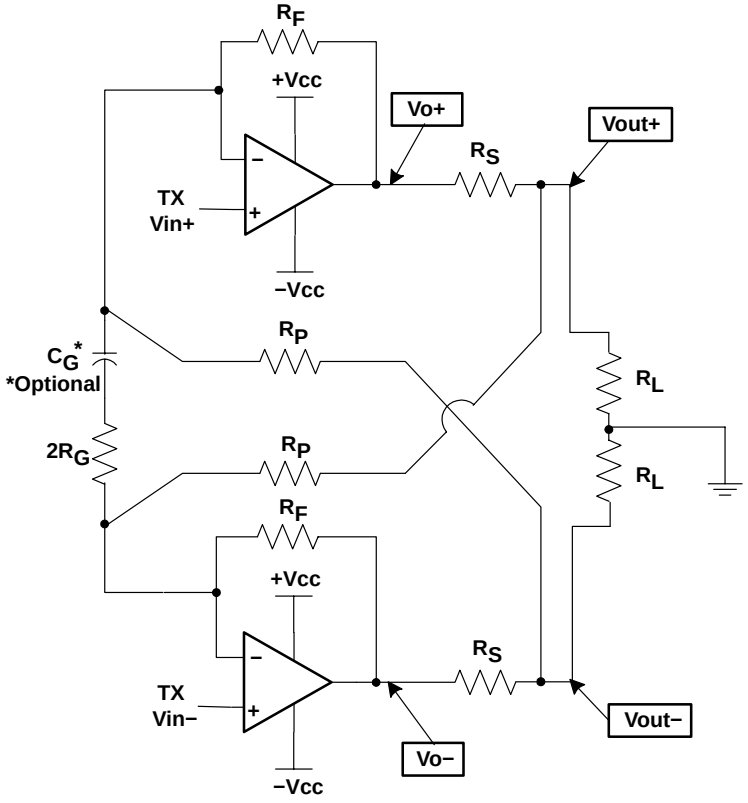

Figure A−1. Active Termination Circuit

The simplest case also assumes that R_P is much greater than R_L and the loading effects are ignored. Using superposition, the output of the TX+ amplifier becomes:

$$V_{o+} = (TXV_{in+})\left(1 + \frac{R_F}{R_G \| R_P}\right) + (V_{out-})\left(\frac{-R_F}{R_P}\right) \quad (52)$$

Using symmetry of the signals, substitute (Vout−) with −(Vout+). This leads to:

$$(V_{out-}) = -(V_{out+}) = -(V_{o+})\left(\frac{R_L}{R_L + R_S}\right) \quad (53)$$

Placing equation 53 into equation 52 yields:

$$V_{o+} = (TXV_{in+})\left(1 + \frac{R_F}{R_G \| R_P}\right) + -(V_{o+})\left(\frac{R_L}{R_L + R_S}\right)\left(\frac{-R_F}{R_P}\right) \quad (54)$$

$$V_{o+} = (TXV_{in+})\left(1 + \frac{R_F}{R_G \| R_P}\right) + (Vo+)\left(\frac{R_L}{R_L + R_S}\right)\left(\frac{-R_F}{R_P}\right) \quad (55)$$

Combining the (V_{o+}) terms yields:

$$(V_{o+})\left[1 - \left(\frac{R_L}{R_L + R_S}\right)\left(\frac{R_F}{R_P}\right)\right] = (TXV_{in+})\left(1 + \frac{R_F}{R_G \| R_P}\right) \quad (56)$$

Which leaves us with the final simplified equation used for equation 5:

$$A_v = \frac{V_{o+}}{(TXV_{in+})} = \frac{1 + \left(\frac{R_F}{R_G \| R_P}\right)}{1 - \left(\frac{R_F}{R_P}\right)\left(\frac{R_L}{R_L + R_S}\right)} \text{ iff } R_L << R_P \quad (57)$$

The next step is to take equation 57 to the next simplified level. If resistor R_P is not much greater than R_L, then the voltage appearing at ($V_{out\pm}$) is not as stated above. The voltage should be reduced because of the added loading effects. The simplest way to add this is by assuming the voltage appearing at the inverting node of the amplifier, that R_P is connected to, is equal to zero. If the gain of the amplifier is large (i.e. A_V >10), then this is a realistic approximation. Placing R_P in parallel with R_L then modifies equation 53, yielding the modified version of equation 57 (which is the same as equation 6):

$$A_v = \frac{V_{o+}}{(TXV_{in+})} = \frac{1 + \left(\frac{R_F}{R_G \| R_P}\right)}{1 - \left(\frac{R_F}{R_P}\right)\left(\frac{R_L \| R_P}{R_L \| R_P + R_S}\right)} \quad (58)$$

Even going to this level makes the rest of the equations used throughout the document very complex. It is highly recommended that the simplest form be used to estimate the proper circuit values. Then, if required, start implementing the more complex equation listed above. If the designer wants to go to the effort, the equations listed in Appendix B can be used to obtain the true circuit values.

Realistically though, using the simplified equations yields circuit values within a few percent of the true value. Even then the design is typically constrained by the 1% resistor values found throughout the industry. This implies that even if the perfect design was created with perfect resistors on paper, the values obtainable in the real world typically limit the design. Bottom line, use the simplified equations and save yourself a lot of time, money, and grief.

Appendix B Accurate Active Termination Circuit Derivation

The assumptions made in Appendix A are also used in Appendix B. The only exception is that the true value for Vout± is used. But, this also has its own limitations based on the fact that there are loading effects due to the receiver circuitry that can, and will, slightly alter the voltage at the Vout± node. This can be pretty much ignored if the common mode receiver circuit is utilized with an α value of 1. But, if α is less than 1, loading effects can start to come into play.

Due to all the complexity of the math involved, the names for the voltage nodes are changed to simplify things. Initially, assume there is no loading of the receiver on the system. After the receiver-less configuration is fully examined, the loading effects of the receiver circuit are added. Figure B−1 is used throughout this section as a reference for the equations.

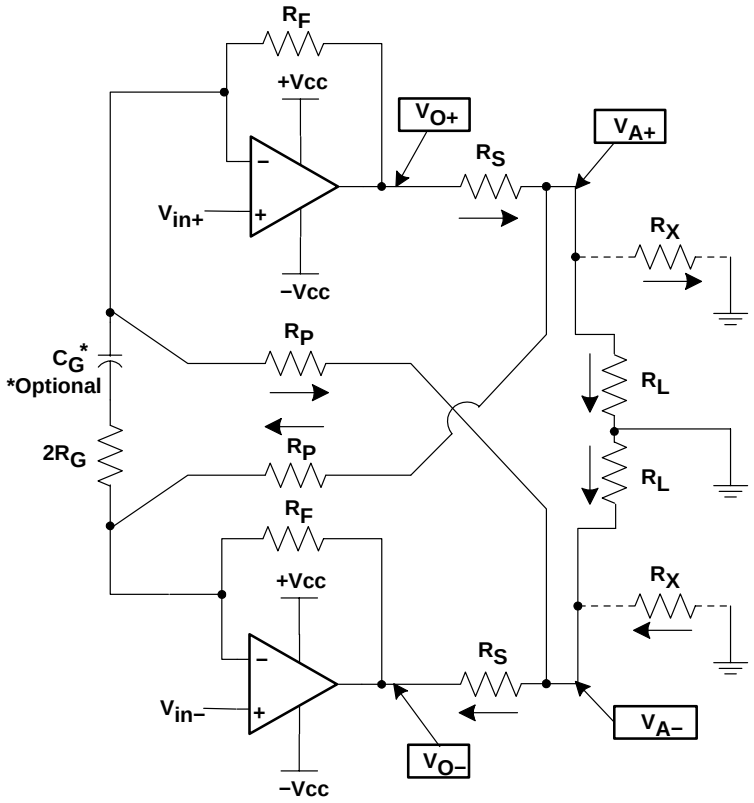

Figure B−1. Active Termination Circuit

Just like in Appendix A, use superposition to figure out the transfer function. This leads to:

$$V_{o+} = V_{in+}\left(1 + \frac{R_F}{R_G \| R_P}\right) + \left(V_{A-}\right)\left(\frac{-R_F}{R_P}\right) \tag{59}$$

Equation 60 uses the differential nature of the circuit voltages that leads to the substitution of V_{A-} with $-V_{A+}$.

$$V_{o+} = V_{in+}\left(1 + \frac{R_F}{R_G \| R_P}\right) + \left(V_{A+}\right)\left(\frac{R_F}{R_P}\right) \tag{60}$$

To solve equation 60 the voltage V_{A+} must be figured out. To accomplish this, look at the currents flowing around the V_{A+} node. As dictated by the arrows in Figure B−1, the KCL (Kirchhoff's Current Law) equation becomes:

$$I_{RS} = I_{RL} + I_{RP} \tag{61}$$

$$\left(\frac{V_{o+} - V_{A+}}{R_S}\right) = \left(\frac{V_{A+}}{R_L}\right) + \left(\frac{V_{A+} - V_{in+}}{R_P}\right) \tag{62}$$

Again, using the differential nature of the system, V_{in-} becomes V_{in+}. Some manipulation leads to:

$$V_{o+} - V_{A+} = V_{A+}\left(\frac{R_S}{R_L}\right) + V_{A+}\left(\frac{R_S}{R_P}\right) + V_{IN+}\left(\frac{R_S}{R_P}\right) \tag{63}$$

Solving for V_{A+} yields:

$$V_{A+} = \frac{V_{O+} R_L R_P - V_{in+} R_S R_L}{R_S R_P + R_S R_L + R_L R_P} \tag{64}$$

To save a lot of headaches, define a variable K to equal the denominator of equation 64 such that:

$$K = R_S R_P + R_S R_L + R_L R_P \tag{65}$$

Substituting equations 64 and 65 into 60 leads to:

$$V_{o+} = V_{in+}\left(1 + \frac{R_F}{R_G \| R_P}\right) + \frac{V_{O+} R_L R_F}{K} - \frac{V_{in+} R_S R_L R_F}{R_P K} \tag{66}$$

Simplifying equation 66 leads to the final solution:

$$A_v = \frac{V_{o+}}{V_{in+}} = \frac{R_P K\left[\left(R_G \| R_P\right) + R_F\right] - R_S R_L R_F\left(R_G \| R_P\right)}{R_P\left(R_G \| R_P\right)\left(K - R_L R_F\right)} \tag{67}$$

This is not the simplest equation to use. Utilizing some of the assumptions discussed in the main document may help simplify equation 67 a little bit more. Equation 10 led to $R_P = \frac{R_F}{1-X}$ and equation 8 gave $R_S = R_L X$ (where $0<X\leq 1$). Putting these into equations 67 and 65 leads to:

$$A_v = \frac{V_{o+}}{V_{in+}} = \frac{K X\left[R_F + R_G(2 - X)\right] - R_G R_S{}^2(1 - X)}{R_G\left(K X - R_S R_F\right)} \tag{68}$$

$$\text{Where } K = \frac{R_S}{X(1-X)}\left[R_F(1 + X) + R_S(1-X)\right] \tag{69}$$

Instead of solving in terms of R_S, it may also be useful to solve in terms of R_L. This yields:

$$A_v = \frac{V_{o+}}{V_{in+}} = \frac{K\left[R_F + R_G(2 - X)\right] - R_G R_L{}^2 X(1 - X)}{R_G\left(K - R_L R_F\right)} \tag{70}$$

$$\text{where } K = \frac{R_L}{1 - X}\left[R_F(1 + X) + R_L X\,(1 - X)\right] \tag{71}$$

These equations all neglected the loading effects of the receiver connection at node V_{A+}. Since connecting another resistor to this node changes the nodal voltage, then a slight modification has to be done. Using the same basic equations above leads to the modified equation to solve for V_{A+}:

$$V_{A+} = \frac{V_{O+} R_L R_P R_X - V_{in+} R_S R_L R_X}{R_X R_S R_P + R_X R_S R_L + R_X R_L R_P + R_S R_L R_P} \tag{72}$$

$$\text{Let } K = R_X R_S R_P + R_X R_S R_L + R_X R_L R_P + R_S R_L R_P \tag{73}$$

Solving for the final voltage gain becomes:

$$A_v = \frac{V_{o+}}{V_{in+}} = \frac{R_P K\left(R_G \| R_P + R_F\right) - R_S R_L R_F R_X\left(R_G \| R_P\right)}{R_P\left(R_G \| R_P\right)\left(K - R_L R_F R_X\right)} \tag{74}$$

Using the same simplifications as before gives us:

$$A_v = \frac{V_{o+}}{V_{in+}} = \frac{K X\left[R_F + R_G(2 - X)\right] - R_X R_G R_S{}^2(1 - X)}{R_G\left(K X - R_S R_F R_X\right)} \tag{75}$$

$$\text{where } K = \frac{R_S}{X(1 - X)}\left[R_F R_X(1 + X) + R_S\left(R_X\,(1 - X) + R_F\right)\right] \tag{76}$$

Solving for R_L in place of R_S leads to:

$$A_v = \frac{V_{o+}}{V_{in+}} = \frac{K\left[R_F + R_G(2 - X)\right] - R_X R_G R_L{}^2 X(1 - X)}{R_G\left(K - R_L R_F R_X\right)} \tag{77}$$

$$\text{where } K = \frac{R_L}{1 - X}\left[R_F R_X(1 + X) + R_L X\left(R_X\,(1 - X) + R_F\right)\right] \tag{78}$$

Even though all of these equations work very well, they are also very encompassing. Using the simplified equations shown throughout the document yields answers close to the answers when using the equations in Appendix B. Since most designers only use 1% resistors, the simplified equations may be a better and easier choice for circuit design.

Appendix C Component Values Used During Testing

Table C−1. Component Values Used in Lab Testing

TRANSFORMER RATIO (1:n)	X (%)	R_S (Ω)	R_F (Ω)	R_P (Ω)	R_G (Ω)	A_V (V/V)
1:1 Midcom 671−5792	10	5.00	1150	1270	7680	11.1
	20	10.0	1150	1430	499	12.1
	30	15.0	1150	1650	261	13.1
1:1.2 Schott 37698	14	4.86	1150	1330	1960	9.56
	20	6.94	1150	1430	715	10.1
	30	10.4	1150	1650	340	10.9
	40	13.9	1150	1910	221	11.8
1:1.42 Schott 33817	15	3.72	1150	1330	3950	8.15
	20	4.96	1150	1430	1090	8.51
	30	7.44	1150	1650	442	9.22
	40	9.92	1150	1910	280	9.93
1:1.8 Schott 36979	20	3.09	1150	1430	2550	6.70
	30	4.63	1150	1650	681	7.27
	40	6.17	1150	1910	402	7.82
1:2 Midcom 671−5792	20	2.50	1150	1430	5230	6.03
	30	3.75	1150	1650	866	6.53
	40	5.00	1150	1910	475	7.04

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