Application Note

Paralleling the OPA593 High-Voltage, High-Current Op Amp for 2 × Output Current

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ABSTRACT

Power operational amplifier (op amp) applications are extending into areas where higher precision along with high-voltage supplies (> 50 V), and currents from hundreds of milliamperes to amperes are required. The OPA593 is a recent TI power op amp introduction that is usable with power supplies up to 85 V. It is capable of an output current of 0.25 A from a 4 mm × 4 mm, WSON package. However, even with all the OPA593 offers a new semiconductor test application has been identified where a current level up to 0.5 A is a must have.

This application note describes how two OPA593 op amps can have their outputs parallel connected to provide that 0.5-A output current. It provides a circuit design that successfully meets all DC and AC aspects of the application including the ability to drive a load capacitance of 1 μF with complete stability.

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1 Introduction

The OPA593 high-voltage, high-current operational amplifier (op amp) is finding design-in opportunities in different test platforms and applications. The 85 V single, ±42.5 V dual-supply capability, 0.25-A maximum output drive current, and accurate current limit set (Iset) make it a good match for semiconductor and other component tester applications. Such applications often require rapid supply voltage and load current changes through the test cycle.

Recently, a new test application surfaced from the field that not only required the OPA593 high output voltage capability, but also high output current up to 0.5 A. This is double the normal 0.25-A output load current capability. A single OPA593 device is not able to provide the higher current level, but a pair of OPA593 amplifiers with their outputs connected in a parallel does. It is often assumed that paralleling op amps is an easy thing to do, but then the performance proves to be less than expected in one way or another. However, by applying careful attention to design details such as current balancing, good performance can be achieved.

Parallel output circuits often appear in the application section of the data sheet for a power op amp. Two commonly-shown configurations include a simple parallel-connected pair of op amps seen in Figure 1-1, and a bit more sophisticated Leader-follower circuit shown in Figure 1-2. Both circuits incorporate output ballast resistors, Rb1 and Rb2 that play an important role in the operation of each circuit. The selection of these circuits is discussed in this document. The Leader-follower circuit is more often applied because it provides accurate voltage output Vo level whereas the output of the simple circuit changes with load.

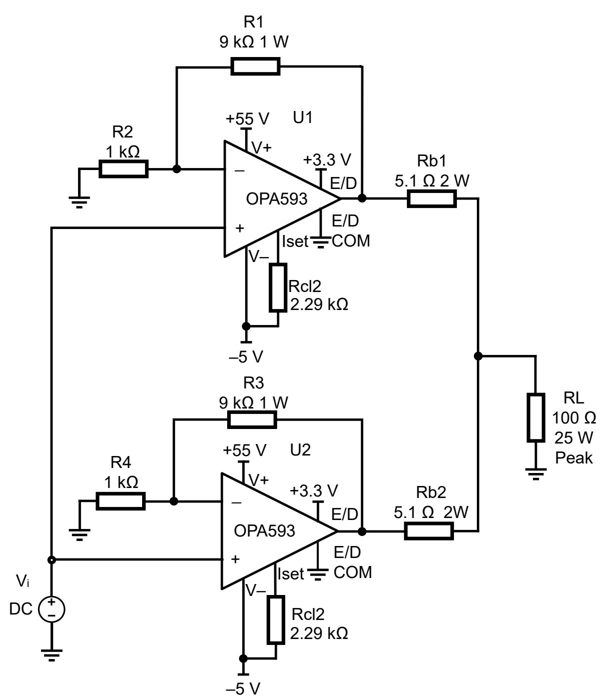

Figure 1-1. Simple Parallel Output Op Amp Circuit

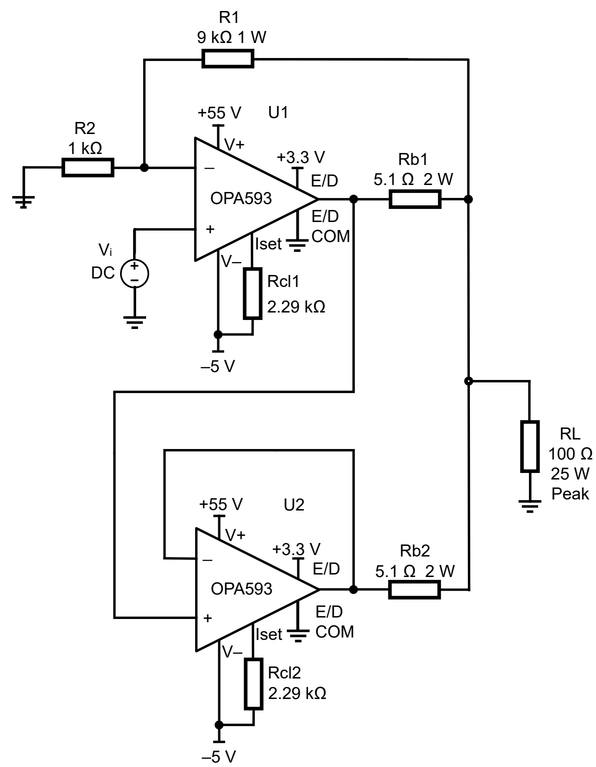

Figure 1-2. Leader-follower Parallel Output Op Amp Circuit

1.1 Parallel Output Circuit Design Considerations

Directly hard-wiring the outputs of two power op amps is not a good electrical practice. If the outputs of the two op amps are directly connected together uneven current sharing can result. That happens because each of the two op amps tries to force a slightly different Vout voltage which is dependent on their individual Vos level. This current imbalance can lead to uneven power dissipation and uneven device heating.

Even though the resulting Vout differences between the op amps may be small, it is the electrical equivalent of connecting two very low-impedance voltage sources directly across one another. The op amp output impedances (Zcl) are very low, typically millohms due to the high loop gain at which each op amp operates. The Zcl differ between them if each op amp has a different closed-loop gain setting as can be the case with the leader-follower configuration. When there is nearly zero connection resistance between the outputs, the current can be quite high and affect the basic circuit functionality. The added output ballast resistances do much to minimize the current that can flow between the two outputs.

An OPA593 leader-follower parallel output circuit is shown in Figure 1-3. The DC voltage and current levels result from the 5-Vdc input, and a resulting output voltage Vout of +50 V. The load current I4 is 0.45 A. Higher output voltage is obtained by increasing the power supplies, up to 85 V across the V+ and V– pins. The output current is upwards to 0.5 A for the two OPA593 op amps in this configuration.

The power dissipations of the OPA593 op amps and the load must be taken into consideration because of power and thermal limitations as with any electronic component. Each OPA593 dissipates 1.25 W, while the 111-Ω load resistor power is 22.5 W for this specific example. The two OPA593 power dissipations become exceedingly high and they go into thermal shutdown if the delta between the supply voltage and theri output voltage is large and sustained for too long.

Remember that the intended application for the presented circuit involves a fast ATE test sequence where the dwell times are short fractions of a second. The average power dissipation in the fast ATE test sequence is much lower than when operating in a continuous high-power dissipation condition.

The Leader-follower configuration offers the following advantages:

- Similar to a single op-amp amplifier it may be connected either as a non-inverting, or inverting amplifier
- One set of gain resistors establishes the overall voltage gain of the complete amplifier doing away with matching sets of resistors

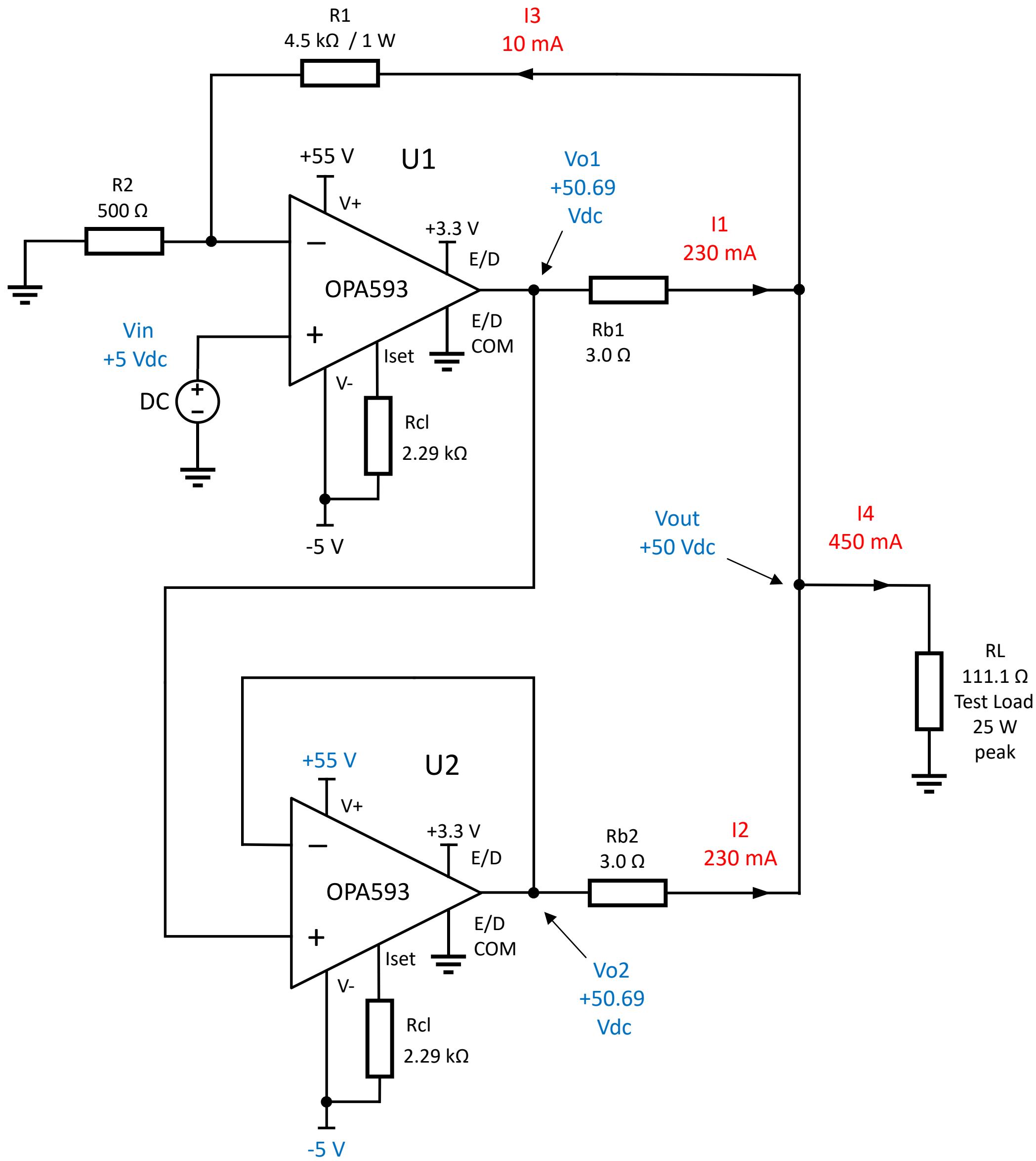

Figure 1-3. Leader-follower Parallel Output Amplifier

The U1 leader amplifier in Figure 1-3 connected as a non-inverting amplifier has its gain set to +10 V/V. The follower amplifier U2, is a simple unity-gain buffer with a gain of +1 V/V. The two op amps U1 and U2 use individual 3.0-Ω output ballast resistors, designated as Rb1 and Rb2. Though the OPA593 typical room temperature Vos (Ta = 25°C) is ±10 µV, it can increase to an overtemperature maximum of ±350 µV. The potentially higher Vos differences between U1 and U2 across temperature reinforces the need for ballasting to minimize the circulating current flow that can occur between their outputs.

The non-inverting of U1 is driven by a +5-Vdc source in the circuit diagram. Its output voltage when measured on the load side of Rb1 is 10 × 5 V, or 50 V. This occurs because Rb1 is within the feedback loop of U1. The voltage at U1 output adjusts to account for the voltage drop developed across Rb1 as the current through the resistor changes.

The follower amplifier U2 senses the voltage directly at the output of U1, and then the output of U2 follows precisely. If the U1 output voltage rises, the output voltage of U2 also rises and compensates for the voltage drop across Rb2 that occurs in response to an I2 increase. I1 and I2 move in unison each providing one-half the total load current I4, which in this example is 450 mA. The U1 and U2 voltage output moved up to +50.69 V, compensating for the 0.69 V voltage drops across Rb1 and Rb2 for the respective I1 and I2 output currents.

There is a reasonable amount of freedom when selecting the Rb1 and Rb2 ballast resistor (Rbal) values. Here are factors to consider to help establish their resistance:

- Always set Rb1 and Rb2 equal in value. The output currents I1 and I2 ratio in proportion to the resistance mismatch between them. A 1% resistance mismatch results in a 1% current imbalance.
- The higher the ballast resistance (Rbal) resistance value, the higher the voltage drop (V_{DROP}) and the higher the resistor power dissipation (Pd) at a particular output current level. The V_{DROP} limits the maximum Vo output swing range if set too high in resistance.
- The higher the Rbal resistance at the op amp output, the more output capacitive load isolation can be obtained. This increased output capacitive load helps in maintaining a higher phase margin. Details are provided in Section 2 - AC Considerations.
- The 3.0-Ω Rbal used for Rb1 and Rb2 in Figure 1-3 results in a good balance between performance and compromise for this OPA593 0.5 A (maximum) application.
- Rbal resistance is usually made lower as the output current range of an application increases. The 3.0 Ω Rbal used for each OPA593 op amp in this application is reasonably scaled to one-tenth the value (0.30 Ω) for a 5-A application.

The complete transfer function for the Leader-follower circuit is surprisingly mathematically involved, but when reduced to a simpler form, Vout is equal to:

Vi = V_{in} Figure 1-3

Vos1 = Input voltage offset of U1

$$Vout = Vi\frac{R1\times Rb1 + R1\times Rb2 + R2\times Rb1 + R2\times Rb2}{R2\times Rb1 + R2\times Rb2} + Vos1\frac{R1\times Rb1 + R1\times Rb2 + R2\times Rb1 + R2\times Rb2}{R2\times Rb1 + R2\times Rb2} \tag{1}$$

If Rb1 = Rb2, then

$$Vout = \left(Vi + Vos1\right)\left[1 + \frac{R1}{R2}\right] \tag{2}$$

Something that may not be immediately apparent with the Vout equation is that the U2 voltage offset voltage (Vos2), is absent from the transfer function. The full transfer function has two equal, but opposite Vos2 terms that directly cancel each other when Rb1 equals Rb2.

The fact that Vos2 cancels out does not mean that it does not have an effect on the circuit. In fact, any Vos2 present results in the U1 and U2 output currents being imbalanced. The higher the Vos2 voltage offset, the higher the imbalance will be. Since the OPA593 has very low Vos the imbalance due to Vos2 is minimal and not necessarily of concern. However, it might be more of an issue for higher power op amps having Vos on the order of millivolts, or more.

2 AC Considerations

The new component test application in consideration not only has the high 0.5-A output current requirement, but the added need to drive a load capacitance up to 1 µF and remain stable in the process. One microfarad is a high-capacitance load for most op amps to drive, including the OPA593. Compensation is required to assure stability, prevent oscillation, and retain good transient response characteristics.

Since the circuit must be compensated to drive the high-capacitance load it makes sense to have a plan going forward because the Leader-follower circuit has multiple loops; the U1 and U2 local loops, and a third loop that begins at the U1 output, goes to the U2 non-inverting input, and then back through Rb2 and Rb1. Compensation made to any one loop has some effect on the overall AC frequency response of the complete circuit. How to go about effectively compensating the circuit may not be readily evident and difficult to determine.

The approach documented here was to compensate U1 and U2 individually, as if each one independently drives the high-capacitive load. Next, evaluate the overall effectiveness of the stability compensation when they are connected back together. This approach turned out to work well for this OPA593 Leader-follower circuit.

Figure 2-1 shows the same circuit configuration as the Figure 1-3 circuit, but with the additional compensation components included. This circuit has proven completely effective driving a load consisting the 1-µF capacitor in parallel a resistance of 100 to 500 Ω. The resistor provides a real component to the load, but the circuit remains stable with just the capacitance. Both U1 and U2 compensated as in Figure 2-1 have an approximate 100-kHz unity-gain bandwidth, and maintain their 50-50 share of the output load current.

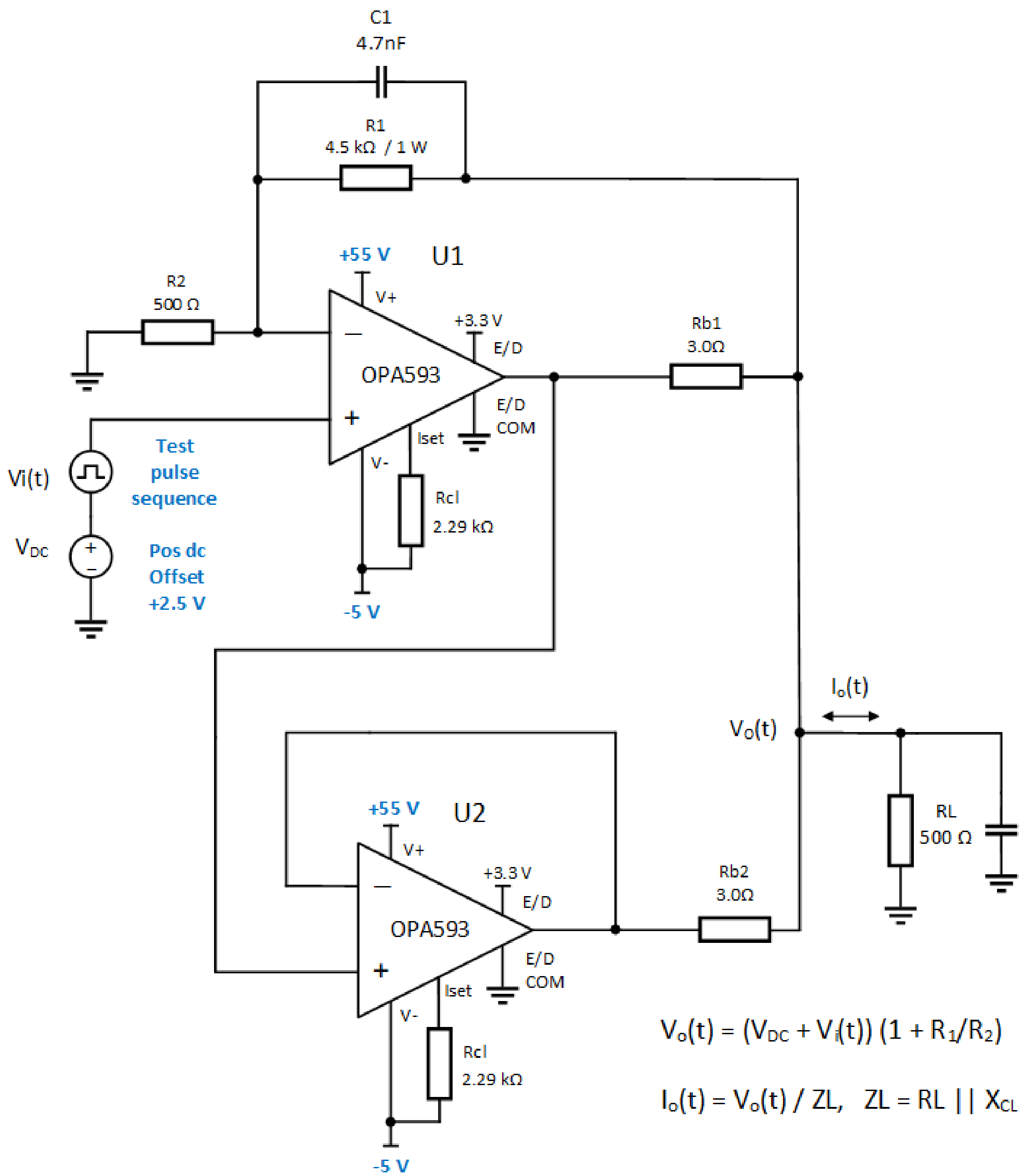

Figure 2-1. Leader-follower Parallel Output Amplifier With Compensation Included

The easiest place to start from a compensation explanation is with U2 in Figure 2-1. U2 is the same follower and 3.0-Ω series output ballast resistor as in the Figure 1-3 DC circuit. What may not be apparent is that Rb2 is doubling as an “Riso” output load isolation resistor now. Adding Riso is one method of compensating an op amp, increasing its ability to drive a high-capacitive load CL and remain stable doing so. A simplified version of the U2 circuit is illustrated in Figure 2-2 where the output ballast resistor is serving the additional function as Riso.

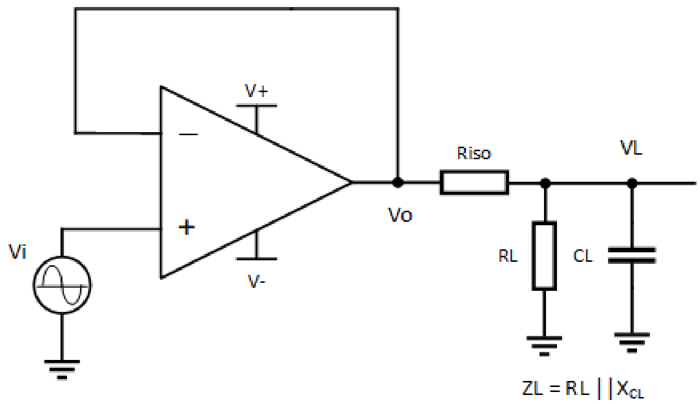

Figure 2-2. Operational Amplifier Riso Compensation for High Cload

The Riso compensation method is presented and further explained in the online: *TI Precision Labs Series – Amplifiers, Op amp Stability – Capacitive Loads*.

When the Riso compensation method is used with a single op amp as seen in Figure 2-2, a voltage divider is created by the Riso resistor and RL impedance to ground that follows it. The voltage at the divider output may be less than what is needed. However, when applied as it is in the Leader-follower circuit in Figure 2-1, the output voltage level is automatically corrected level by circuit configuration.

Compensation of U1 is a bit more involved than what was required for U2. As seen in Figures, its 3.0-Ω ballast resistor Rb1 is positioned within the feedback loop. It is not possible to move the Rb1 outside the loop without completely undoing the way the Figure 2-1 Leader-follower configuration is designed to function.

The U1 leader amplifier loaded with a 1-μF output load capacitor, and a 0-Ω Riso (Rb1) yields a phase margin of about 2 degrees. It is almost a certainty that the circuit would be unstable and oscillate. The 3.0-Ω Rb1 on U1 is within its local feedback loop and not outside the loop as is the case for Rb2 on U2. Despite Rb1 resistance being divided down by the loop gain of U1, it still provides a level of Riso resistance. Quite surprisingly, the phase margin increases to nearly 30 degrees. That is considered a marginally stable condition and the circuit should be stable. However, its transient behavior and bandwidth would be much different than those of the U2 circuit whose phase margin is about 70 degrees.

Additional compensation was needed at U1 to increase its phase margin and bandwidth to more closely match those of U2. This was accomplished by adding C1, a 4.7-nF capacitor, across the feedback resistor R1 on U1. This R1, C1 combination adds a pole to the (1/β) response of the inverse feedback factor at about 7.5 kHz. The loop-gain of U1 then breaks upward reducing the higher frequency roll-off rate from –40 dB/dec to –20 dB/dec. The net result is that the bandwidth of U1 increases to just above 100 kHz and its phase margin is close to that of U2.

Once the U1 and U2 stages were individually compensated, they are merged back together in the Leader-follower circuit. Some small deviations in the overall gain and phase responses are expected because they now interact with the AC responses of each other. However, simulations along with bench tests verified a completely stable output.

The Leader-follower circuit was tested with resistive loads, capacitive loads to 1 μF, and combinations of the two together. The circuit always remained stable with clean transient behavior. The overall phase margin approaches 60°.

3 Bench Test Results

The final test circuit of Figure 2-1 was realized by connecting two OPA593EVM evaluation modules together. The bench tests were intended to evaluate the OPA593 parallel 0.5-A output current capability, and to observe the output behaviors when loaded with different RL and CL loads. Figure 3-1 shows the two EVMs and the bench test equipment setup ready for testing.

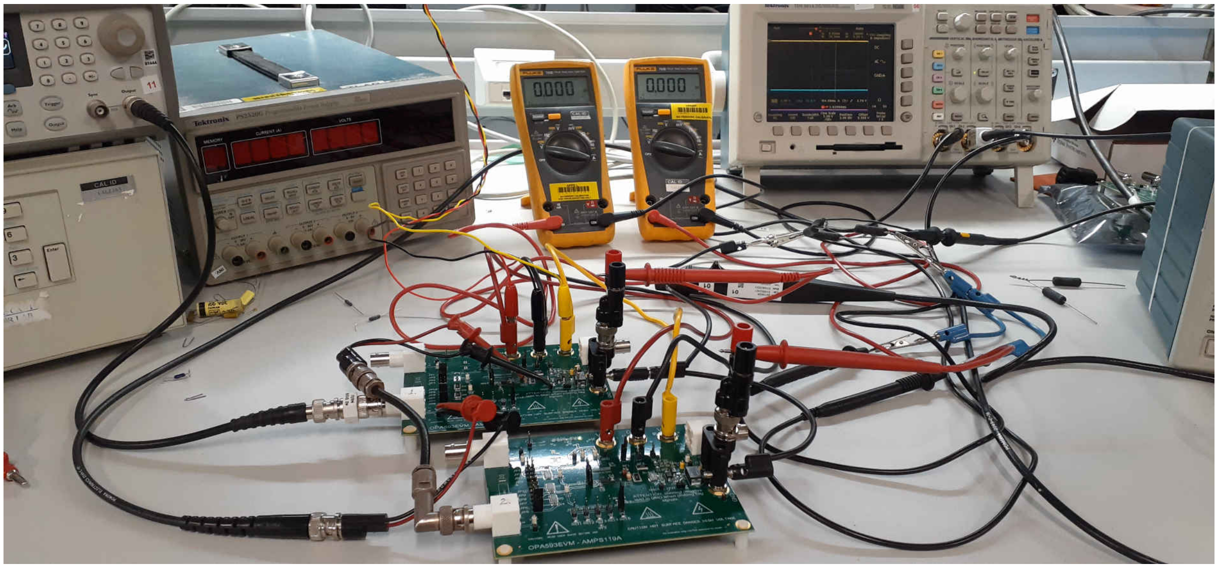

Figure 3-1. OPA593 Parallel Output Test Setup

The first test evaluated a sine-wave output of 0 to 50 V, developed across a 100 Ω, 20 W resistive load. This equated to 0.5-A peak output current. The OPA593EVM power supplies were set to +55 V and –5 V, and current-limit Rset resistors were set to 2.29 kΩ to set the maximum output current limit to about 250 mA for each OPA593EVM. Current limiting should then occur within the OPA593 ±5% rated limit is exceeded. The input stimulus was +2.5 Vdc, plus a 5 Vpp 1-kHz sine wave.

In Figure 3-2 the top trace is the +2.5 Vdc, plus a 5 Vpp 1-kHz sine measured at the U1 non-inverting input. The middle trace is the output sine waveform coming from the two OPA593 parallel outputs producing a peak-to-peak output that extends from 0 V to 50 V. The lower trace is a 200 mA/div current measurement acquired using a Tek TCPA300 AC/DC current probe. The trace verifies that a peak 0.5-A current is being produced by the parallel output amplifier when driving the 100-Ω load.

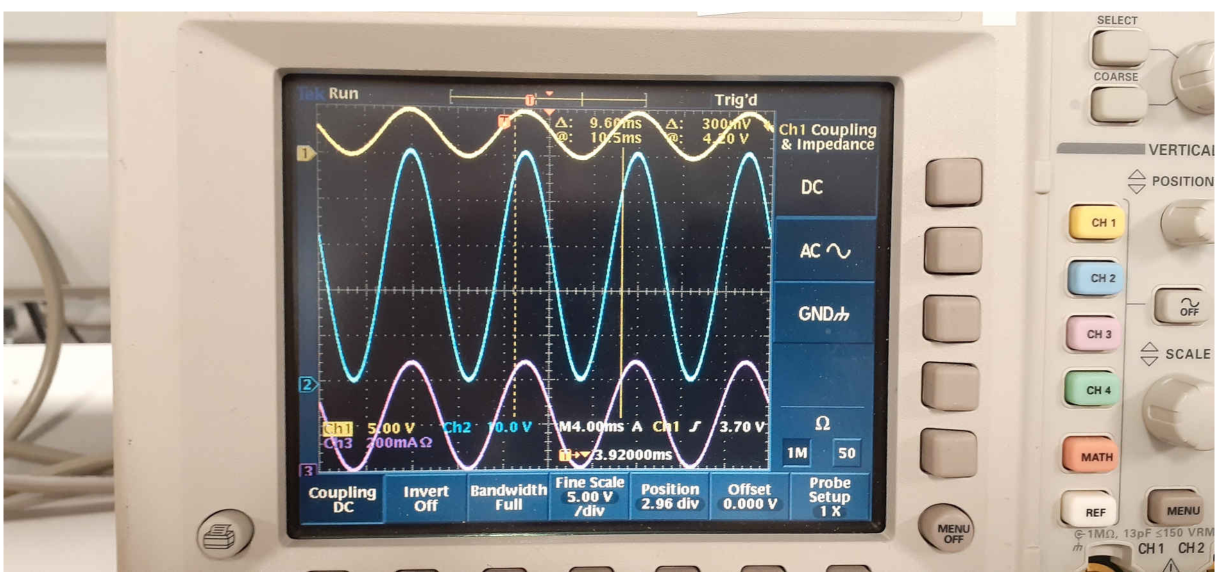

Figure 3-2. OPA593 Parallel Output Op Amp 0.5-A Peak Test Result

An attempt to drive the circuit harder and produce more output current resulted in one or both of the OPA593 op amps hitting their user-established automatic current limit of approximately 250 mA. The OPA593 EVM current-limit LED turned on when the internal current limit of the op amp was activated. As a consequence, the output sine wave became clipped on the current peaks verifying the current limiting was activated. This current-limit feature provides protection for both the OPA593 and the load it is driving.

The final test was to observe the behavior of the amplifier when driving a high-capacitance load up to 1 μF. This is the maximum capacitive load which the compensation of the circuit was designed to drive and remain stable doing so.

An indirect method that may be applied to evaluate the phase margin of an op-amp circuit involves a small-signal transient overshoot test (dominant 2-pole system). It is presented in TI's *Analog Engineer's Pocket Reference Guide* in the *Amplifier* section. The test applies a low-level step, or square-wave to the input of the amplifier. The output step is kept to about 50- to 100-mV peak to avoid slew rate limiting. Then, the overshoot amplitude is measured relative to the settled output amplitude. Figures 46 and 47 in the pocket reference show how the phase margin is estimated from a graph.

A phase margin of 45° is considered an acceptable margin, yielding stable operation. It corresponds to a signal overshoot of approximately 25%. Higher margin may be beneficial and a 90° phase margin produces no phase delay in the feedback loop and results in perfect damping.

Figure 3-3 shows the small-signal transient response of the OPA593 parallel output circuit when driving a parallel 1-μF and 500-Ω load to ground. The load resistance was increased so that the load was predominantly capacitive. The overshoot is minimal at just a few percent indicating a phase margin in the range of 60°. This agrees well with a PSpice simulation of the OPA593 parallel output that produced a similar margin.

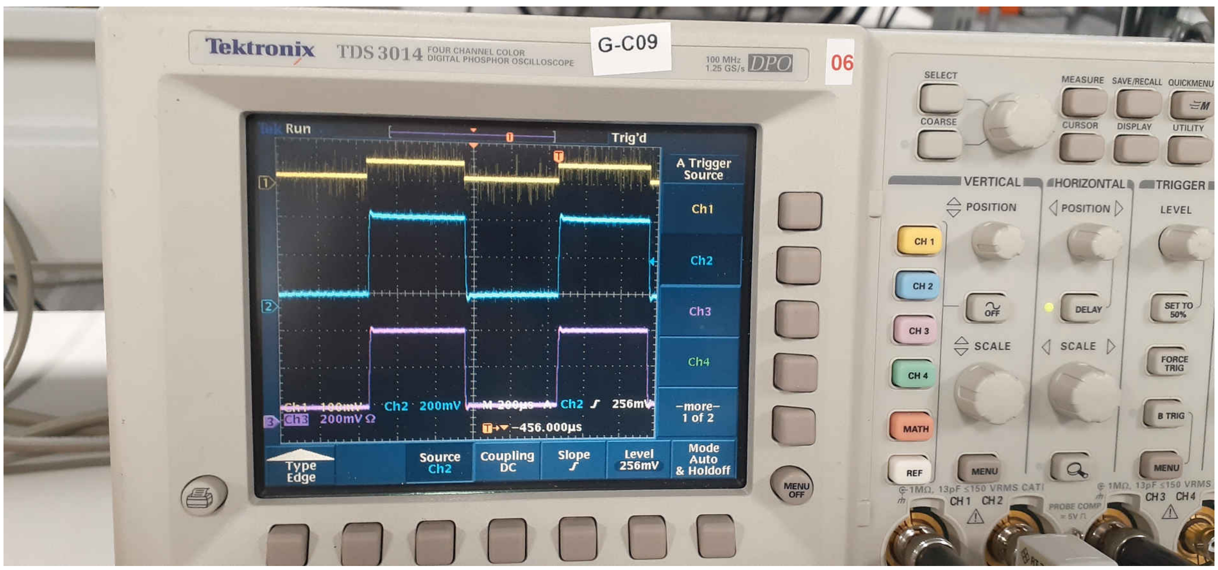

Figure 3-3. OPA593 Parallel Output Op Amp Small Signal Transient Response

Tests conducted with a large signal, square-wave output while driving a high-capacitive load of hundreds of nanofarads and 1 μF caused dim lighting of the OPA593EVM current-limit LEDs. The LED response was determined to be the result of the output current attempting to exceed the 250 mA set current limit of each EVM. This occurred during the transition of the output square wave from low level to high level. It was simply a matter of the edge transition current of the square wave, $i = C\, dv/dt$. The faster the edge rate, the higher the instantaneous current is for a particular load capacitance. The LED lighting was the result of the current limiting during the dv/dt event period.

4 Conclusion

A practical design for an OPA593 device in a Leader-follower parallel output configuration was developed and tested with good results. The circuit is applicable to numerous component test and analog power applications. Special attention was made to balancing the output current load shared between the two OPA593 high-voltage, high-current op amps. The circuit readily delivered a 0.5-A output current to a 100 Ω load. Particular attention was paid to compensating the amplifier circuit so that it could readily drive a high-capacitance 1-μF load. The OPA593 parallel output amplifier maintained complete stability for all output loads tested.