# OPA593 85-V, 250-mA Output Current, Precision Operational Amplifier

## 1 Features

- Low offset voltage: ±10 µV
- Low offset voltage drift: ±0.4 µV/°C
- High output current: 250 mA
- Low noise: 6 nV/√Hz at 10 kHz
- Rail-to-rail output
- Wide bandwidth: 10-MHz GBW
- High slew rate: 40 V/µs
- Wide supply: ±4 V to ±42.5 V, 8 V to 85 V
- Quiescent current: 3.25 mA
- Current limit accurate to 5%
- Disable function
- Overtemperature and overcurrent flags
- Temperature range: –40°C to +125°C
- Available in WSON package

## 2 Applications

- Semiconductor test
- Semiconductor manufacturing
- DC power supply, AC source, electronic load
- LCD test

## 3 Description

The OPA593 is a high-voltage (85 V), wide bandwidth (10 MHz), high-output-current (250 mA), unity-gain-stable operational amplifier.

The OPA593 uses a laser trimming technique to improve the offset voltage (10 µV) and offset voltage drift (0.4 µV/°C), thus avoiding the need for calibration. An external resistor can be used to limit the current (±5% accuracy), thus providing more precise measurements. In case of an overcurrent or overtemperature condition, the device indicates erroneous operation through a status flag. An included disable feature can be used to shutdown the device, saving power and placing the output into a high-impedance state.

The device is unity-gain stable, enabling operation as a high-impedance buffer, while the wide bandwidth (10 MHz) and high slew (40 V/µs) enable high signal gains. The high output current and capacitive drive allow the device to drive external FETs used to provide higher system currents, such as in a digital power supply.
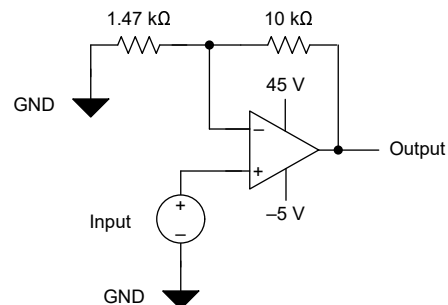
**Package Information**

| PART NUMBER | PACKAGE[1] | BODY SIZE (NOM) |
|---|---|---|
| OPA593 | WSON (12) | 4.00 mm × 4.00 mm |

(1) For all available packages, see the package option addendum at the end of the data sheet.
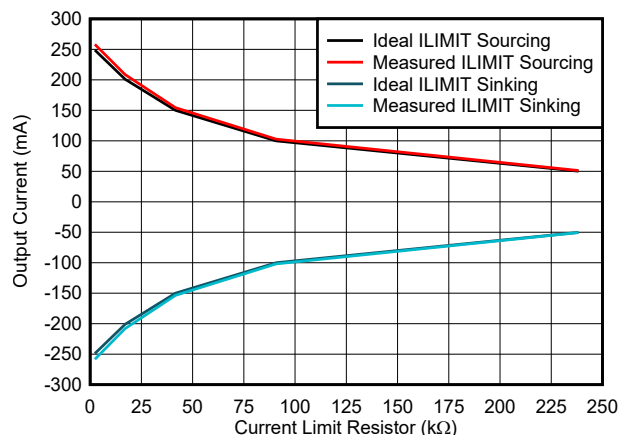


**Output Current vs Current-Limit Resistor Configuration**



**Output Driver Configured With a Gain of 8**

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## Table of Contents

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| **Changes from Revision A (March 2022) to Revision B (August 2022)** | **Page** |
|---|---|
| • Changed supply minimum voltage from ±5 V to ±4 V, and from 10 V to 8 V throughout document..................1 | |
| • Changed current limit accuracy from 10% to 5% in *Features* section.............................................. 1 | |

| **Changes from Revision * (January 2022) to Revision A (March 2022)** | **Page** |
|---|---|
| • Changed unit from Ω to kΩ to in Table 7-1, column 2, *Resistor* ..........................................9 | |

Product Folder Links: *OPA593*

# 5 Pin Configuration and Functions
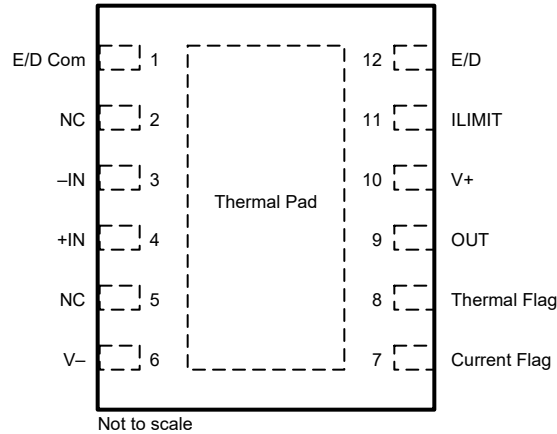


**Figure 5-1. DNT (12-Pin WSON) Package, Top View**

**Table 5-1. Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| Current Flag | 7 | Output | Overcurrent status flag |
| E/D | 12 | Input | Enable and disable |
| E/D Com | 1 | Input | Enable and disable common |
| ILIMIT | 11 | Input | Current limit |
| +IN | 4 | Input | Noninverting input |
| –IN | 3 | Input | Inverting input |
| NC | 2, 5 | — | No internal connection |
| OUT | 9 | Output | Output |
| Thermal Flag | 8 | Output | Overtemperature status flag |
| Thermal Pad | Thermal pad | — | The thermal pad is internally connected to V–. The thermal pad must be soldered to a printed-circuit board (PCB) connected to V–, even with applications that have low power dissipation. |
| V+ | 10 | Power | Positive (highest) power supply |
| V– | 6 | Power | Negative (lowest) power supply |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_S$ | Supply voltage, $V_S$ = (V+) – (V–) | | | 93 | V |
| | Signal input pin voltage[2] | | (V–) – 0.1 | (V+) + 0.1 | V |
| | E/D to E/D Com pin voltage | | | 5.5 | V |
| | ILIMIT pin voltage | | V– | (V–) + 3.35 | V |
| | All input pins current[2] | | | ±10 | mA |
| | Output short circuit current[3] | | | Continuous | |
| $T_A$ | Operating temperature | | –55 | 125 | °C |
| $T_J$ | Junction temperature | | | 150 | °C |
| $T_{STG}$ | Storage temperature | | –55 | 125 | °C |

(1)   Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2)   Input pins, Status Flag, E/D, and E/D Com, and Output are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails must be current-limited to 10 mA or less.
(3)   Short-circuit to ground.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±2000 | V |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2] | ±500 | |

(1)   JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2)   JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_S$ | Supply voltage, $V_S$ = (V+) – (V–) | Single supply voltage | 8 | | 85 | V |
| | | Dual supply voltage | ±4 | | ±42.5 | |
| $T_A$ | Operating temperature | | –40 | | 125 | °C |

## 6.4 Thermal Information

| | | OPA593 | UNIT |
|---|---|---|---|
| | | DNT (WSON) | |
| **THERMAL METRIC**[1] | | **12 PINS** | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 40.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 30.2 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 17.8 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.3 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 17.7 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 4.3 | °C/W |

(1)   For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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## 6.5 Electrical Characteristics

at $V_S$ = ±42.5 V, $T_A$ = 25°C, $R_L$ = 10 kΩ to mid-supply, $I_{OUT}$ limit set to 100 mA, and $V_{CM}$ = $V_{OUT}$ = mid-supply (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | |
| $V_{OS}$ | Input offset voltage | | | ±10 | ±100 | µV |
| $dV_{OS}/dT$ | Input offset voltage drift | $T_A$ = –40°C to +125°C | | ±0.4 | ±2 | µV/°C |
| PSRR | Power supply rejection ratio | $V_S$ = ±4 V to ±42.5 V | | 1 | 5 | µV/V |
| **INPUT BIAS CURRENT** | | | | | | |
| $I_B$ | Input bias current | $T_A$ = 25°C | | 10 | 20 | pA |
| | | $T_A$ = –40°C to +85°C | | | 500 | |
| | | $T_A$ = –40°C to +125°C | | | 1 | nA |
| $I_{OS}$ | Input offset current | | | 10 | 20 | pA |
| | | $T_A$ = –40°C to +85°C | | | 500 | |
| | | $T_A$ = –40°C to +125°C | | | 1 | nA |
| **NOISE** | | | | | | |
| | Input voltage noise | f = 0.01 Hz to 10 Hz | | 2.5 | | µV$_{PP}$ |
| $e_n$ | Input voltage noise density | f = 10 Hz | | 80 | | nV/√Hz |
| | | f = 1 kHz | | 8 | | |
| | | f = 10 kHz | | 6 | | |
| $i_n$ | Current noise density | f = 1 kHz | | 2 | | fA/√Hz |
| **INPUT VOLTAGE** | | | | | | |
| $V_{CM}$ | Common-mode voltage | Linear operation | (V–) – 0.1 | | (V+) – 3.5 | V |
| CMRR | Common-mode rejection | (V–) ≤ $V_{CM}$ ≤ (V+) – 3.5 V | 130 | 140 | | dB |
| | | $T_A$ = –40°C to +125°C, (V–) ≤ $V_{CM}$ ≤ (V+) – 3.5 V | 110 | 120 | | |
| **INPUT IMPEDANCE** | | | | | | |
| | Differential | | | $10^{13}$ ‖ 0.3 | | Ω ‖ pF |
| | Common-mode | | | $10^{13}$ ‖ 9.4 | | Ω ‖ pF |
| **OPEN-LOOP GAIN** | | | | | | |
| $A_{OL}$ | Open-loop voltage gain | (V–) + 0.3 V < $V_O$ < (V+) – 0.3 V, $R_L$ = 10 kΩ, $T_A$ = +25°C | 135 | 140 | | dB |
| | | (V–) + 0.3 V < $V_O$ < (V+) – 0.3 V, $R_L$ = 10 kΩ, $T_A$ = –40°C to +125°C | 120 | 140 | | |
| | | (V–) + 1 V < $V_O$ < (V+) – 1 V, $R_L$ = 2 kΩ, $T_A$ = +25°C | 110 | 130 | | |
| | | (V–) + 1 V < $V_O$ < (V+) – 1 V, $R_L$ = 2 kΩ, $T_A$ = –40°C to +125°C | 110 | 130 | | |
| | | (V–) + 2.5 V < $V_O$ < (V+) – 2.5 V, $R_L$ = 600 Ω, $T_A$ = +25°C | 100 | 120 | | |
| | | (V–) + 2.5 V < $V_O$ < (V+) – 2.5 V, $R_L$ = 600 Ω, $T_A$ = –40°C to +125°C | 100 | 120 | | |
| **FREQUENCY RESPONSE** | | | | | | |
| GBW | Gain-bandwidth product | | | 10 | | MHz |
| SR | Slew rate | Gain = ±1, $V_O$ = 70-V step | | 40 | | V/µs |
| $t_S$ | Settling time | To ±0.1%, gain = –1, $V_O$ = 70-V step, $C_L$ = 100 pF | | 0.75 | | µs |
| | | To ±0.01%, gain = –1, $V_O$ = 70-V step, $C_L$ = 100 pF | | 1.5 | | |
| THD+N | Total harmonic distortion + noise | Gain = +1, $V_O$ = 70 $V_{PP}$ f = 1 kHz, $R_L$ = 600 Ω | | -105 | | dB |
| | | Gain = +1, $V_O$ = 70 $V_{PP}$ f = 1 kHz, $R_L$ = 2 kΩ | | -110 | | |

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Product Folder Links: *OPA593*

## 6.5 Electrical Characteristics (continued)

at $V_S$ = ±42.5 V, $T_A$ = 25°C, $R_L$ = 10 kΩ to mid-supply, $I_{OUT}$ limit set to 100 mA, and $V_{CM}$ = $V_{OUT}$ = mid-supply (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OUTPUT** | | | | | | |
| $V_O$ | Voltage output swing from rail | No load | | 10 | 25 | mV |
| | | $I_{OUT}$ = 50 mA | | 50 | 125 | |
| | | $I_{OUT}$ = 100 mA | | 400 | 750 | |
| | | $I_{OUT}$ = 250 mA | | 1.2 | 2 | V |
| | Continuous output current, dc | $V_S$ = ±42.5 V | 200 | 250 | | mA |
| $C_{LOAD}$ | Capacitive load drive | | | See typical curves | | pF |
| $Z_O$ | Open-loop output impedance | | | See typical curves | | Ω |
| | Output impedance | Output disabled | | TBD | | Ω |
| | Output capacitance | Output disabled | | TBD | | pF |
| **CURRENT LIMIT** | | | | | | |
| $I_{LIMIT}$ | Current limit | | –250 | | +250 | mA |
| | Current limit accuracy | 25 mA ≤ $I_{OUT}$ ≤ 50 mA | | | 10 | % |
| | | 50 mA ≤ $I_{OUT}$ ≤ 250 mA | | | 5 | |
| | Current limit equation | $R_{CL}$ connected between ILMIT pin and V– pin supply | | (3.687 V * 4000) / (56.7 kΩ + $R_{CL}$) | | |
| **STATUS FLAG PIN (Referenced to E/D Com)** | | | | | | |
| | Status Flag delay | Overcurrent delay | | 10 | | µs |
| | | Overcurrent recovery delay | | 10 | | |
| | | Overtemperature delay | | 10 | | |
| | | Overtemperature recovery delay | | 10 | | |
| | Thermal shutdown | Alarm (status flag high) | | 170 | | °C |
| | | Return to normal operation (status flag low) | | 150 | | |
| | Status flag output voltage | Normal operation | | See typical curves | | |
| **E/D (ENABLE/DISABLE) PIN** | | | | | | |
| $V_{E/D}$ | Output enable voltage | Pin open or forced high | E/D Com + 2.5 | | E/D Com + 5 | V |
| | Output disable voltage | Pin forced low | E/D Com | | E/D Com + 0.65 | V |
| $I_E$ | Enable input current | | | 50 | | µA |
| | Output disable time | | | 10 | | µs |
| | Output enable time | | | 10 | | µs |
| **E/D COM PIN** | | | | | | |
| | E/D Com pin voltage | | (V–) | | (V+) – 6 | V |
| **POWER SUPPLY** | | | | | | |
| $I_Q$ | Quiescent current | | | 3.25 | 3.75 | mA |
| | | $T_A$ = –40°C to +125°C | | | 4 | |
| | | Output disabled | | 0.3 | | |

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## 6.6 Typical Characteristics

at $T_A$ = 25°C, $V_S$ = ±42.5 V, and $V_{CM}$ = $V_{OUT}$ = mid-supply (unless otherwise noted)
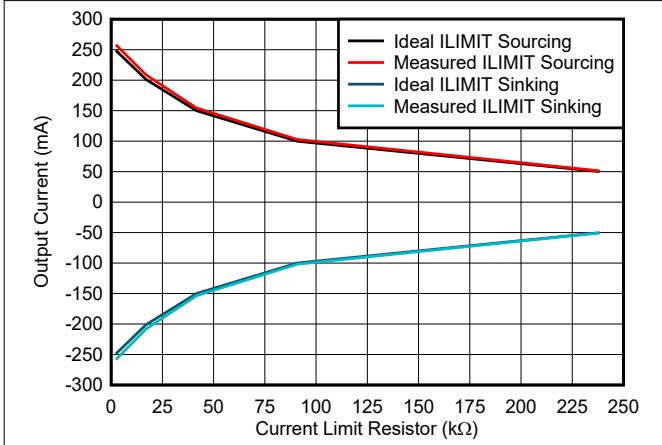


Figure 6-1. Output Current vs Current-Limit Resistor Configuration
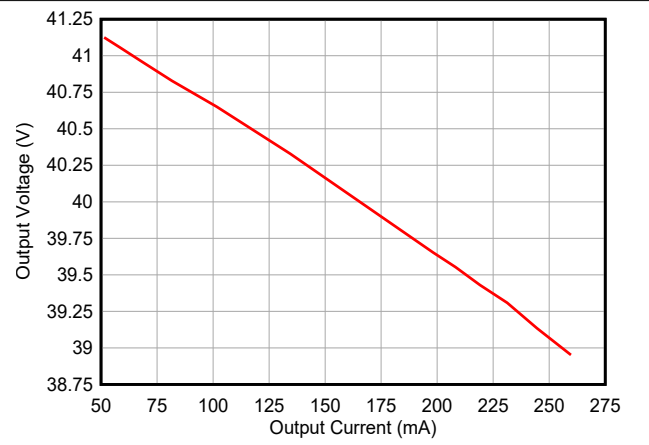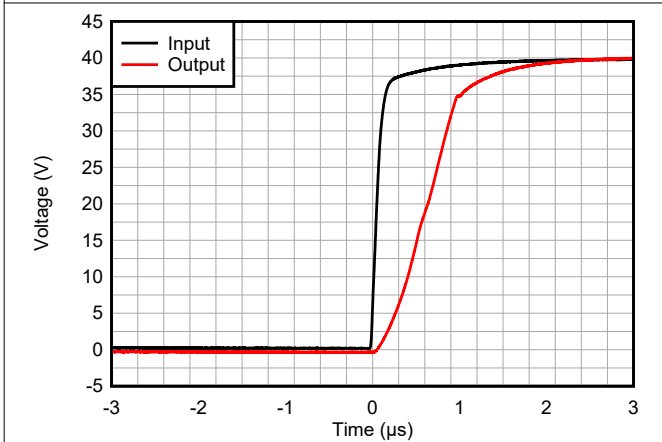


Figure 6-2. Output Voltage vs Output Current



Figure 6-3. Positive Slew
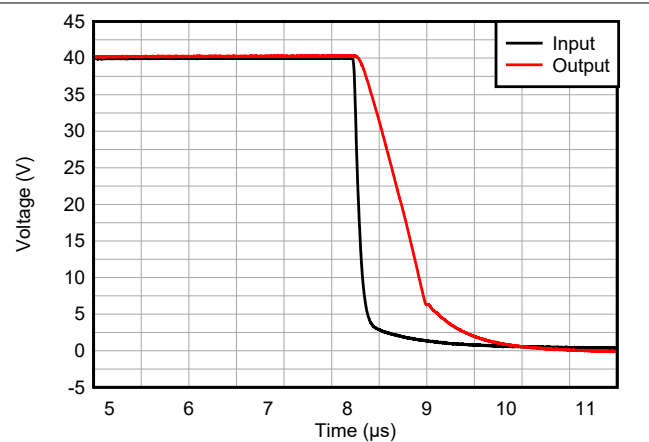


Figure 6-4. Negative Slew

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# 7 Detailed Description

## 7.1 Overview

The OPA593 is a high-voltage (85 V), power operational amplifier (op amp) with a high output current drive of 250 mA. The device features a current limit with an accuracy of ≤ 5% when the output current is greater than 50 mA. The current limit helps protect the system in the event of an output short to ground. Additionally, the device has two flags that indicate an overcurrent fault condition (beyond the configured limit) and an overtemperature fault condition (when the output stage shuts down to prevent damage to the device). Lastly, the output can be disabled to save system power and minimize thermal dissipation.

The unity-gain stable OPA593 has no phase inversion, a common-mode voltage range that includes the negative rail, a rail-to-rail output, and high dc precision. This device also has a wide signal range, 10 MHz of gain bandwidth, and high output current. All these features make the OPA593 an excellent choice as an output driver for a device under test (DUT) in automated test equipment (ATE) systems, or for signal processing in industrial systems using signals greater than 36 V.

## 7.2 Functional Block Diagram
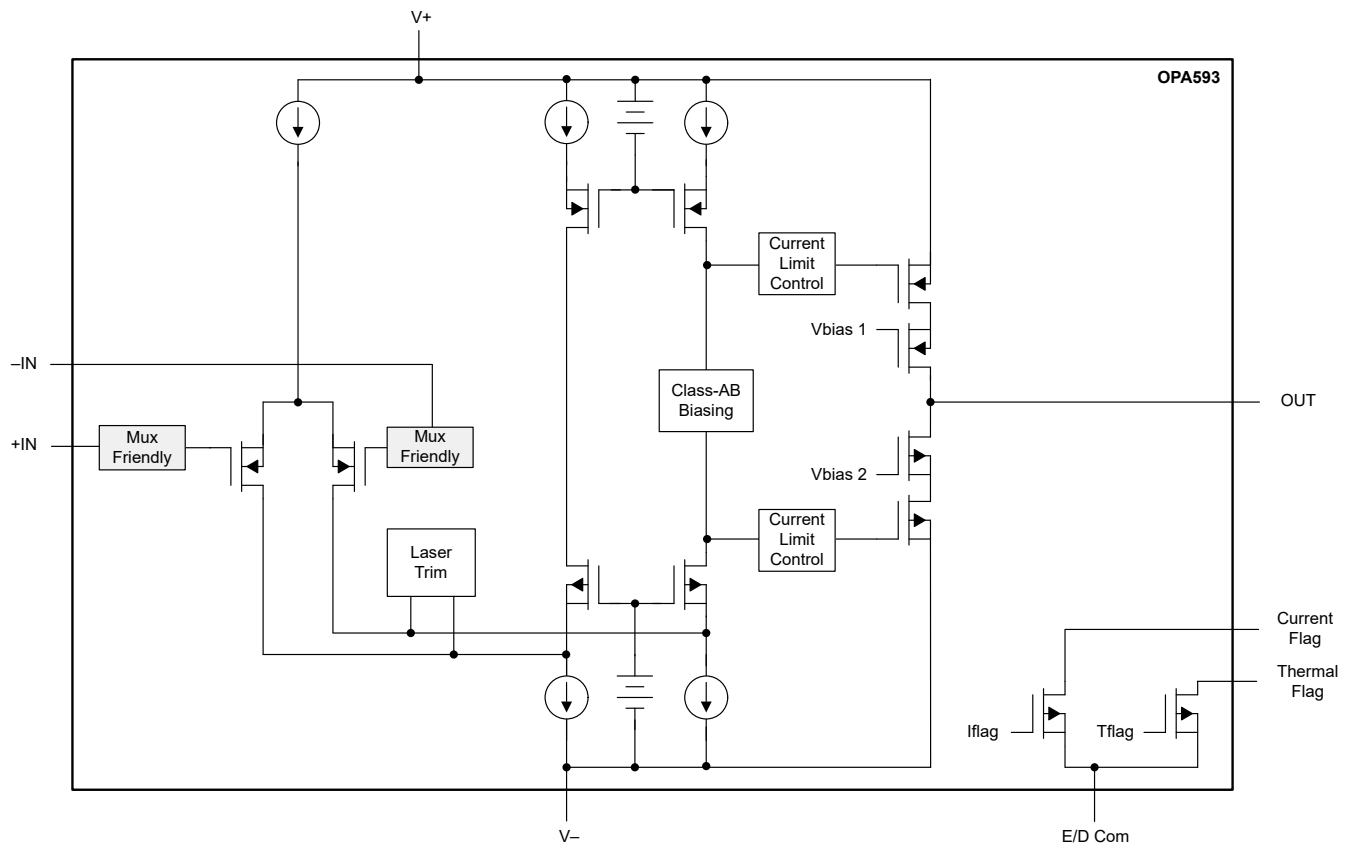
## 7.3 Feature Description

### 7.3.1 Current Limit

The OPA593 has a high-accuracy, externally programmable current limit that has a ±5% tolerance for output currents ≥ 50 mA. The current limit is set through the ILIMIT pin and is programmable from 10 mA to 250 mA (typical). A resistor can be used to limit the current to a fixed value or a digital-to-analog converter (DAC) can be used to vary the current limit during operation. Figure 7-1 shows a simplified diagram of the current-limit mirror configurations, as well as common resistor or DAC settings and the respective output current limit.
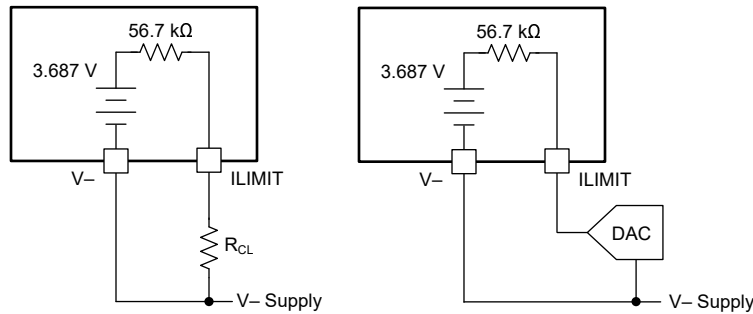


**Figure 7-1. OPA593 Internal Current Limit Configurations**

The most common configuration is to set the current limit using a resistor ($R_{CL}$) connected between the ILIMIT pin and the negative supply (V–). With this configuration, Equation 1 and Equation 2 are used to calculate the current limit based on the external resistor value or the resistor needed given the desired current limit value:

$$I_{LIMIT} = \frac{3.687\,V \times 4000}{56.7\,k\Omega + R_{CL}} \tag{1}$$

$$R_{CL} = \frac{3.687\,V \times 4000}{I_{LIMIT}} - 56.7\,k\Omega \tag{2}$$

An alternative to fixing the current limit to a single value using an external resistor is to use a DAC, which enables a variable current limit.

> **CAUTION**
> With this configuration, the output of the DAC must not exceed the ILIMIT specification in Section 6.1 to avoid reverse biasing the internal current limit circuitry and potentially damaging the device.

Use Equation 3 to set the current limit when a DAC is used ($V_{LIMIT}$ = DAC output voltage):

$$V_{LIMIT} = 3.687\,V - \frac{I_{LIMIT} \times 56.7\,k\Omega}{4000} \tag{3}$$

Several nominal current limit values along with their respective external resistor values and DAC output voltages are listed in Table 7-1.

**Table 7-1. Nominal Current-Limit Values**

| OUTPUT CURRENT LIMIT (mA) | RESISTOR (kΩ) | DAC VOLTAGE (V) |
|:---:|:---:|:---:|
| 50 | 237 | 2.98 |
| 100 | 90.9 | 2.27 |
| 200 | 16.9 | 0.85 |

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The current limit of the OPA593 has a ±10% tolerance for output currents between 25 mA and 50 mA, and is ±5% accurate for currents ≥ 50 mA. Any resistor or DAC tolerances add to the OPA593 tolerance, so take care when selecting the external components to make sure and provide the desired system level accuracy. Figure 7-2 shows a correlation between the ideal or calculated output current limit and the actual current limit as measured on the OPA593.
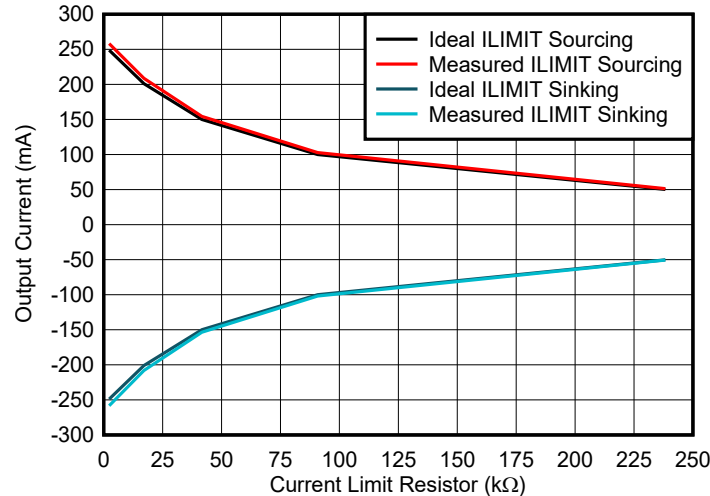


**Figure 7-2. Output Current vs Current-Limit Resistor Configuration**

### 7.3.2 Overcurrent Flag

The OPA593 features an overcurrent flag to indicate a condition where the output current draw attempts to exceed the limit configured through the ILIMIT pin, such as in a output short to ground fault condition. In such a situation, the internal current limit of the amplifier limits the output current to the configured value and the flag trips. This flag is an open-drain output designed to connect to standard low-voltage logic circuitry, such as a microcontroller (MCU).

### 7.3.3 Overtemperature Flag

The OPA593 features an internal thermal shutdown feature. The op amp output stage disables when the junction temperature reaches 170°C. After the junction temperature cools to 150°C, the output stage is enabled, and the op amp resumes normal operation. In the event of an overtemperature condition a thermal flag trips. This flag is an open-drain output designed to connect to standard low-voltage logic circuitry, such as an MCU.

### 7.3.4 Output Enable and Disable

The OPA593 incorporates an enable and disable feature that uses the E/D pin to disable the output stage of the amplifier, which lowers the power consumption of the op amp and switches the output to a high-impedance state.

The E/D pin is referenced to the E/D Com pin. If left floating, the E/D pin is internally pulled up to enable the device. If externally controlled, the E/D pin must be supplied with a voltage between 2.5 V and 5 V greater than the E/D Com pin voltage. Even though the OPA593 output is enabled with a floating E/D pin, a moderately fast, negative-going signal capacitively coupled to the E/D pin can overpower the internal pullup and cause device shutdown. If the enable function is not used, a conservative and recommended approach is to connect E/D through a 30-pF capacitor to a low-impedance source. Another alternative is to connect an external current source from V+ (positive supply) that is sufficient to hold the enable level greater than the shutdown threshold. Figure 7-3 shows a circuit that connects E/D and E/D Com.
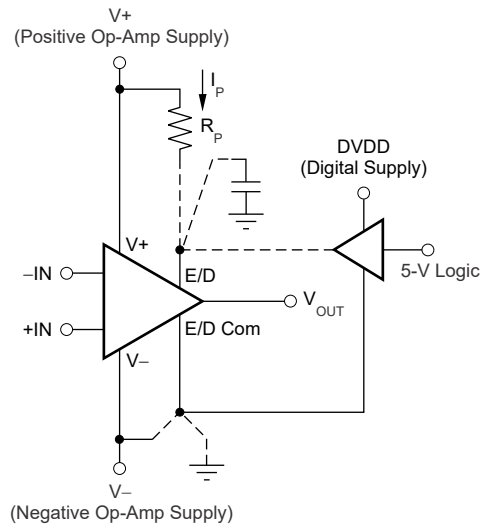


**Figure 7-3. E/D and E/D Com**

When the E/D pin is dropped to a voltage between 0 V and 0.65 V greater than the E/D Com pin voltage, the output of the OPA593 is disabled. Because the inputs are still active, an input signal can be passed to the output of the amplifier, despite being in a high-output-impedance state. The voltage at the amplifier output is reduced because of a drop across this output impedance, and can appear distorted compared to a normal operation output.

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### 7.3.5 Mux-Friendly Inputs

The OPA593 uses a unique input architecture to eliminate the need for input protection diodes but still provides robust input protection under transient conditions. Conventional input diode protection schemes shown in Figure 7-4 can be activated by fast transient step responses and can introduce signal distortion and settling time delays because of alternate current paths, as shown in Figure 7-5. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes that cause an increase in input current, resulting in extended settling time.
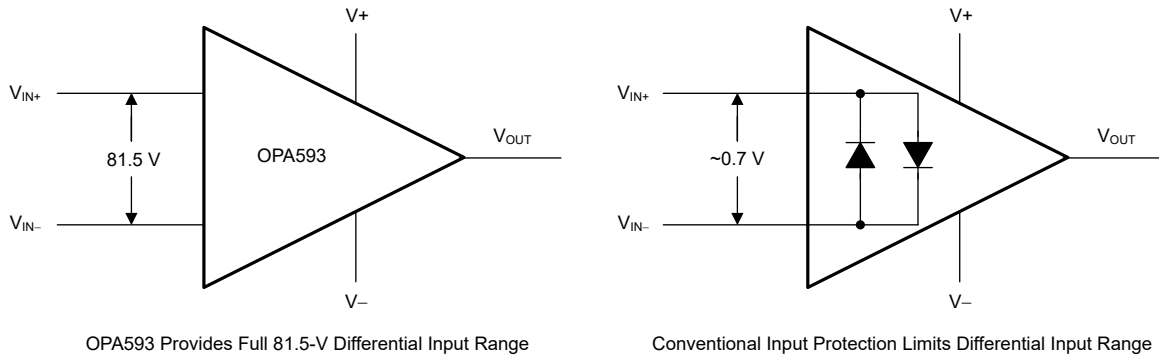


OPA593 Provides Full 81.5-V Differential Input Range    Conventional Input Protection Limits Differential Input Range

**Figure 7-4. OPA593 Input Protection Does Not Limit Differential Input Capability**



*Input Low-Pass Filter*          *Simplified Mux Model*          *Buffer Amplifier*
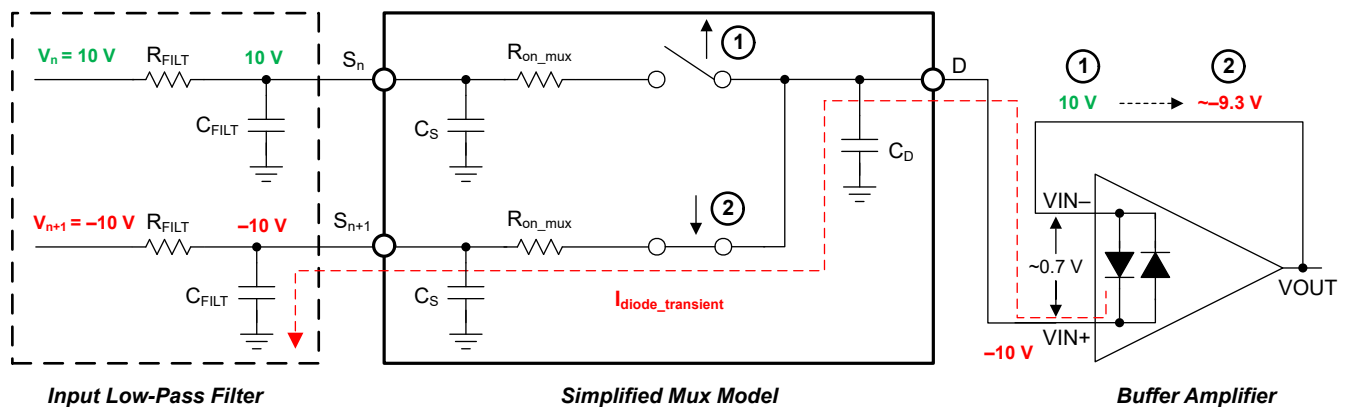
**Figure 7-5. Back-to-Back Diodes Create Settling Issues**

The OPA593 a true high-impedance differential input capability for high-voltage applications. This patented input protection architecture does not introduce additional signal distortion or delayed settling time, making this device an excellent choice for multichannel, high-switched, input applications. The OPA593 tolerates a maximum differential swing (voltage between inverting and noninverting pins of the op amp) of up to 85 V, making this device a great choice for use as a comparator or in applications with fast-ramping or switched input signals.

### 7.4 Device Functional Modes

The OPA593 has two modes of operation. The first mode is normal operation where the amplifier is enabled, either by supply a voltage to the enable-disable (E/D) pin that is between 2.5 V and 5 V greater than the E/D Com pin. The second mode of operation is a lower-power, disabled state where the E/D pin is driven between 0 V and 0.65 V greater than the E/D Com pin. In this state, the amplifier output is disabled and enters a high output impedance state.

Product Folder Links: *OPA593*

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# 8 Application and Implementation

> **Note**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

The OPA593 is a high-voltage, high output current op amp. The device is capable of operating with supplies as low as ±4 V (8 V) and as high as ±42.5 V (85 V), with an output current up to 250 mA and an internal current limit with an accuracy of up to ±5%. Thanks to the small size, high operating voltage range, output current, and high dc precision, the device is designed for operating as a high gain stage, driving heavy loads and conditional large signals. The additional features of the OPA593, including the current limit, overcurrent, and overtemperature flags, thermal protection, output disable and mux-friendly inputs, help the device protect both the op amp and the system from potential damage due to various fault conditions.
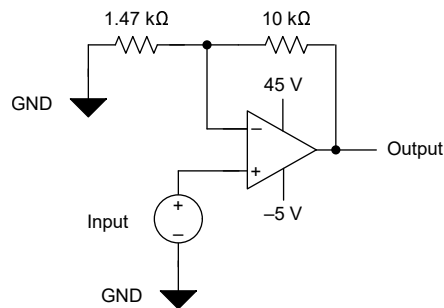
## 8.2 Typical Application



**Figure 8-1. Output Driver Configured With a Gain of 8**

### 8.2.1 Design Requirements

The OPA593 is designed for use as an output driver stage with gain thanks to the wide supply voltage and high output current with programmable current limit. These features combined with the small size of the DNT package (4 mm x 4 mm) makes this device a great choice for high-channel density systems such as semiconductor test and manufacturing platforms where many channels can be present. In this design, the OPA593 is configured for a gain of 8. A small negative supply is provided so that if the application requires a small output voltage, such as in the case of a device under test (DUT) continuity check, the amplifier is able to provide the output without being limited by the negative rail (that is, saturating the output).

**Table 8-1. Design Parameters**

| PARAMETER | VALUE |
|---|---|
| Supply voltage | +45 V, –5 V |
| Input voltage | 0 V to 5 V |
| Output voltage | 0 V to 40 V |
| System gain | 8 |
| Output current | Up to 250 mA |

Product Folder Links: *OPA593*

ADVANCE INFORMATION

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### 8.2.2 Detailed Design Procedure

In this design example, the OPA593 is configured as both a gain and output driver stage. The input signal to the amplifier is 0 V to 5 V and the device is configured with a positive gain of 8. This configuration results in an output voltage of 0 V to 40 V. The supply voltages are selected to provide adequate headroom so that the amplifier can sink or source up to 250 mA without slamming the output into the rail, while minimizing the swing from the supply to the output to minimize the thermal dissipation of the device.

This simple design example is common in many systems using a DAC to provide the input signal and require a wide output signal with high output current. Such systems include test & measurement platforms and power supplies.

Figure 8-2 shows the input and output signal of this OPA593 circuit.
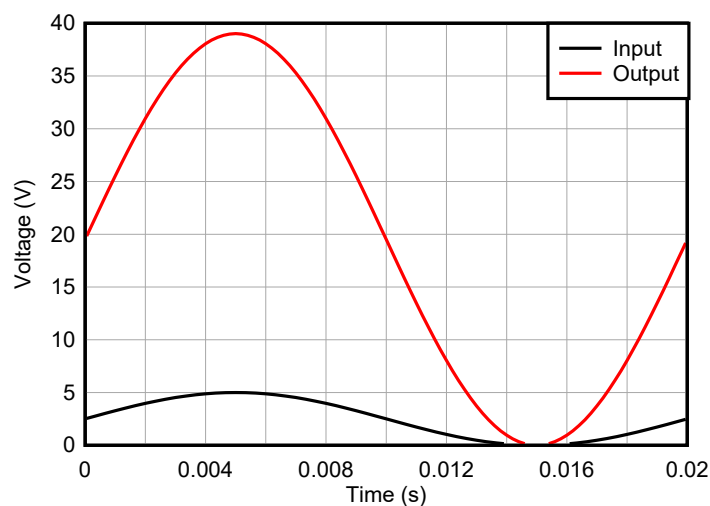
### 8.2.3 Application Curve



**Figure 8-2. OPA593 Output Driver Circuit, Input and Output Signals**

Product Folder Links: *OPA593*

## 8.3 Power Supply Recommendations

The OPA593 operates from power supplies up to ±42.5 V, or a total of 85 V, with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. A power-supply bypass capacitor of at least 0.1 µF is required for proper operation. Make sure that the capacitor voltage is rated for high voltage across the full operating temperature range. Parameters that vary significantly with operating voltage are shown in Section 6.6.

Some applications do not require an equal positive and negative output voltage swing. Power-supply voltages do not have to be equal. The OPA593 operates with as little as 8 V between the supplies, and with up to 85 V between the supplies.

## 8.4 Layout

### 8.4.1 Layout Guidelines

During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat is conducted away from the package into either a ground plane or other heat-dissipating device. Always solder the thermal pad to the PCB, even with applications that have low power dissipation. Follow these steps to attach the device to the PCB:

1. Connect the thermal pad to the most negative supply voltage on the device, V–.
2. Prepare the PCB with a top-side etch pattern. There must be etching for the leads, as well as etching for the thermal pad.
3. Thermal vias improve heat dissipation, but are not required. The thermal pad can connect to the PCB using an area equal to the pad size with no vias, but must be externally connected to V–.
4. Place recommended holes in the area of the thermal pad. Recommended thermal land size and thermal via patterns for the SON-12 DNT package are shown in the thermal land pattern mechanical drawing appended at the end of this document. Keep the holes small, so that solder wicking through the holes is not a problem during reflow. Use a 0.2-mm size via with a minimum of five connected directly below the thermal pad.
5. Additional vias can be placed anywhere along the thermal plane outside of the thermal pad area. These vias help dissipate the heat generated by the OPA593 device. These additional vias can be larger than the vias directly under the thermal pad because the additional vias are not in the thermal pad area to be soldered; thus, wicking is not a problem.
6. Connect all holes to the internal power plane of the correct voltage potential, V–.
7. When connecting these holes to the plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations, making the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the OPA593 WSON package must make the connections to the internal plane with a complete connection around the entire circumference of the plated-through hole.
8. The top-side solder mask must leave the pins of the package and the thermal pad area exposed. The bottom-side solder mask must cover the holes of the thermal pad area. This masking prevents solder from being pulled away from the thermal pad area during the reflow process.
9. Apply solder paste to the exposed thermal pad area and all of the device pins.
10. With these preparatory steps in place, simply place the device in position, and run through the solder reflow operation as with any standard surface-mount component.
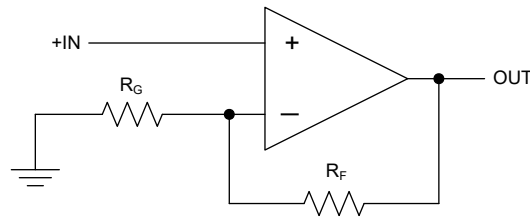
**ADVANCE INFORMATION**

### 8.4.2 Layout Example



**Figure 8-3. Schematic Representation**
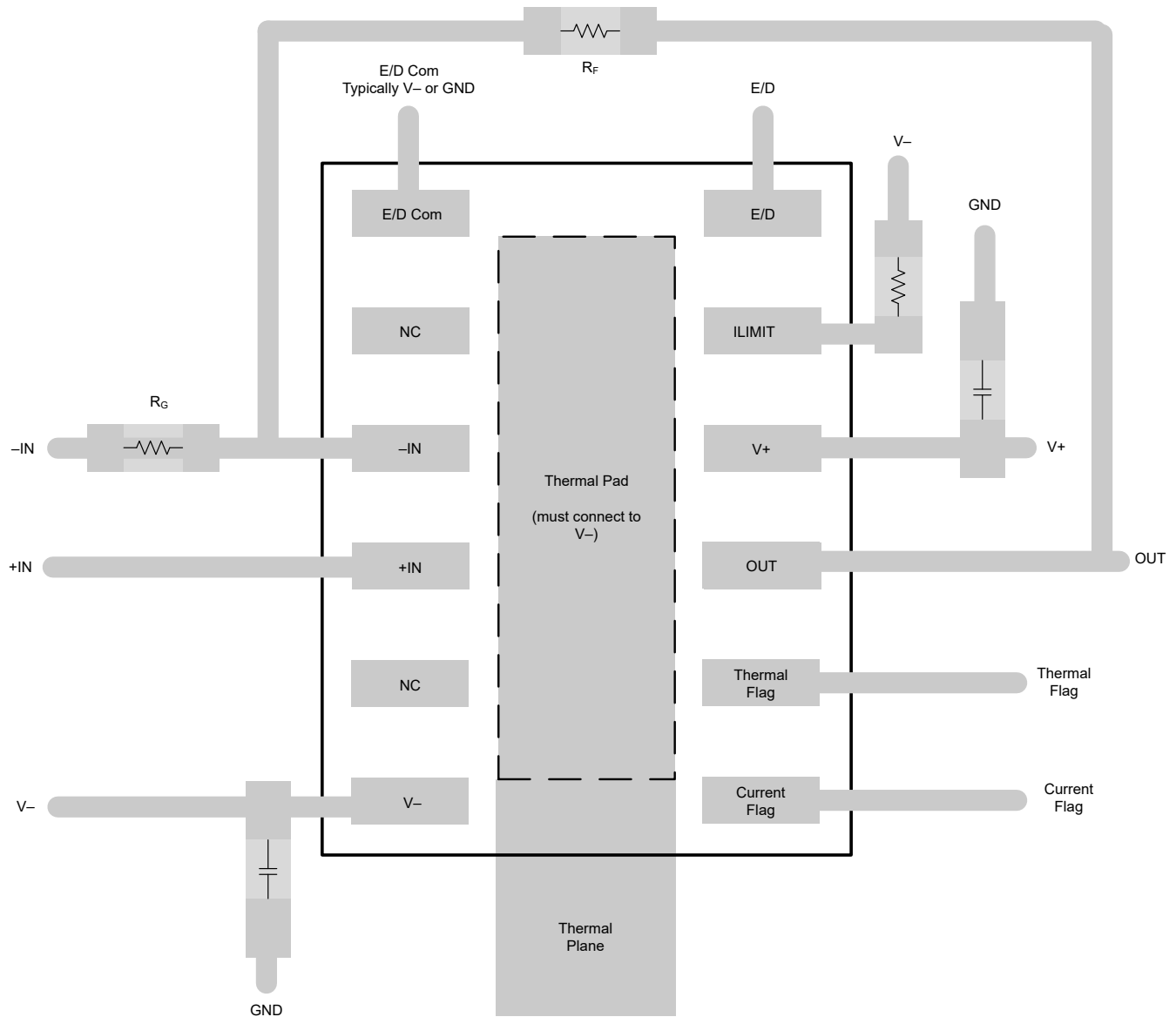


**Figure 8-4. OPA593 Board Layout for Noninverting Configuration**

Product Folder Links: *OPA593*

# 9 Device and Documentation Support

## 9.1 Device Support

### 9.1.1 Development Support

#### 9.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

#### 9.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design tools and simulation web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

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**Note**

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

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## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 9.4 Trademarks

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## 9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

TI Glossary          This glossary lists and explains terms, acronyms, and definitions.

**ADVANCE INFORMATION**

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

# PACKAGE OPTION ADDENDUM

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| XOPA593DNTR | ACTIVE | WSON | DNT | 12 | 5000 | TBD | Call TI | Call TI | -40 to 125 | | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:**  TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
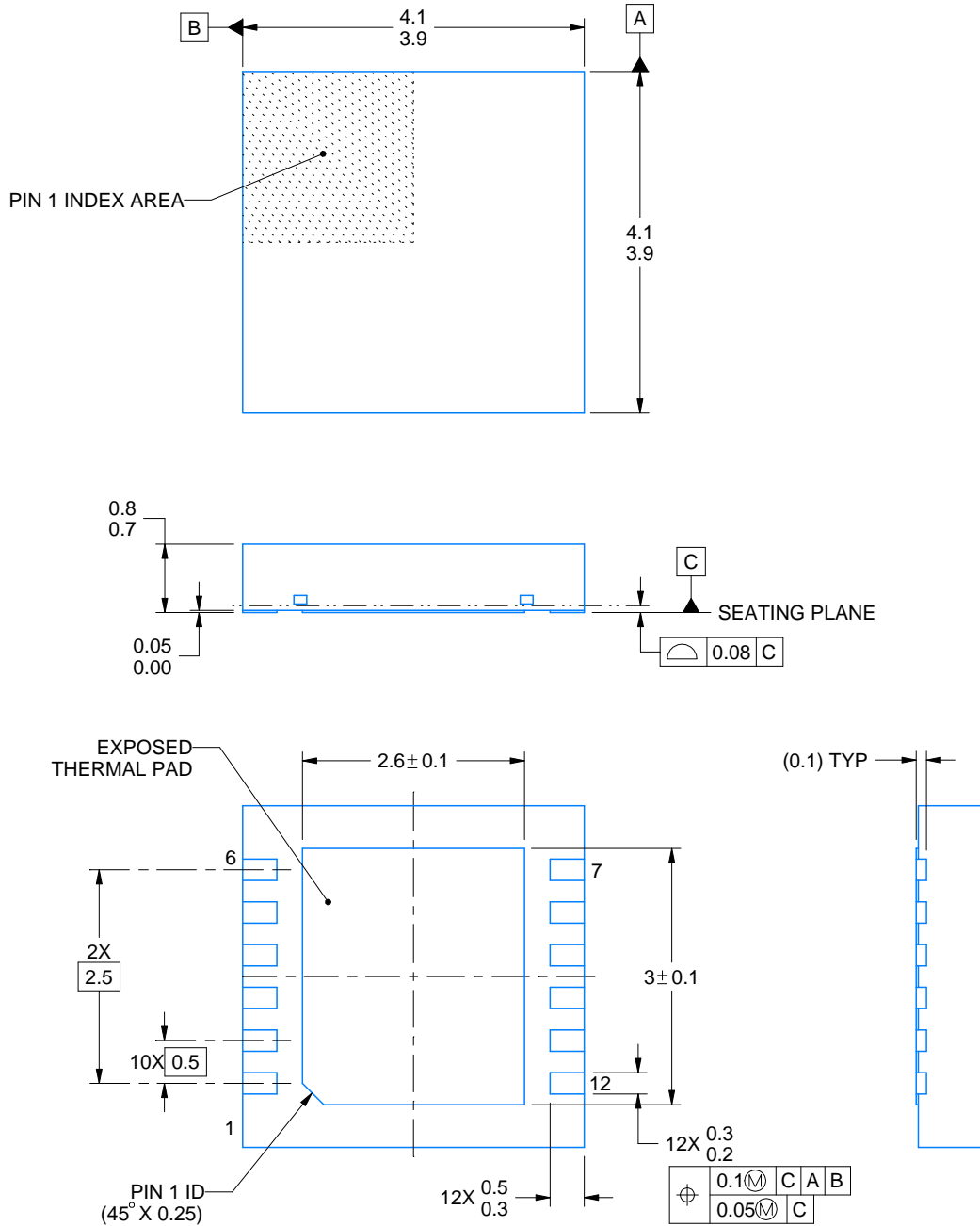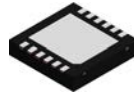
**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

4.1
3.9

B

A

PIN 1 INDEX AREA

4.1
3.9

0.8
0.7

C

SEATING PLANE

0.05
0.00

0.08 C

EXPOSED
THERMAL PAD

2.6 ± 0.1

(0.1) TYP

6

7

2X
2.5

3 ± 0.1

10X 0.5

12

1

12X 0.3
0.2

PIN 1 ID
(45° X 0.25)

12X 0.5
0.3

0.1 Ⓜ C A B
0.05 Ⓜ C
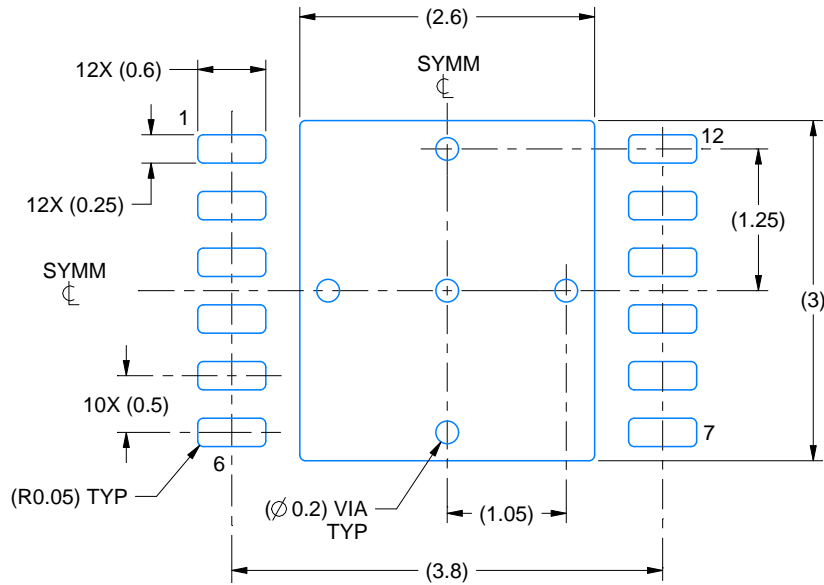
4214928/C   10/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

12X (0.6)

12X (0.25)

10X (0.5)

(R0.05) TYP

(2.6)

SYMM

SYMM

1

6

(∅ 0.2) VIA
TYP

(1.05)

(3.8)

12

(1.25)

(3)

7

**LAND PATTERN EXAMPLE**
EXPOSED METAL SHOWN
SCALE:15X

0.07 MAX
ALL AROUND

EXPOSED METAL

SOLDER MASK
OPENING

METAL

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

EXPOSED METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

SOLDER MASK
DEFINED
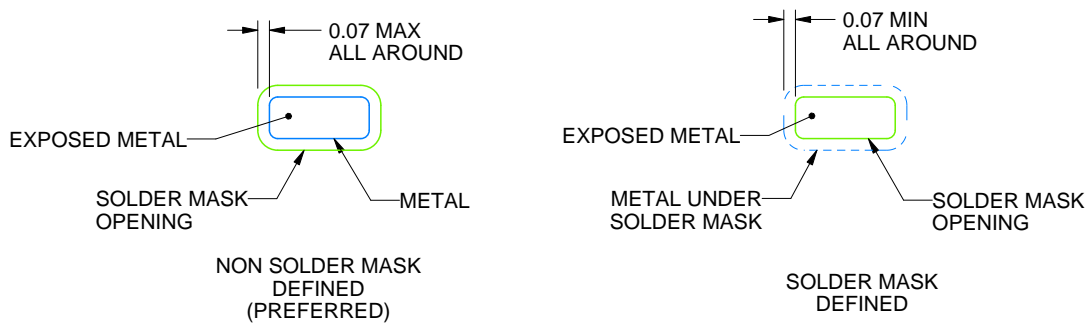
**SOLDER MASK DETAILS**

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

# DNT0012B

SYMM

METAL
TYP

12X (0.6)

(0.68)

1

12X (0.25)

12

10X (0.5)

(0.76)

SYMM

(R0.05) TYP

6

7

4X
(1.31)

4X (1.15)

(3.8)
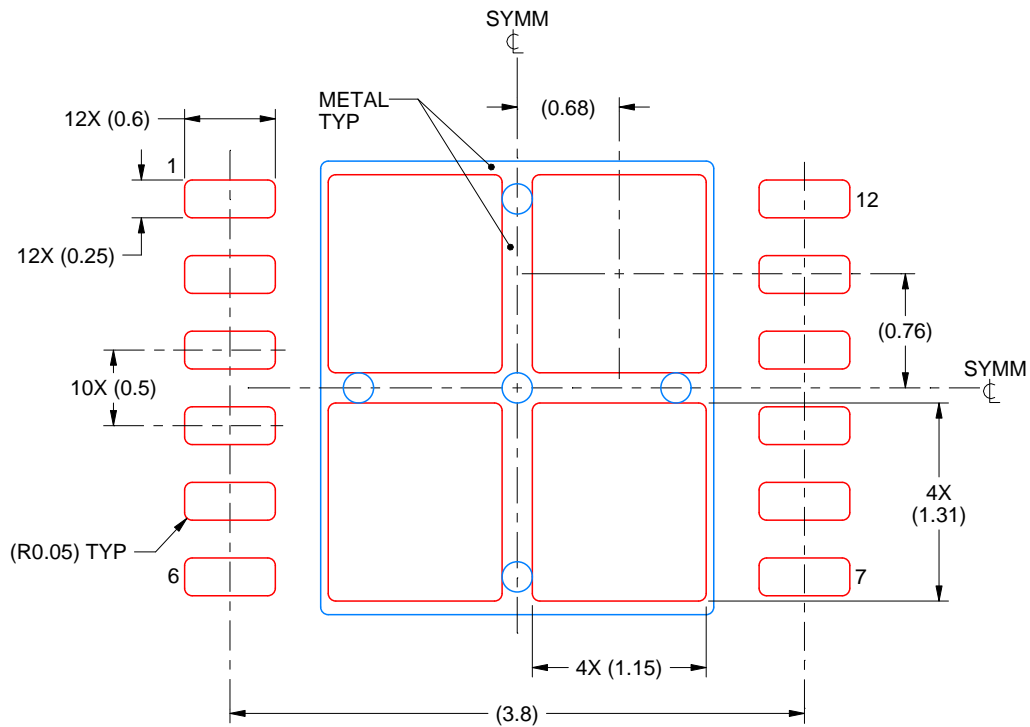
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.

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