# OPA817 800-MHz, High-Precision, Unity-Gain Stable, FET-Input Operational Amplifier

## 1 Features

- Wide bandwidth:
  - Gain-bandwidth product: 390 MHz
  - Bandwidth (G = 1 V/V): 800 MHz
  - Large-signal bandwidth (2 $V_{PP}$): 245 MHz
  - Slew rate: 970 V/µs
- High precision:
  - Input offset voltage: 250 µV (maximum)
  - Input offset voltage drift: 4 µV/°C (maximum)
- Input voltage noise: 4.5 nV/√Hz
- Input bias current: 4 pA
- Low distortion ($R_L$ = 100 Ω, $V_O$ = 2 $V_{PP}$):
  - HD2, HD3 at 10 MHz: –86 dBc, –99 dBc
- Supply range: 6 V to 12.6 V
- Supply current: 23.5 mA
- Shutdown current: 55 µA
- Performance upgrade to OPA656

## 2 Applications

- High-speed data acquisition (DAQ)
- Active probes
- Oscilloscopes
- Wideband transimpedance amplifiers (TIAs)
- Wafer scanning equipment
- Optical communication modules
- Optical time-domain reflectometry (OTDR)
- Test and measurement front-ends
- Medical and chemical analyzers

## 3 Description

The OPA817 is a unity-gain stable, voltage-feedback operational amplifier for high-speed, high-precision and wide dynamic range applications.

The OPA817 has a low-noise junction gate field-effect transistor (JFET) input stage that features a wide gain-bandwidth of 390-MHz and a supply range from 6-V to 12.6-V. The fast slew rate of 970-V/µs allows a wide large-signal bandwidth and low distortion when used as high impedance buffer in high-speed digitizers, active probes and other test and measurement applications.

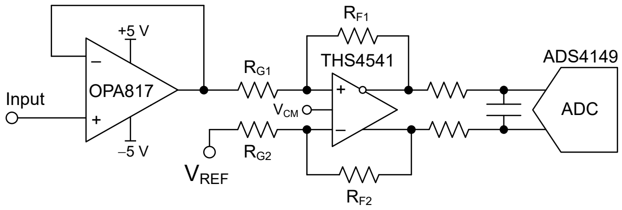
The OPA817 offers extremely low input offset voltage of ±250-µV and offset voltage drift of ±4-µV/°C. The combination of pico-amperes of input bias current and low input voltage noise (4.5-nV/√Hz) makes the OPA817 an ideal wideband transimpedance amplifier in optical test and communication equipment as well as medical and scientific instrumentation.

The OPA817 is available in an 8-lead WSON package with an exposed thermal pad for heat dissipation. This device is specified to operate over the industrial temperature range of –40°C to +105°C.

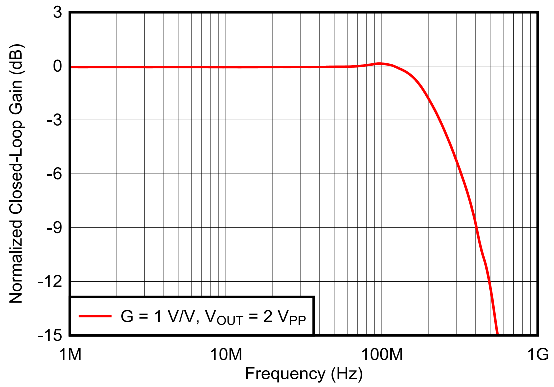
**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| OPA817 | WSON (8) | 3.00 mm × 3.00 mm |

(1) For all available packages, see the package option addendum at the end of the data sheet.



High Input Impedance Digitizer Front-End



Large-Signal Frequency Response

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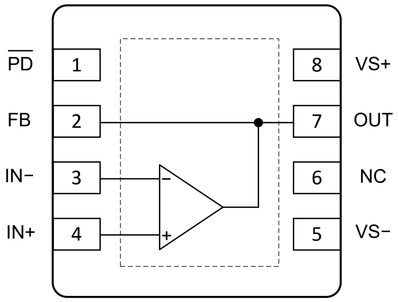
## 4 Revision History

| DATE | REVISION | NOTES |
|---|---|---|
| July 2022 | * | Initial Release |

## 5 Device Comparison Table

| DEVICE | Supply Voltage (V) | BW (MHz) | Input | SLEW RATE (V/µs) | VOLTAGE NOISE (nV/√Hz) | MINIMUM STABLE GAIN (V/V) |
|---|---|---|---|---|---|---|
| OPA817 | ±6.3 | 390 | FET | 970 | 4.5 | 1 |
| OPA818 | ±6.5 | 2700 | FET | 1400 | 2.2 | 7 |
| OPA657 | ±5 | 1600 | FET | 700 | 4.8 | 7 |
| OPA656 | ±5 | 230 | FET | 290 | 7 | 1 |
| OPA659 | ±6 | 350 | FET | 2550 | 8.9 | 1 |
| OPA858 | ±2.5 | 5500 | CMOS | 2000 | 2.5 | 7 |
| THS4631 | ±15 | 210 | FET | 1000 | 7 | 1 |

## 6 Pin Configuration and Functions



Not to scale

NC - no internal connection

**Figure 6-1. DTK Package, 8-Pin WSON With Thermal Pad (Top View)**

**Table 6-1. Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| FB | 2 | O | Feedback resistor connection (optional) |
| IN– | 3 | I | Inverting input |
| IN+ | 4 | I | Noninverting input |
| NC | 6 | — | No connect (no internal connection to die) |
| OUT | 7 | O | Output of amplifier |
| $\overline{\text{PD}}$ | 1 | I | Power down (low = amplifier enabled, high = amplifier disabled); internal 2-MΩ pull-up allows floating this pin |
| VS– | 5 | P | Negative power supply |
| VS+ | 8 | P | Positive power supply |
| Thermal pad | | — | Electrically isolated from the die substrate. The thermal pad can be connected to any potential between the device power-supplies, but it is recommended to connect it to a heat-spreading plane, typically ground. |

(1) I = input, O = output, P = power

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_S$ | Total supply voltage ($V_{S+}$ – $V_{S–}$) | | 13 | V |
| $V_I$ | Input voltage | $V_{S–}$ | $V_{S+}$ | V |
| $V_{ID}$ | Differential input voltage | | $\pm V_S$ | V |
| $I_I$ | Continuous input current | | ±10 | mA |
| | Continuous power dissipation | See Thermal Information | | |
| $T_J$ | Maximum junction temperature | | 150 | °C |
| $T_A$ | Operating free-air temperature | –40 | 105 | °C |
| $T_{stg}$ | Storage temperature | –65 | 125 | °C |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2) | ±1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{S+} – V_{S–}$ | Total supply voltage | 6 | 10 | 12.6 | V |
| $T_A$ | Ambient temperature | –40 | 25 | 105 | °C |

## 7.4 Thermal Information

| THERMAL METRIC(1) | | OPA817 | UNIT |
|---|---|---|---|
| | | DTK (WSON) | |
| | | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 64.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 53.0 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 32.8 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 1.3 | °C/W |
| $Y_{JB}$ | Junction-to-board characterization parameter | 32.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 9.0 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

### 7.5 Electrical Characteristics: $V_S = \pm 5$ V

At G = 1 V/V, $R_F = 0\ \Omega$ for G = 1 V/V, $R_F = 250\ \Omega$ for other gains, $R_L = 100\ \Omega$ referenced to mid-supply, input and output referenced to mid-supply, and $T_A \cong 25°C$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **AC PERFORMANCE** | | | | | | |
| SSBW | Small-signal bandwidth | $V_{OUT} = 200\ \text{mV}_{PP}$ | | 800 | | MHz |
| | | $V_{OUT} = 200\ \text{mV}_{PP}$, G = 2 V/V | | 425 | | |
| | | $V_{OUT} = 200\ \text{mV}_{PP}$, G = 5 V/V | | 100 | | |
| | | $V_{OUT} = 200\ \text{mV}_{PP}$, G = 10 V/V | | 40 | | |
| GBWP | Gain-bandwidth product | $V_{OUT} = 200\ \text{mV}_{PP}$, G = 100 V/V | | 390 | | MHz |
| LSBW | Large-signal bandwidth | $V_{OUT} = 2\ \text{V}_{PP}$ | | 245 | | MHz |
| | | $V_{OUT} = 4\ \text{V}_{PP}$ | | 140 | | |
| | Bandwidth for 0.1-dB flatness | $V_{OUT} = 2\ \text{V}_{PP}$ | | 100 | | MHz |
| SR | Slew rate (10% to 90%) | $V_{OUT}$ = 4–V step | | 970 | | V/μs |
| | Slew rate (10% to 90%) | $V_{OUT}$ = 1–V step, Gain = 2 V/V | | 900 | | |
| $t_R$, $t_F$ | Rise, fall time | $V_{OUT}$ = 200–mV step | | 1.5 | | ns |
| | Settling time to 0.1%, | $V_{OUT}$ = 2–V step | | 6 | | ns |
| | Overshoot and undershoot | $V_{OUT}$ = 2–V step | | 8 | | % |
| | Output Overdrive recovery time | $V_{OUT} = V_{S-}$ to $V_{S+}$, G = 2 V/V, | | 15 | | ns |
| HD2 | Second-order harmonic distortion | f = 1 MHz, $V_{OUT} = 2\ \text{V}_{PP}$ | | –100 | | dBc |
| | | f = 10 MHz, $V_{OUT} = 2\ \text{V}_{PP}$ | | –86 | | |
| | | f = 50 MHz, $V_{OUT} = 2\ \text{V}_{PP}$ | | –70 | | |
| | | f = 10 MHz, $V_{OUT} = 2\ \text{V}_{PP}$, $R_L = 1\ \text{k}\Omega$ | | –100 | | |
| HD3 | Third-order harmonic distortion | f = 1 MHz, $V_{OUT} = 2\ \text{V}_{PP}$ | | –120 | | dBc |
| | | f = 10 MHz, $V_{OUT} = 2\ \text{V}_{PP}$ | | –99 | | |
| | | f = 50 MHz, $V_{OUT} = 2\ \text{V}_{PP}$ | | –66 | | |
| | | f = 10 MHz, $V_{OUT} = 2\ \text{V}_{PP}$, $R_L = 1\ \text{k}\Omega$ | | –100 | | |
| $e_N$ | Input voltage noise | f ≥ 200 kHz | | 4.5 | | nV/√Hz |
| | Voltage noise 1/f corner frequency | | | 2.6 | | kHz |
| | Input current noise | | | 18 | | fA/√Hz |
| **DC PERFORMANCE** | | | | | | |
| $A_{OL}$ | Open-loop voltage gain | $V_{OUT} = \pm 1$ V | 78 | 85 | | dB |
| | | $T_A$ = –40°C to +85°C | 72 | | | |
| | | $T_A$ = –40°C to +105°C | 69 | | | |
| $V_{OS}$ | Input-referred offset voltage | | | 50 | 250 | μV |
| | | $T_A$ = –40°C to +85°C | | | 500 | |
| | | $T_A$ = –40°C to +105°C | | | 600 | |
| | Input offset voltage drift | $T_A$ = –40°C to +85°C | | 1 | 4 | μV/°C |
| | | $T_A$ = –40°C to +105°C | | 1 | 4 | |
| $I_B$ | Input bias current | | | 2 | 20 | pA |
| | | $T_A$ = –40°C to +85°C | | | 1250 | |
| | | $T_A$ = –40°C to +105°C | | | 2500 | |
| $I_{OS}$ | Input offset current | | | 1 | 20 | pA |
| | | $T_A$ = –40°C to +85°C | | | 700 | |
| | | $T_A$ = –40°C to +105°C | | | 1250 | |
| | Internal feedback trace resistance | Device turned OFF, OUT to FB pin resistance | | 0.7 | | Ω |

## 7.5 Electrical Characteristics: $V_S$ = ±5 V (continued)

At G = 1 V/V, $R_F$ = 0 Ω for G = 1 V/V, $R_F$ = 250 Ω for other gains, $R_L$ = 100 Ω referenced to mid-supply, input and output referenced to mid-supply, and $T_A$ ≅ 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT** | | | | | | |
| | Most positive input voltage(1) | | 2.1 | 2.7 | | V |
| | | $T_A$ = –40°C to +85°C | 2.0 | | | |
| | | $T_A$ = –40°C to +105°C | 2.0 | | | |
| | Most negative input voltage(1) | | | -3.9 | -3.5 | V |
| | | $T_A$ = –40°C to +85°C | | | -3.4 | |
| | | $T_A$ = –40°C to +105°C | | | -3.4 | |
| CMRR | Common-mode rejection ratio | $V_{CM}$ = ±0.5 V | 92 | 110 | | dB |
| | | $T_A$ = –40°C to 85°C | 91 | | | |
| | | $T_A$ = –40°C to 105°C | 90 | | | |
| | Input impedance common-mode | | | 60 \|\| 2.9 | | GΩ \|\| pF |
| | Input capacitance differential mode | | | 0.1 | | pF |
| **OUTPUT** | | | | | | |
| $V_{OL}$ | Output voltage, low | no-load | | -3.9 | -3.6 | V |
| | | $R_L$ = 100 Ω | | -3.7 | -3.4 | |
| | | $T_A$ = –40°C to +85°C | | | -3.3 | |
| | | $T_A$ = –40°C to +105°C | | | -3.2 | |
| $V_{OH}$ | Output voltage, high | no-load | 3.7 | 3.9 | | V |
| | | $R_L$ = 100 Ω | 3.4 | 3.7 | | |
| | | $T_A$ = –40°C to +85°C | 3.3 | | | |
| | | $T_A$ = –40°C to +105°C, | 3.2 | | | |
| | Linear output drive (sourcing/sinking) | $V_{OUT}$ = ±1 V, $\Delta V_{OS}$ < 2 mV | ±58 | 80 | | mA |
| | | $T_A$ = –40 to 85°C, $\Delta V_{OS}$ < 3 mV | ±40 | | | |
| | | $T_A$ = –40 to 105°C, $\Delta V_{OS}$ < 3 mV | ±35 | | | |
| | Short-circuit current | | | 100 | | mA |
| $Z_O$ | Closed loop output Impedance | f = 100 kHz | | 0.04 | | Ω |
| **POWER SUPPLY** | | | | | | |
| $I_Q$ | Quiescent current | | | 23.5 | 24.2 | mA |
| | | $T_A$ = –40°C to +85°C | | | 24.4 | |
| | | $T_A$ = –40°C to +105°C | | | 24.5 | |
| PSRR+ | Power-supply rejection ratio | $\Delta V_{S+}$ = ±0.5 V | 81 | 100 | | dB |
| | | $T_A$ = –40°C to +85°C | 77 | | | |
| | | $T_A$ = –40°C to +105°C | 76 | | | |
| PSRR- | Power-supply rejection ratio | $\Delta V_{S-}$ = ±0.5 V, | 81 | 100 | | dB |
| | | $T_A$ = –40°C to +85°C | 77 | | | |
| | | $T_A$ = –40°C to +105°C | 76 | | | |

## 7.5 Electrical Characteristics: $V_S$ = ±5 V (continued)

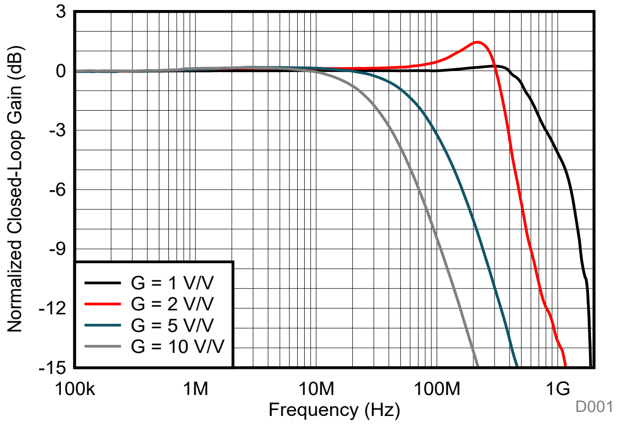
At G = 1 V/V, $R_F$ = 0 Ω for G = 1 V/V, $R_F$ = 250 Ω for other gains, $R_L$ = 100 Ω referenced to mid-supply, input and output referenced to mid-supply, and $T_A$ ≅ 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER DOWN** | | | | | | |
| | Enable voltage threshold | Specified *on* above ($V_{S+}$) – 1 V | | | 4 | V |
| | Disable voltage threshold | Specified *off* below ($V_{S+}$) – 3 V | 2 | | | V |
| | Power-down quiescent current | $\overline{PD}$ ≤ ($V_{S+}$) – 3V | | 55 | 100 | uA |
| | Power-down pin bias current in shutdown mode | $\overline{PD}$ = 0 V to ($V_{S+}$) – 3 V | | 9 | 12 | uA |
| | Power-down pin bias current in active mode | $\overline{PD}$ = ($V_{S+}$) – 1 V to ($V_{S+}$) | | 0.5 | 1 | uA |
| | Turn-on time delay | Time from $\overline{PD}$ voltage exceeds threshold to $V_{OUT}$ = 90% of final value, $V_{IN}$ = 1V | | 0.3 | | µs |
| | Turn-off time delay | Time from $\overline{PD}$ voltage reduces below threshold to $I_Q$ = 10% of active mode value | | 0.1 | | µs |

(1) Input range for CMRR > 77-dB.

## 7.6 Typical Characteristics: $V_S$ = ±5 V

At G = 1 V/V, $R_F$ = 0 Ω for G = 1 V/V, $R_F$ = 250 Ω for other gains, $R_L$ = 100 Ω referenced to mid-supply, input and output referenced to mid-supply, and TA ≅ 25°C (unless otherwise noted).



$V_{OUT}$ = 200 mV$_{PP}$

Figure 7-1. Noninverting Small-Signal Frequency Response

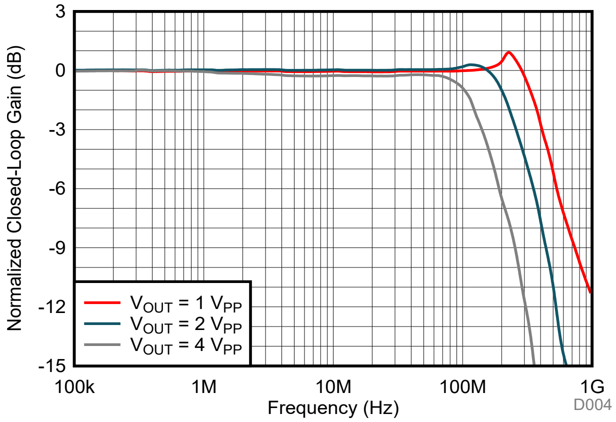


Figure 7-2. Noninverting Large-Signal Frequency Response

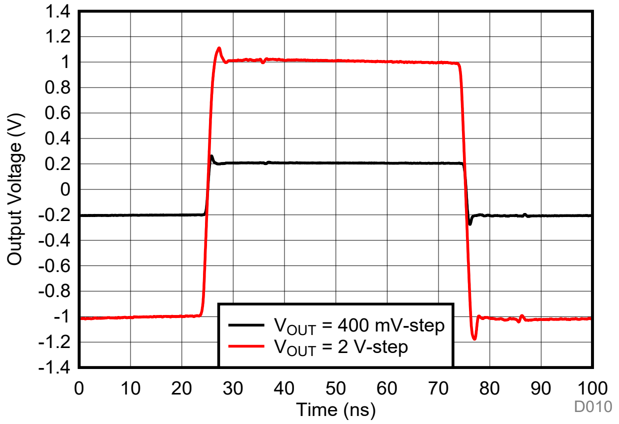


Figure 7-3. Noninverting Large-Signal Pulse Response

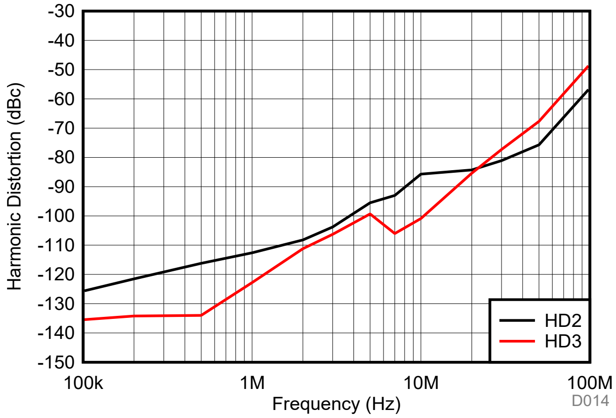


Figure 7-4. Harmonic Distortion vs Frequency

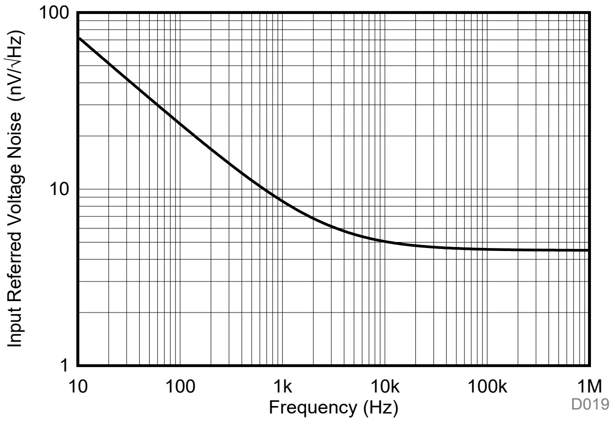


Figure 7-5. Voltage Noise Density vs Frequency

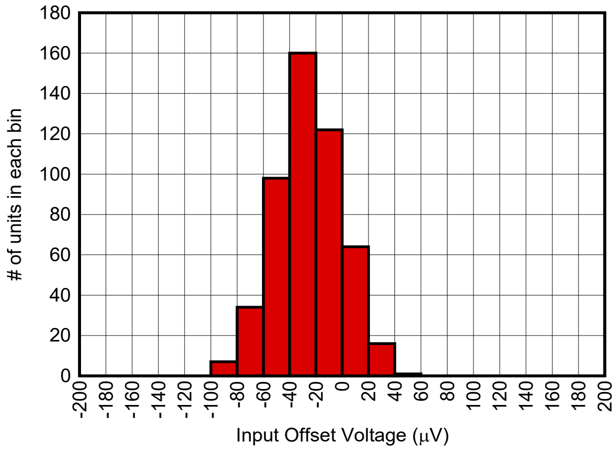


Figure 7-6. Input Offset Voltage Histogram

# 8 Detailed Description

## 8.1 Overview

The OPA817 is a high voltage, unity gain stable, 390 MHz gain-bandwidth product (GBWP), voltage feedback operational amplifier (op amp) featuring a 4.5 nV/√Hz low noise JFET input stage. The low offset voltage (250 µV maximum), offset voltage drift (4 µV/°C maximum), and unity gain bandwidth of 800 MHz makes it ideal for high input impedance, high-speed data acquisition front-ends. The high voltage capability combined with 970 V/µs slew rate enables applications needing wide output swings (9 $V_{PP}$ at $V_S$ = 12 V) for high-frequency signals such as those often found in medical instrumentation, optical front-end, test, and measurement applications. The low noise JFET input with pico-amperes of bias current makes the device attractive in high-gain TIA applications and in test and measurement front-ends. OPA817 also features a power-down mode that disables the core amplifier for power savings.

The OPA817 is built using TI's proprietary high-voltage, high-speed, complementary bipolar SiGe process.

## 8.2 Functional Block Diagram

The OPA817 is a conventional voltage feedback op amp with two high-impedance inputs and a low-impedance output. Figure 8-1 and Figure 8-2 shows two standard amplifier configuration examples that are supported for this device. The reference voltage ($V_{REF}$) level shifts the DC operating point for each configuration, which is typically set to mid-supply in single-supply operation. $V_{REF}$ is typically set to ground in split-supply applications.

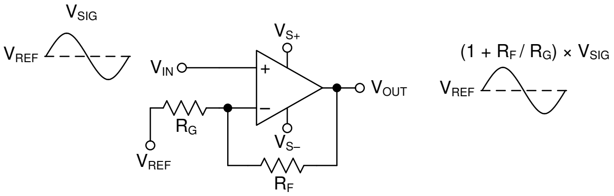


Figure 8-1. Noninverting Amplifier

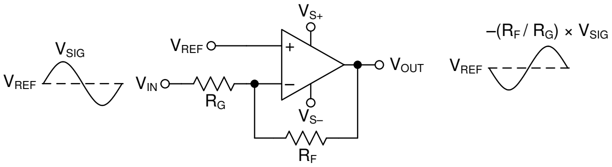


Figure 8-2. Inverting Amplifier

## 8.3 Feature Description

### 8.3.1 Input and ESD Protection

The OPA817 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the *Absolute Maximum Ratings*. As Figure 8-3 shows, all device pins are protected with internal ESD protection diodes to the power supplies.

The diodes provide moderate protection to input overdrive voltages beyond the supplies as well. The protection diodes can typically support a 10-mA continuous current. Where higher currents are possible (for example, in systems with ±12-V supply parts driving into the OPA817), current limiting series resistors should be added in series with the two inputs to limit the current. Keep these resistor values as low as possible because high values degrade both noise performance and frequency response. There are no back-to-back ESD diodes between $V_{IN+}$ and $V_{IN-}$. As a result, the differential input voltage between $V_{IN+}$ and $V_{IN-}$ is entirely absorbed by the $V_{GS}$ of the input JFET differential pair and must not exceed the voltage ratings shown in the *Absolute Maximum Ratings*.

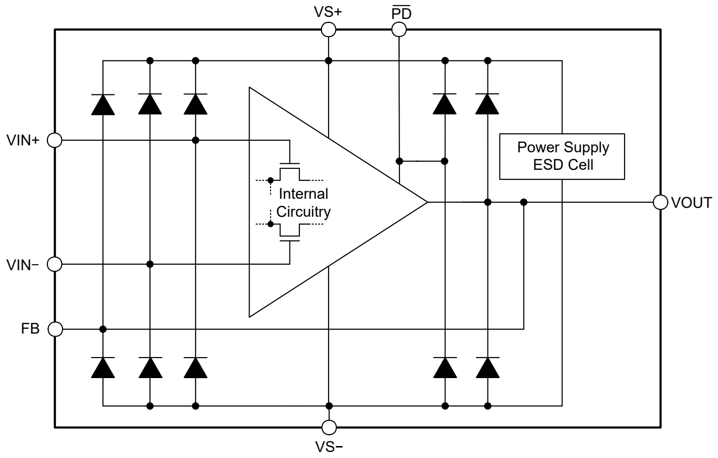


**Figure 8-3. Internal ESD Protection**

### 8.3.2 Feedback Pin

For high speed analog design, minimizing parasitic capacitances and inductances is critical to get the best performance from a high-speed amplifier such as the OPA817. Parasitic capacitance and inductance are especially detrimental in the feedback path and at the inverting input. They result in undesired poles and zeroes in the feedback that could result in reduced phase margin or instability. Techniques used to correct this phase margin reduction often result in reduced application bandwidth. To keep system engineers from making these tradeoff choices and to simplify the PCB layout, OPA817 features an FB pin on the same side as the inverting input pin (IN–). Figure 8-4 shows how this feature allows for a very short feedback resistor ($R_F$) connection between the FB and the IN– pin, which minimizes parasitic capacitance and inductance with minimal PCB design effort. Internally the FB pin is connected to OUT pin through metal routing on the silicon. Due to the fixed metal sizing of this connection, the FB pin has limited current carrying capability. Therefore, the specifications in the *Absolute Maximum Ratings* section must be adhered to for continuous operation. For applications requiring high accuracy, the metal routing resistance from OUT to FB can be considered and added to $R_F$ to set the desired gain. For more information, see Section 7.5.

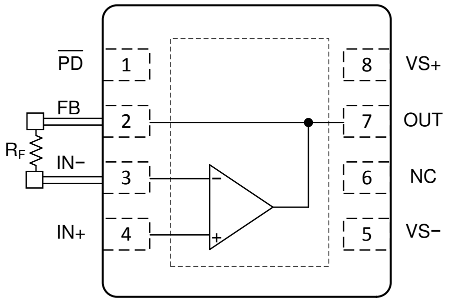
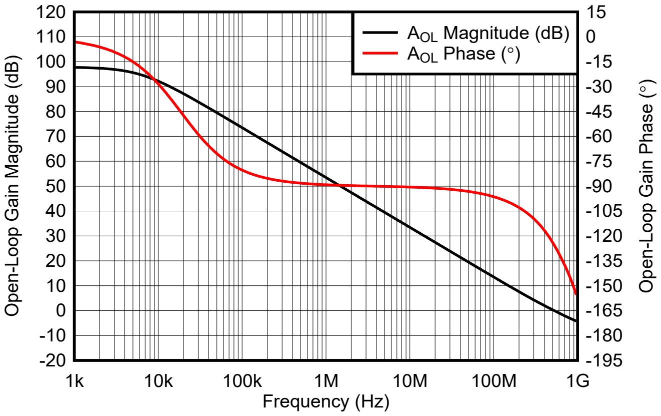


**Figure 8-4. $R_F$ Connection Between FB and IN– Pins**

### 8.3.3 FET-Input Architecture with Wide Gain-Bandwidth Product

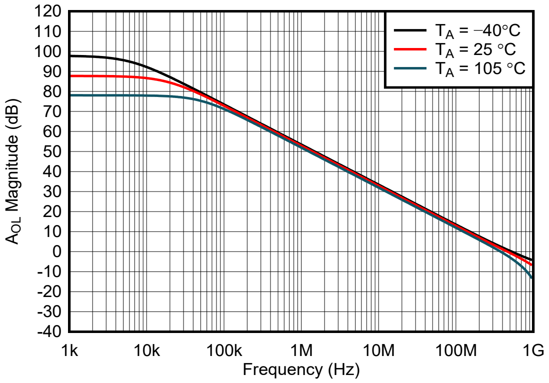
Figure 8-5 shows the open-loop gain and phase response of the OPA817. The GBWP of an op amp is measured in the 20 dB/decade constant slope region of the $A_{OL}$ magnitude plot. The open-loop gain of 60 dB for the OPA817 is along this 20 dB/decade slope and the corresponding frequency intercept is at 390 kHz. Converting 60 dB to linear units (1000 V/V) and multiplying it with the 390 kHz frequency intercept gives the GBWP of OPA817 as 390 MHz. As can be inferred from the $A_{OL}$ Bode plot, the second pole in the $A_{OL}$ response occurs after $A_{OL}$ magnitude drops below 0 dB (1 V/V). This results in phase change of less than 180° at 0 dB $A_{OL}$ indicating that the amplifier will be stable in a gain of 1 V/V. Amplifiers like OPA817 that are JFET-input, low noise and unity-gain stable can be used as high input impedance buffers and gain stages with minimal degradation in SNR. It has 800 MHz of SSBW in gain of 1V/V configuration with approximately 55° phase margin.

The low input offset voltage and offset voltage drift of OPA817 makes it a very suitable amplifier for high precision, high input impedance, wideband data acquisition system front-ends. As Figure 9-2 shows, the system benefits from the low noise JFET input stage with pico-amperes of input bias current to achieve higher precision at 1-MΩ input impedance settings and higher SNR at 50-Ω input impedance setting simultaneously in a typical data acquisition front-end circuit.



$R_L$ = 100 Ω Simulation

Figure 8-5. Open-Loop Gain Magnitude and Phase Vs Frequency



$R_L$ = 100 Ω Simulation

Figure 8-6. Open-Loop Gain Magnitude vs Temperature

### 8.3.4 Device Functional Modes

#### *8.3.4.1 Power-Down ($\overline{PD}$) Pin*

The OPA817 includes a power-down mode for low-power or standby operation and only consumes 55 µA (typical) of current when placed in power-down mode. Low-power systems that are only active for small periods of time benefit from this feature. The OPA817 can transition from low-power mode to active-mode in 300 ns (typical). For power-down pin control thresholds, refer to Section 7.5. An internal pull-up resistor of 2-MΩ provides a weak pull-up to $V_{S+}$ if $\overline{PD}$ is left unconnected. An external 1-nF capacitor to $V_{S+}$ may be used to avoid external noise coupling and false triggering. If the power-down mode is not used in an application, then connect the $\overline{PD}$ pin to $V_{S+}$.

# 9 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

### 9.1.1 Wideband, High-Input Impedance DAQ Front-End

The OPA817 features a unique combination of high GBWP, low-input voltage noise, and the DC precision of a trimmed JFET-input stage to provide a high input impedance for a voltage-feedback amplifier. Figure 9-2 shows how its very high GBWP of 390 MHz and high large signal bandwidth of 245 Mhz can be used to either deliver wide signal bandwidths at high gains or to extend the achievable bandwidth or gain in typical high-speed, high-input impedance data acquisition front-end applications. To achieve the full performance of the OPA817, careful attention to the printed circuit board (PCB) layout and component selection is required as discussed in the following sections of this data sheet. OPA817 also features a wider supply range thereby enabling a wider common-mode input range to support higher input signal swings.

Figure 9-1 shows the noninverting gain of +2 V/V circuit used as the basis for most of the *Typical Characteristics*. Most of the curves were characterized using signal sources with 50-Ω driving impedance, and with measurement equipment presenting a 50-Ω load impedance. As Figure 9-1 shows, the 49.9-Ω shunt resistor at the $V_{IN}$ terminal matches the source impedance of the test generator, while the 49.9-Ω series resistor at the $V_O$ terminal provides a matching resistor for the measurement equipment load. Generally, data sheet voltage swing specifications are at the output pin ($V_O$ in Figure 9-1) while output power specifications are at the matched 50-Ω load. As shown in Figure 9-1, the total 100-Ω load at the output combined with the 250-Ω total feedback network load presents the OPA817 with an effective output load of 83.3 Ω for the circuit.

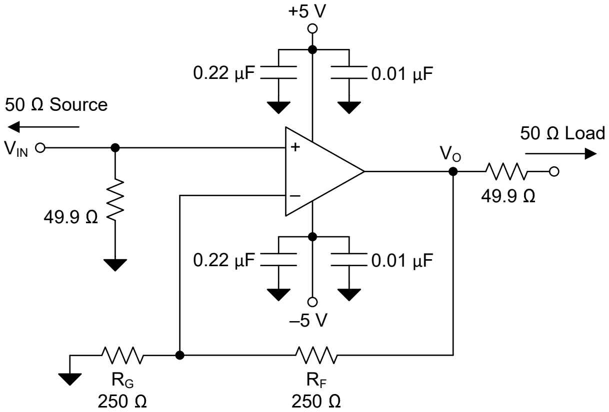


**Figure 9-1. Noninverting G = +2 V/V Configuration and Test Circuit**

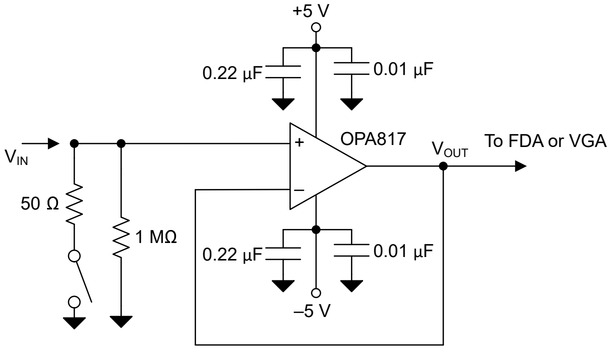


**Figure 9-2. High Input Impedance DAQ Front-End**

Voltage-feedback operational amplifiers, unlike current feedback amplifiers, can use a wide range of resistor values to set their gain. As Figure 9-1 shows, the parallel combination of $R_F$ || $R_G$ should always be kept to a lower value to retain a controlled frequency response for the noninverting voltage amplifier. In the noninverting configuration, the parallel combination of $R_F$ || $R_G$ will form a pole with the parasitic input capacitance at the inverting node of the OPA817 (including layout parasitic capacitance). For best performance, this pole should be at a frequency greater than the closed loop bandwidth for the OPA817.

### 9.1.2 Wideband, Transimpedance Design Using OPA817

The OPA817 design is optimized for wideband, low-noise transimpedance applications with high GBWP, low-input voltage, current noise, and low input capacitance. The high voltage capability allows greater flexibility of supply voltages along with wider output voltage swings. Figure 9-3 shows an example circuit of a typical photodiode amplifier circuit. As Figure 9-3 shows, the photodiode is generally reverse biased in a TIA application so that the photodiode current in the circuit of flows into the op amp feedback path. This results in an output voltage that reduces from $V_{REF}$ with increasing photodiode current. In this type of configuration and depending on the application needs, $V_{REF}$ can be biased closer to $V_{S+}$ to achieve the desired output swing. Consider the common-mode input range when $V_{REF}$ bias is used so that the common-mode input voltage stays within the valid range of the OPA817.

The key design elements that determine the closed-loop bandwidth, $f_{–3dB}$, of the circuit are as follows:

1. The op amp GBWP.
2. The transimpedance gain, $R_F$.
3. The total input capacitance, $C_{TOT}$, that includes photodiode capacitance, input capacitance of the amplifier (common-mode and differential capacitance), and PCB parasitic capacitance.

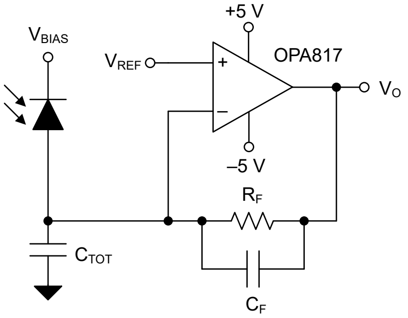


**Figure 9-3. Wideband, Low-Noise, Transimpedance Amplifier**

Equation 1 shows the relationship between the above mentioned three elements for a Butterworth response.

$$f_{-3dB} = \sqrt{\frac{GBWP}{2\pi R_F C_{TOT}}} \quad (1)$$

The feedback resistance ($R_F$) and the total input capacitance ($C_{TOT}$) form a zero in the noise gain and results in instability if left uncompensated. To counteract the effect of the zero, a pole is inserted in the noise gain by adding the feedback capacitor ($C_F$). The *Transimpedance Considerations for High-Speed Amplifiers* application report discusses theories and equations that show how to compensate a transimpedance amplifier for a particular gain and input capacitance. The bandwidth and compensation equations from the application report are available in a Microsoft Excel™ calculator. *What You Need To Know About Transimpedance Amplifiers – Part 1* provides a link to the calculator. As shown in Figure 9-3, the details of maximizing the dynamic range of TIA front-ends are provided in the *Maximizing the Dynamic Range of Analog TIA Front-End* application note.

ADVANCE INFORMATION

## 9.2 Typical Applications

### 9.2.1 High Bandwidth, 100-kΩ Gain Transimpedance Design

The high GBWP, low input voltage, and current noise of the OPA817 make it an excellent wideband transimpedance amplifier for moderate to high transimpedance gains.

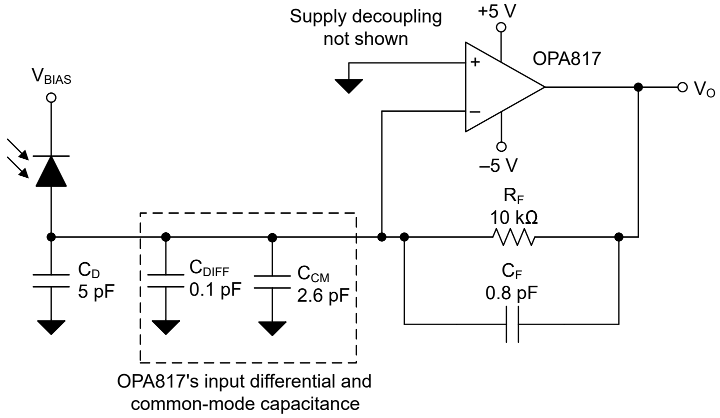


**Figure 9-4. Wideband, High-Sensitivity, Transimpedance Amplifier**

### 9.2.2 Design Requirements

Table 9-1 lists the design requirements for a high-bandwidth, high-transimpedance-gain amplifier.

**Table 9-1. Design Requirements**

| TARGET BANDWIDTH (MHz) | TRANSIMPEDANCE GAIN (kΩ) | PHOTODIODE CAPACITANCE (pF) |
|---|---|---|
| 28 | 10 | 5 |

### 9.2.3 Detailed Design Procedure

Designs that require high bandwidth from a large area detector with relatively high transimpedance gain benefit from the low-input voltage noise of the OPA817. This input voltage noise is peaked up over frequency by the diode source capacitance, and can, in many cases, become the limiting factor to input sensitivity. Figure 9-4 shows the transimpedance circuit with the parameters as defined in Table 9-1. With these three variables set (including the parasitic input capacitance for the OPA817 and the printed circuit board (PCB) added to $C_D$), the feedback capacitor value ($C_F$) can be set to control the frequency response. For a discussion about the theories and equations that show how to compensate a transimpedance amplifier for a particular transimpedance gain and input capacitance, see the Transimpedance Considerations for High-Speed Amplifiers application report. The bandwidth and compensation equations from the application report are available in a Microsoft Excel™ calculator. A link to the calculator is provided at What You Need To Know About Transimpedance Amplifiers – Part 1. Determine the total input capacitance ($C_{TOT}$) to help with the component selection. $C_{TOT}$ is referred to as $C_{IN}$ in the calculator. $C_{TOT}$ is the sum of $C_D$, $C_{DIFF}$, and $C_{CM}$, which is 7.7 pF. As listed in Table 9-2, using the value of $C_{TOT}$, the targeted closed-loop bandwidth ($f_{-3\ dB}$) of 28 MHz, and transimpedance gain of 10 kΩ requires an amplifier with approximately 380 MHz GBWP and a feedback capacitance ($C_F$) of 0.8 pF. With OPA817's 390 MHz GBWP, it will be a suitable amplifier for the design requirements.

**Table 9-2. Results of Inputting Design Parameters in the TIA Calculator**

| ***Calculator II*** | | |
|---|---|---|
| Closed-loop TIA Bandwidth ($f_{-3dB}$) | 28 | MHz |
| Feedback Resistance ($R_F$) | 10 | kΩ |
| Input Capacitance ($C_{IN}$) | 7.7 | pF |
| Op amp Gain Bandwidth Product (GBP) | 379.3 | MHz |
| Feedback Capacitance ($C_F$) | 0.793 | pF |

Figure 9-5 shows the simulated closed-loop bandwidth response of the circuit in Figure 9-4. The circuit was designed for $f_{-3\ dB}$ = 28 MHz and the simulated closed-loop 3-dB frequency is 26.5 MHz. Figure 9-6 shows the noise simulation of the TIA circuit. The output-referred voltage noise is shown on the Y-axis to the left, and the input-referred current noise (which is essentially output-referred voltage noise divided by the transimpedance gain of 10 kΩ) is shown on the secondary Y-axis to the right.

The flat-band output voltage noise is 13.5 nV/√Hz and is equivalent to 1.35 pA/√Hz of input-referred current noise. The noise in the relatively low frequency region, where the noise gain of the amplifier is 1 V/V, is dominated by the thermal noise of the 10 kΩ resistor (12.9 nV/√Hz at 27°C). At mid frequencies beyond the zero (formed by $R_F$ and $C_{TOT}$), the noise gain of the amplifier amplifies the voltage noise of the amplifier. The amplifier's noise starts to become the dominant noise contributor from this frequency onwards before the output noise starts to roll off at frequencies beyond the 3-dB closed-loop bandwidth. When considering integrated root-mean-square (RMS) noise, the mid-frequency noise will be a significant contributor; hence, using a 4.5 nV/√Hz low-noise amplifier like OPA817 is advantageous to minimize total RMS noise in the system.

### 9.2.4 Application Curves

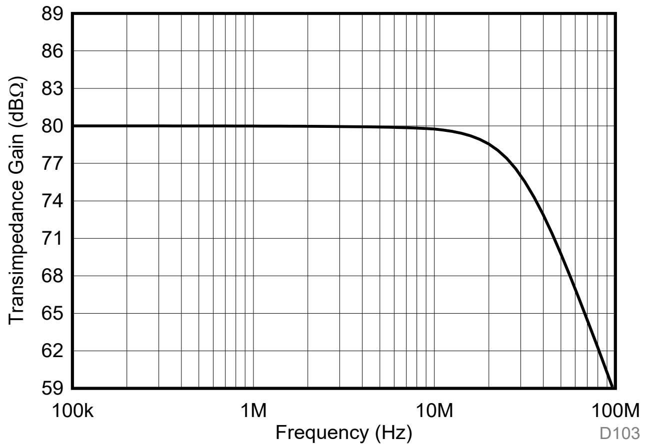


Figure 9-5. Closed-Loop Bandwidth of TIA

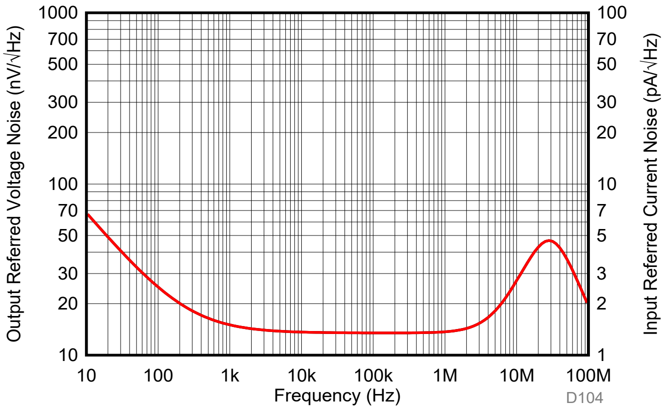


Figure 9-6. Noise Density vs Frequency of TIA

## 10 Power Supply Recommendations

The OPA817 is intended to operate on supplies ranging from 6 V to 12.6 V. OPA817 supports single-supply, split, balanced, and unbalanced bipolar supplies. When operating at supplies below 8 V, consideration must be given to the input common-mode range of the amplifier. Under these supply conditions, the common-mode must be biased appropriately for linear operation. Thus, the limit to lower supply voltage operation is the usable input voltage range for the JFET-input stage.

## 11 Layout

### 11.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier like the OPA817 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include the following:

1. **Minimize parasitic capacitance to any ac ground for all of the signal I/O pins.** Parasitic capacitance on the output and inverting input pins can cause instability. On the noninverting input, parasitic capacitance can react with the source impedance to cause unintentional bandlimiting. Ground and power metal planes act as one of the plates of a capacitor while the signal trace metal acts as the other separated by PCB dielectric. To reduce this unwanted capacitance, care must be taken to minimize the routing of the feedback network. A plane cutout around and underneath the inverting input pin on all ground and power planes is recommended. Otherwise, ground and power planes should be unbroken elsewhere on the board.

2. **Minimize the distance (less than 0.25-in) from the power-supply pins to high-frequency decoupling capacitors.** Use high quality, 100-pF to 0.1-µF, C0G and NPO-type decoupling capacitors with voltage ratings at least three times greater than the amplifiers maximum power supplies to ensure that there is a low-impedance path to the amplifiers power-supply pins across the amplifiers gain bandwidth specification. At the device pins, do not allow the ground and power plane layout to be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections must always be decoupled with these capacitors. Larger (2.2-µF to 6.8-µF) decoupling capacitors, effective at lower frequency, must be used on the supply pins. These are placed further from the device and are shared among several devices in the same area of the PC board.
3. **Careful selection and placement of external components will preserve the high frequency performance of the OPA817.** Use low-reactance resistors. Surface-mount resistors work best and allow a tighter overall layout. Never use wirewound type resistors in a high frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the inverting input and the output pin, respectively. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Even with a low parasitic capacitance at the noninverting input, high external resistor values can create significant time constants that can degrade performance. When OPA817 is configured as a conventional voltage amplifier, keep the resistor values as low as possible and consistent with the load driving considerations. Decreasing the resistor values keeps the resistor noise terms low and minimizes the effect of the parasitic capacitance. However, lower resistor values increase the dynamic power consumption because $R_F$ and $R_G$ become part of the output load network of the amplifier
4. **Heat dissipation is important for a high voltage device like OPA817**. For good thermal relief, the thermal pad should be connected to a heat spreading plane that is preferably on the same layer as OPA817 or connected by as many vias as possible, if the plane is on a different layer. It is recommended to have at least one heat spreading plane on the same layer as the OPA817 that makes a direct connection to the thermal pad with wide metal for good thermal conduction when operating at high ambient temperatures. If more than one heat spreading plane is available, then connect them by a number of vias to further improve the thermal conduction.

### 11.1.1 Thermal Considerations

The OPA817 will not require heatsinking or airflow in most applications. Maximum allowed junction temperature will set the maximum allowed internal power dissipation as described in the following paragraph. In no case should the maximum junction temperature be allowed to exceed 150°C.

Operating junction temperature ($T_J$) is given by $T_A + P_D \times R_{\theta JA}$. The total internal power dissipation ($P_D$) is the sum of quiescent power ($P_{DQ}$) and additional power dissipated in the output stage ($P_{DL}$) to deliver load power. Quiescent power is the specified no-load supply current times the total supply voltage across the part. $P_{DL}$ will depend on the required output signal and load, but for a grounded resistive load the $P_{DL}$ will be at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for balanced bipolar supplies). Under this condition $P_{DL} = V_S{}^2/(4 \times R_L)$ where $R_L$ includes feedback network loading.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

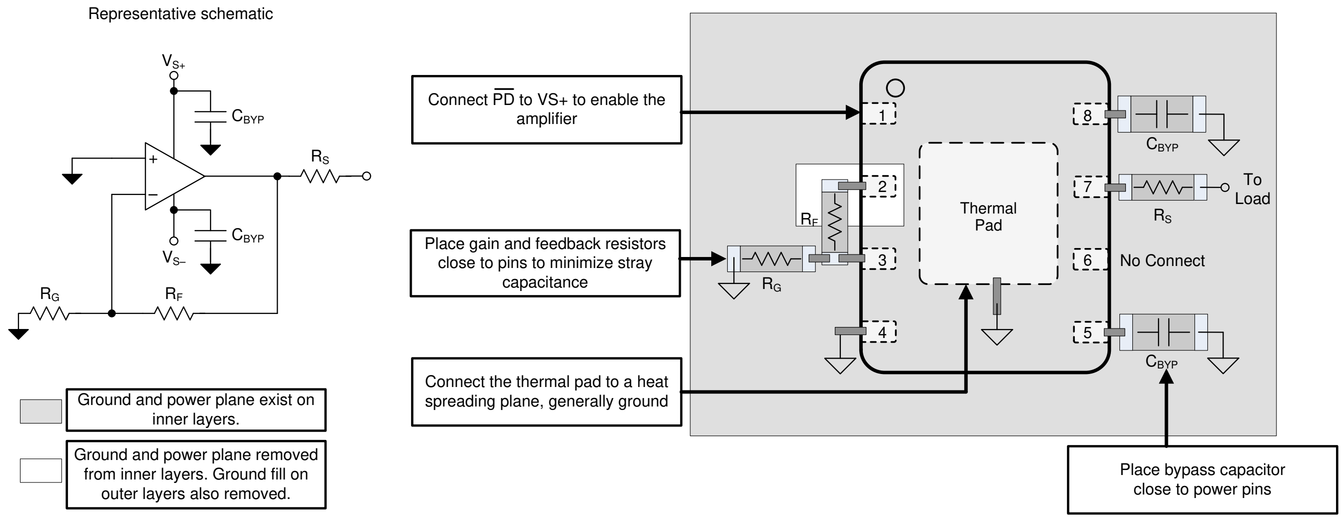
As a worst-case example, compute the maximum $T_J$ using OPA817 in the circuit of Figure 9-1 operating at the maximum specified ambient temperature of +105°C and driving a grounded 100-Ω load.

$P_D = 10\text{ V} \times 23.5\text{ mA} + 5^2 /(4 \times (100\ \Omega \parallel 500\ \Omega)) \cong 310\text{ mW}$

Maximum $T_J = 105°\text{C} + (0.310\text{ W} \times 64.9°\text{C/W}) = 125.1°\text{C}$.

All actual applications will be operating at lower internal power and junction temperature.

## 11.2 Layout Example



Connect $\overline{PD}$ to VS+ to enable the amplifier

Place gain and feedback resistors close to pins to minimize stray capacitance

Connect the thermal pad to a heat spreading plane, generally ground

Place bypass capacitor close to power pins

**Figure 11-1. Layout Recommendation**

# 12 Device and Documentation Support

## 12.1 Device Support

### 12.1.1 Development Support

- Texas Instruments, *Wide Bandwidth Optical Front-end Reference Design*

## 12.2 Documentation Support

### 12.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Transimpedance Considerations for High-Speed Amplifiers* application report
- Texas Instruments, *Maximizing the Dynamic Range of Analog TIA Front-End* techincal brief
- Texas Instruments, *What You Need To Know About Transimpedance Amplifiers – Part 1*
- Texas Instruments, *What You Need To Know About Transimpedance Amplifiers – Part 2*
- Texas Instruments, *Training Video: How to Design Transimpedance Amplifier Circuits*
- Texas Instruments, *Training Video: High-Speed Transimpedance Amplifier Design Flow*

## 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 12.5 Trademarks

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TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.7 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 13 Mechanical, Packaging, and Orderable Information

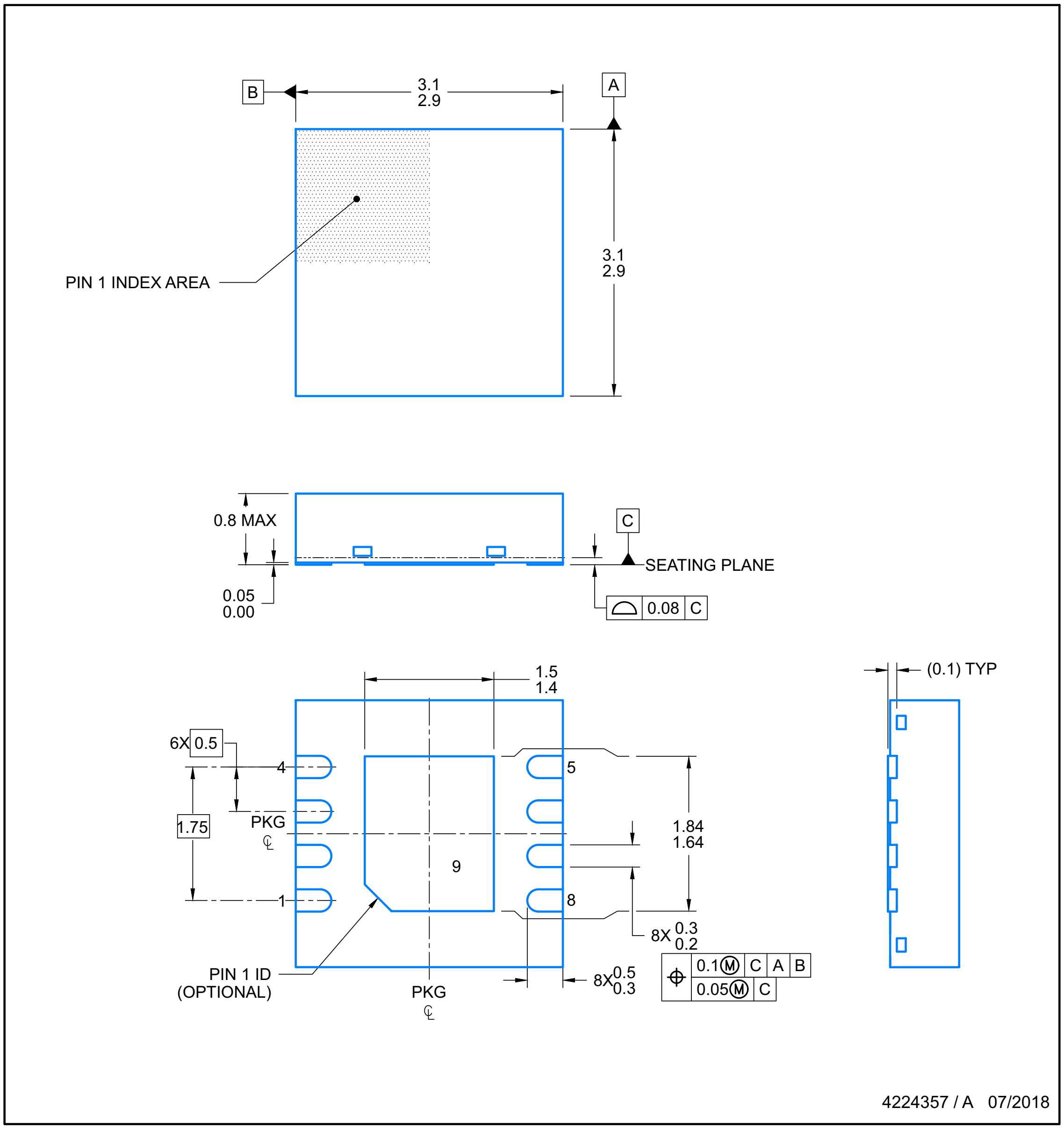
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

# PACKAGE OUTLINE

## DTK0008A

### WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

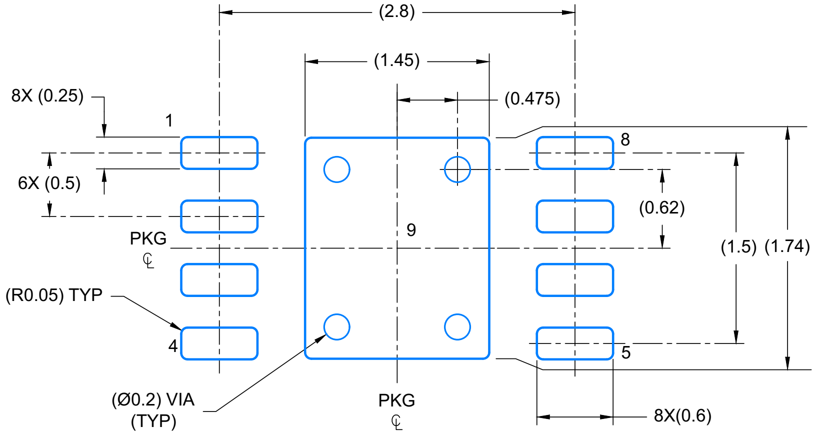
ADVANCE INFORMATION

# EXAMPLE BOARD LAYOUT

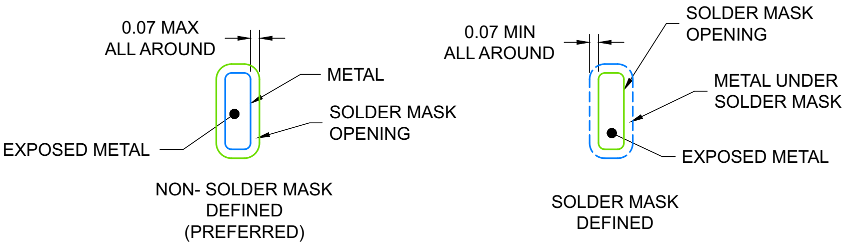
## DTK0008A

## WSON - 0.8 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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NOTES: (continued)

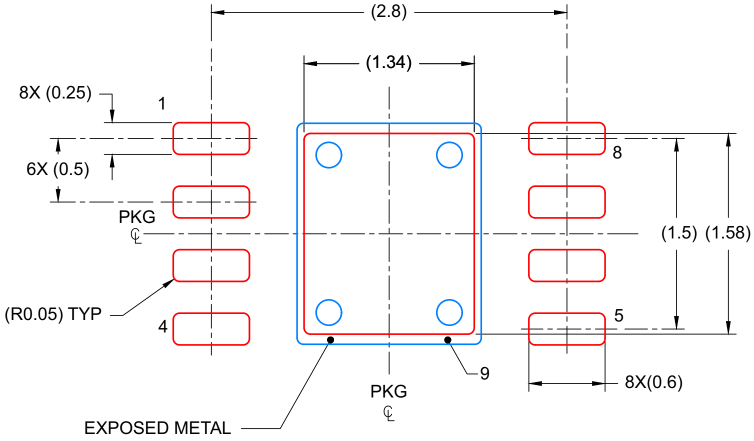
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

**DTK0008A**

**WSON - 0.8 mm max height**

PLASTIC QUAD FLATPACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 9: 84%
SCALE: 20X

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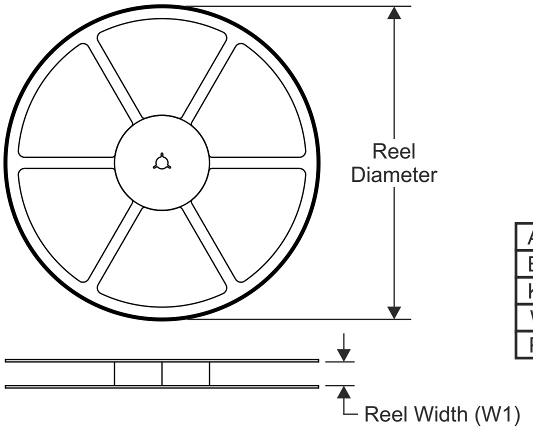
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

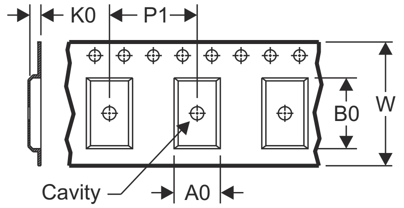
ADVANCE INFORMATION

## 13.1 Tape and Reel Information

**REEL DIMENSIONS**

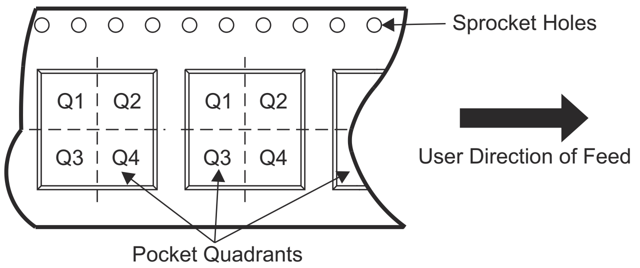


**TAPE DIMENSIONS**



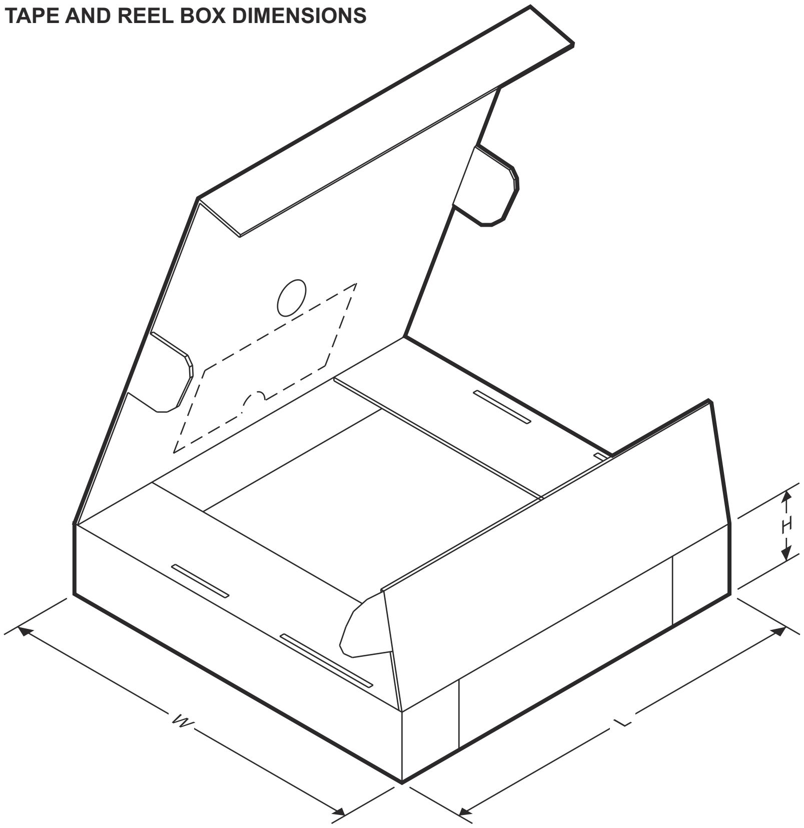
| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA817DTKR | WSON | DTK | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

**TAPE AND REEL BOX DIMENSIONS**



| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| OPA817DTKR | WSON | DTK | 8 | 3000 | 367.0 | 367.0 | 35.0 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| XOPA817DTKR | ACTIVE | WSON | DTK | 8 | 3000 | TBD | Call TI | Call TI | -40 to 105 |  | Samples |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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