Application Report
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RLC Filter Design for ADC Interface Applications

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ABSTRACT

As high performance Analog-to-Digital Converters (ADCs) continue to improve in their performance, the last stage interface from the final amplifier into the converter inputs becomes a critical element in the system design if the full converter dynamic range is desired. This application note describes the performance and design equations for a simple passive 2nd-order filter used successfully in ADC interface applications.

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1 Introduction

Last-stage interfaces to high-speed converters typically have included a simple RC filter as both a noise bandwidth limiting stage and a way to provide a path (through the capacitor) to absorb the sampling glitch coming out of the converter. This simple interface is proving increasingly inadequate as converter SNRs and input analog bandwidths continue to increase. A simple 2nd order RLC filter can provide both lower noise power bandwidth and more aggressive attenuation of the 3rd-order harmonic distortion at the high end of the analog input range.

2 Filter Topology and Options

Figure 1 shows the basic starting point for the single-ended input to single-ended output version of the filter to be analyzed. A second resistor is included to ground (R_2) over what would normally be considered a standard filter. This resistor provides considerably more design options in the total interface design and will be included in the analysis for this added flexibility. The algebra will easily give results if $R_2 \rightarrow \infty$, so it will certainly be an option to eliminate this resistor later using the more complete development initially.

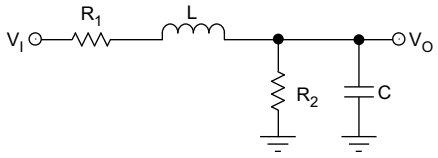

Figure 1. Proposed RLC Passive Filter

In the application where V_I is the output of an op amp and V_O is the input of an ADC, R_2 can provide DC biasing current to the output stage of the amplifier if a DC operating voltage out of the amplifier is required to match the common-mode input voltage of the ADC. This DC current can often improve harmonic distortion by turning what is normally a Class AB output stage in the amplifier to a Class A stage. If the final design requires a DC blocking cap to be inserted at R_1, then R_2 becomes the DC biasing resistor at the input of the ADC. For the circuit of Figure 1, R_2 does cost a DC and AC attenuation in the signal from V_I to V_O – it is intended that the designs using an R_2 will pick values for R_1 and R_2 where this attenuation is < 10%. For the DC level at V_I, R_2 will also drop this down slightly. This can be recovered by adjusting the V_I DC level up accordingly; or, in the case of differential input ADCs where Figure 1 will become a differential filter, R_2 can become the resistor between the legs with no ground connection. This will still give the same filter response for the differential output, but no attenuation for the common-mode DC operating voltage. These options will be explored in more detail, after the filter design discussion.

Equation 1 gives the general Laplace transfer function for the circuit of Figure 1.

$$\frac{V_O}{V_I} = \frac{\frac{1}{LC}}{S^2 + S\left[\frac{1}{R_2C} + \frac{R_1}{L}\right] + \left(1 + \frac{R_1}{R_2}\right)\frac{1}{LC}} \tag{1}$$

If the DC attenuation introduced by R_2 is defined as:

$\alpha = R_2 / (R_1 + R_2)$

and the total DC impedance seen by V_I as:

$R_T = R_1 + R_2$

then, Equation 1 becomes Equation 2.

$$\frac{V_O}{V_I} = \frac{\frac{1}{LC}}{S^2 + S\left[\frac{1}{\alpha R_T C} + \frac{R_T(1-\alpha)}{L}\right] + \left(\frac{1}{\alpha LC}\right)} \tag{2}$$

From Equation 2, the key elements for a 2nd-order filter can be written as shown in Equation 3 and Equation 4.

$$W_O = \sqrt{\frac{1}{\alpha LC}} \tag{3}$$

$$Q = \frac{\sqrt{\frac{1}{\alpha LC}}}{\frac{1}{\alpha R_T C} + \frac{R_T(1-\alpha)}{L}} \tag{4}$$

The W_O and Q completely describe the frequency response for a 2nd-order filter. The intent here is to simply pick an R_T (in order to set a DC standing current out of V_I assuming it is sitting at the required DC bias point for the converter) and α as an acceptable attenuation to take in the signal gain. With those two resistive parts of the design simply selected, Equation 3 and Equation 4 may be solved for the required L and C, given a target W_O and Q.

After some manipulation, Equation 3 and Equation 4 may be used to find the required L, as shown in Equation 5 and Equation 6, while Equation 7 gives the required C once L is determined. Both Equation 5 and Equation 6 are valid solutions for L. Using the higher value for L given by Equation 5 will lead to a lower required C value, while using Equation 6 will lead to a higher C value. Some converters have an input parasitic C that will require Equation 6 to be used to allow a physical implementation.

$$L = \frac{R_T}{2W_O Q}\left[1 + \sqrt{1-(1-\alpha)(2Q)^2}\right] \tag{5}$$

$$L = \frac{R_T}{2W_O Q}\left[1 - \sqrt{1-(1-\alpha)(2Q)^2}\right] \tag{6}$$

Solve Equation 3 for C to get Equation 7, and then substitute the results of either Equation 5 or Equation 6 to get the required C:

$$C = \frac{1}{\alpha L\left(W_O{}^2\right)} \tag{7}$$

A couple of limits to this analysis can be drawn from Equation 5. Specifically, as $\alpha \rightarrow 1$ (meaning $R_2 \rightarrow \infty$), only Equation 5 provides a solution while Equation 6 goes to zero. This shows that the lower L, higher C solution of Equation 6 is created by including R_2 as an added design option. Also, the solution for L can go imaginary for certain combinations of α and Q. It is most useful to pick an α, then solve for the maximum Q allowed, before the terms under the radical in Equation 5 and Equation 6 go negative. Equation 8 shows this constraint on the design.

$$Q < \frac{1}{2}\sqrt{\frac{1}{1-\alpha}} \tag{8}$$

With α typically > 0.9, this does not put much constraint on Q, since we are normally not looking for a peaked response at the output of the filter. For example, at α = 0.9, Q must be < 1.58 in order to get a solution for L in Equation 5 or Equation 6. A design targeting a Q of 1.58 would be getting a frequency response peaking of 4.4dB (see Equation 25). A more typical selection for Q is 0.707, where a maximally flat Butterworth filter shape results. When Q = 0.707, Equation 5 reduces to Equation 9.

$$L = \frac{R_T}{2W_O Q}\left(1 + \sqrt{2\alpha - 1}\right) \tag{9}$$

Again, when $\alpha \rightarrow 1$ (meaning $R_2 \rightarrow \infty$), the more typical design equation for L in Equation 10 is used, where R_T is now only R_1 and Q = 0.707 is assumed.

$$L = \frac{R_T}{W_O Q} \tag{10}$$

3 Design Example

Consider a typical filter design target and apply the design equations developed here to implement a 2nd-order passive RLC filter, using the circuit of Figure 1.

3.1 Conditions and Targets

Assume V_I has a 2.5 V DC component to match up to the converter midrange.

A 5 mA DC bias current out of V_I is acceptable and has been shown to improve distortion for the amplifier driving V_I. This will set R_T = 500 Ω. Allow a 0.915dB attenuation in the signal, which will require α = 0.9.

Exceptional flatness through 10 MHz is desired with a –3dB cutoff at 18 MHz. Since there are added poles in the system, a 0.5dB rolloff at 9 MHz needs to be compensated by the filter. This 0.5dB peaking can be shown (see Equation 27) to require a Q = 0.864. Then, the F_O to hit an 18 MHz F_{-3dB} can be shown (see Equation 26) to be:

$$W_O = (2\pi) * \frac{18\,MHz}{1.176} = (2\pi) * 15.31\,MHz = 2\pi F_O \tag{11}$$

Using Equation 5 (and always remembering to adjust the F_O = 15.3 MHz to radians with a 2π multiplier) gives an L shown in Equation 12.

$$L = \frac{500\ \Omega}{2(2\pi)15.31\,MHz\,(0.864)}\left[1+\sqrt{1-(1-0.9)\left(2(0.864)\right)^2}\right] = 5.5\ \mu H \tag{12}$$

With L resolved, C is provided in Equation 13.

$$C = \frac{1}{0.9(5.5\ \mu H)(2\pi 15.31\,MHz)^2} = 21.7\ pF \tag{13}$$

Looking at the alternative (low L) solution created by having an R_2 in place, and putting values into Equation 6, gives Equation 14:

$$L = \frac{500\ \Omega}{2(2\pi)15.31\,MHz\,(0.864)}\left[1-\sqrt{1-(1-0.9)\left(2(0.864)\right)^2}\right] = 0.49\ \mu H \tag{14}$$

Then, using this alternative value for L in Equation 7, provides Equation 15.

$$C = \frac{1}{0.9(0.49\ \mu H)(2\pi 15.31\,MHz)^2} = 245\ pF \tag{15}$$

Continuing with the design,

$$R_2 = 0.9 * 500\ \Omega = 450\ \Omega \text{ and } R_1 = R_T - R_2 = 500\ \Omega - 450\ \Omega = 50\ \Omega \tag{16}$$

Figure 2 shows the final design with values (Equation 12 and Equation 13 results), while Figure 3 shows the simulated frequency response that results for either combination of L and C.

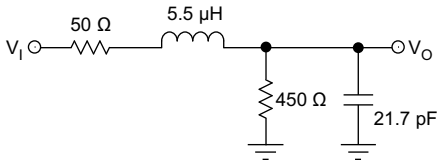

Figure 2. Design Example for 18 MHz Cutoff With 0.5dB Peaking Using Low C Design

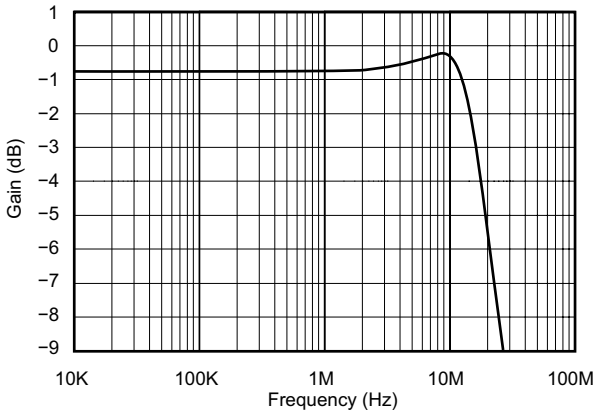

Figure 3. Simulated Filter Performance

This filter response shows the expected 0.9dB loss at low frequencies, a 0.5dB peaking at 9 MHz, and a –3dB frequency at 18 MHz. Aside from providing a noise power bandwidth limit for the noise spectrum at V_I, this filter gives some attenuation for harmonic distortion at the higher end of the desired input frequency range. For instance, if the maximum analog frequency ranges up to 10 MHz, as the input frequency extends above 6 MHz, significant attenuation of the 3rdharmonic will be provided. At 6 MHz input, the 3rd falls at 18 MHz and will see 3dB attenuation from the harmonic power present at V_I. As this input frequency moves up to 10 MHz, this 2ndorder filter provides 12.4dB attenuation for the 3rd-harmonic falling at 30 MHz. This attenuation of harmonics is less effective for 2nd-harmonic terms and of no impact for 3rd-order intermodulation terms where the two carriers are closely spaced. This 2nd-order distortion issue is most easily handled by going differential with both the amplifier and filter circuit.

4 Input Impedance Considerations

The example filter of Figure 2 will become the load to the amplifier driving V_I. If the impedance over frequency looking into this filter becomes very low, it can unnecessarily load that amplifier, thus, degrading the distortion performance. Figure 4 shows the simulated input using either combination of L and C.

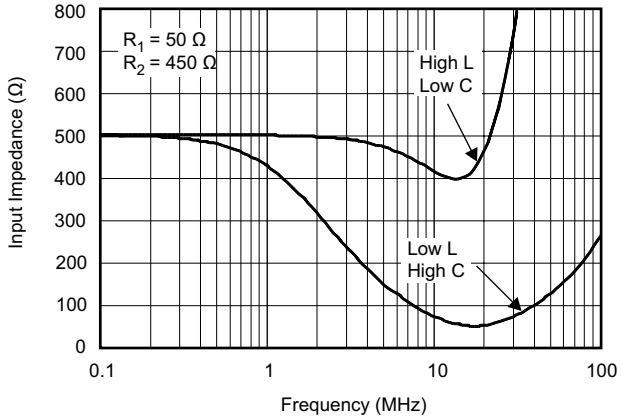

Figure 4. Simulated Input Impedance of the RLC Filter

As expected, the low frequency input impedance is the R_T selected for the design (500 Ω) while the high-frequency behavior is quite different between the two solutions. The low L, high C solution (of Equation 14 and Equation 15) shows a very low impedance as the frequency increases. The < 100 Ω load impedance at 10 MHz can significantly degrade the achievable distortion performance for the amplifier driving V_I.

To maintain a reasonably high load impedance for this filter design option, it is recommended that R_1 be increased to a minimum value of 200 Ω when the low L/high C design option is used. This will set a floor to the load impedance even as the LC portion of the circuit goes to very low impedance. It will, however, restrict the available Class A biasing current in R_1 and R_2, unless higher signal attenuations are allowed. It is preferable to provide the Class A current as an added resistor to ground at V_I (having no impact on the filter shape) than to take higher signal attenuations.

Shifting the R values up, and setting R_1 = 200 Ω while retaining α = 0.9 (giving R_2 = 1800 Ω and R_T = 2000 Ω) will adjust the L value up and the C value down through Equation 14 and Equation 15, and give the filter design of Figure 5.

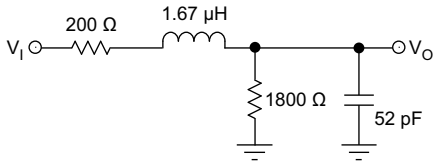

Figure 5. Higher Input Impedance Filter

This implementation will give the same frequency response as shown in Figure 3. It will also hold a much higher minimum input impedance over that shown in Figure 4. A comparison of input impedance for the two filter options of Figure 2 and Figure 5 is shown in Figure 6. This higher C design option is particularly useful, since the desired cutoff frequencies increase to where the required C value for the low C option drops below the expected input parasitic of the converter.

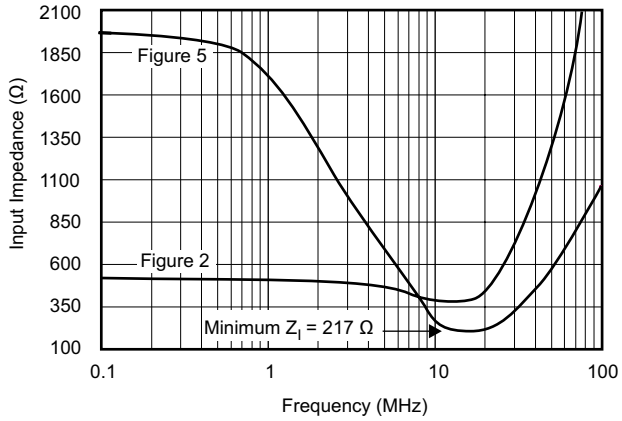

Figure 6. Input Impedance Comparison of Figure 2 and Figure 5

5 Converting the Design to a Differential Filter and R_2 Options Most

Most emerging high performance ADCs offer a differential input in order to get improved SFDR through even-order harmonic suppression. To convert the example filter design of Figure 2 to a differential filter, first consider Figure 7, where each element is simply duplicated.

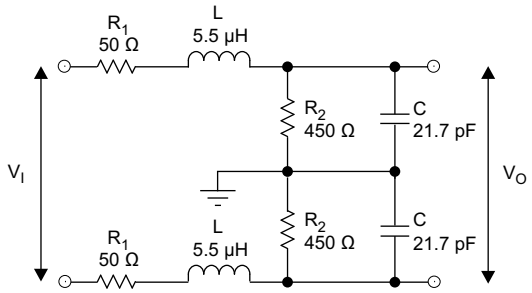

Figure 7. Simple Differential Version of 2nd-Order Filter

One important difference in understanding the operation of Figure 7 is to consider both the common-mode and differential-mode characteristics. For the differential signals, which matter most to the ADC input, this circuit is exactly the same as Figure 2 in that the midpoint ground for R_2 and C is transparent to the differential signal. The common-mode part of V_I still sees the DC load provided by R_2 and will also have the same frequency response as the differential input signal.

Assuming for a moment that the DC biasing is desirable, but the common-mode filtering is not needed, Figure 8 provides a simpler version by combining the two capacitors in series into one capacitor.

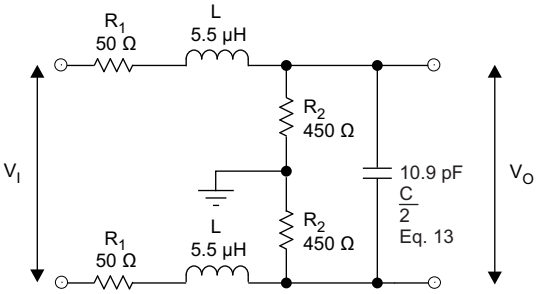

Figure 8. Simplified Differential Filter

The input common-mode signal still sees a common-mode load through R_2, but now receives no filtering effect due to C. The purely differential capacitor now acts only to filter the differential signal and is transparent to any common-mode AC signal. This is normally acceptable since there should be very little AC common-mode signal present into V_I and, more importantly, most modern differential input ADCs reject common-mode over frequency extremely well.

The capacitor value of Figure 8 may be on the order of the input parasitic capacitance of the converter. In fact, in some cases, this capacitor may be implemented only by that input parasitic, and eliminated as an external component. In other applications, the ADC input capacitance may exceed that required by the circuit of Figure 8. In that case, the alternate solution for L and C should be used to reduce the L but increase the C to the point where an implementation including the effect of the ADC input capacitance is possible.

Figure 9 shows the example filter design where no DC bias current is drawn, but R_2 must be included to get this second solution for L and C in order to raise the required C above the ADC parasitic input capacitance. This is also scaling R_1 and R_2 up to the design of Figure 8.

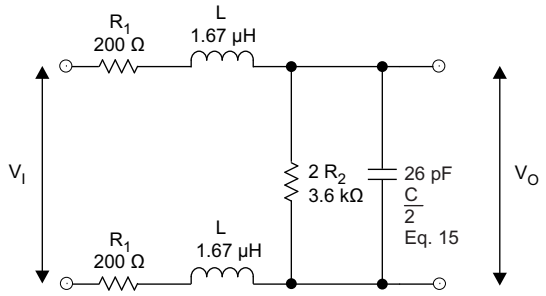

Figure 9. Alternate LC Values With No Common-Mode Load

Here, the R_2 resistors are also combined from the single-ended analysis to give a purely differential load. The capacitor is shown in Equation 15, cut in half to make the series combination from the topology of Figure 7 equivalent to Figure 9. This circuit has no DC or AC common-mode load. It does provide the same filter characteristic of Figure 7 for the differential signal at V_I. Since there is no common-mode load, there is no attenuation for any common-mode signal present at V_I and no DC biasing current from V_I.

There are some added interesting alternative uses for R_2 in this design. If, for instance, the amplifiers that are used cannot swing as far positively as the ADC input range requires, R_2 may be connected to the positive supply to provide a resistive level shift positively.

For example: Assume a 2VPP input ADC operating on +5 V supply where a 2.5 V common-mode is nominal, but ±0.5V shift from this level is acceptable. Assume the amplifier loses distortion performance as it swings closer to its supply voltage and assume it is a ±5 V device. Each input of the ADC must see a VCM within the 2 → 3 V range, with ±0.5 V swing around this to provide a full-scale input. Design the amplifier to sit at 1.5 V DC output with a level shift to 2 V DC through the resistor network to the ±5 V supply.

Setting R_1 = 200 Ω, only 2.5 mA of sinking current is required to level-shift 0.5 V. If the total current from a 1.5 V amplifier output to +5 V supply is 2.5 mA, then the total $R_1 + R_2$ needs to be 1400 Ω, making R_2 = 1200 Ω and α = (1200/1400) = 0.857. To get the full ±0.5V at the output of this attenuator, the amplifier will need a ±0.5 / (0.857) = ±0.583 V swing. Sitting at 1.5 VDC, this then requires a 0.917 V to 2.08 V output swing from the amplifier. This output swing, and Class A bias into the output pin, would also work well with a single +5 V supply amplifier having a rail-to-rail output swing.

With R_T = 1400 Ω and α = 0.857, continue the design with a targeted filter characteristic of a maximally flat Butterworth (Q = 0.707) and F_{-3dB} = 28 MHz. Use the second design option for L and C to solve for a higher C value, then collapse into a differential single C design. Using Equation 9, solve for L as Equation 17, where a (−) sign is substituted prior to the radical.

$$L = \frac{1400\ \Omega}{2(2\pi)28\ MHz(0.707)}\left(1-\sqrt{2(0.857)-1}\right) = 873\ nH \quad (17)$$

$$C = \frac{1}{0.857\,(873\ nH)(2\pi 28\ MHz)^2} = 43\ pF \tag{18}$$

Figure 10 shows the completed design, where a typical amplifier and ADC are included. The amplifier is providing a differential signal gain of 3 where an AC-coupled signal path through an inverting topology allows the common-mode output to be set directly as a 1.5 V DC bias on the non-inverting inputs.

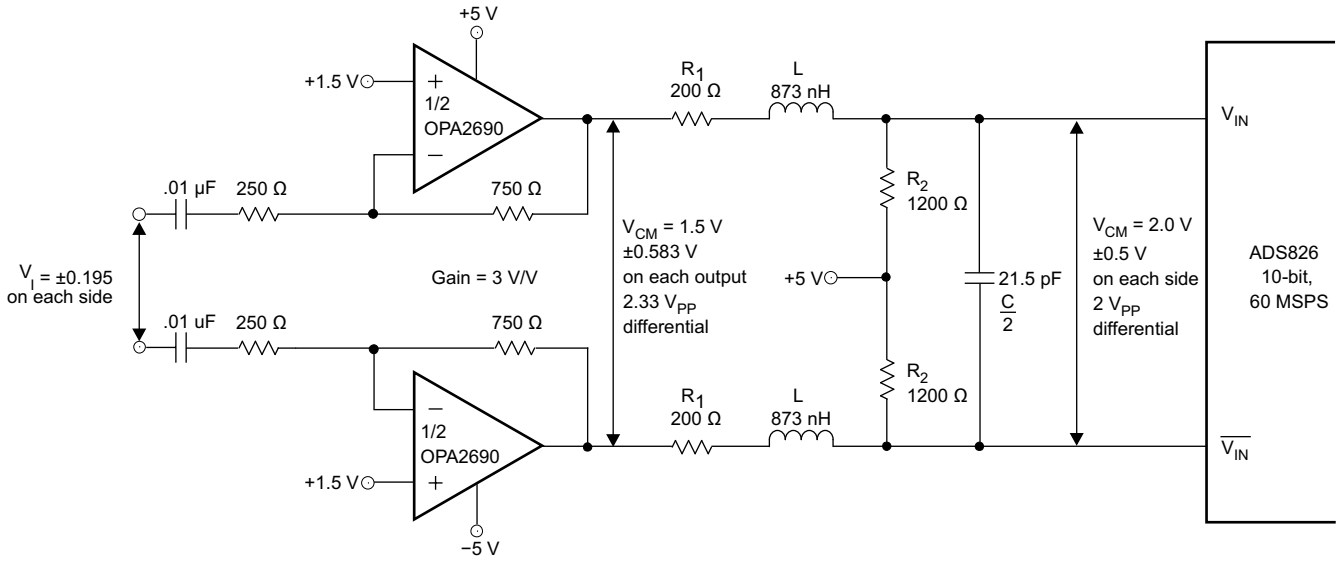

Figure 10. RLC Filter With Common-Mode Level Shifting

Another good use for R_2 is where a DC blocking cap is used in series with R_1 and the ADC common-mode voltage is brought in through R_2. In this design, R_2 is normally much higher than R_1, giving an $\alpha \rightarrow 1$. Equation 19 gives the approximate transfer function of the high-pass part of this filter (ignoring the LC for the low-pass design) using the analysis circuit of Figure 11.

$$\frac{V_O}{V_I} = \left[\frac{R_2}{R_1 + R_2}\right] * \frac{s}{s + \dfrac{1}{C_H(R_1 + R_2)}} = \alpha \frac{s}{s + \dfrac{1}{C_H R_T}} \tag{19}$$

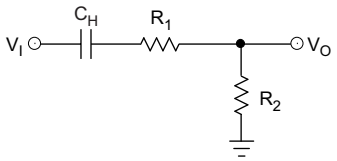

Figure 11. High-Pass Analysis Circuit As

As an example, target a design that places the high-pass pole at 16 kHz, with R_T = 300 Ω and α = 0.98. Place the 2nd-order low-pass at 16 MHz again, using a Butterworth response.

CH = 0.033 µF

R_2 = 294 Ω

R_1 = 6 Ω

Using the first solution for L (see Equation 5):

L = 4.2 µH

and

C = 24.2 pF

The total design is shown in Figure 12.

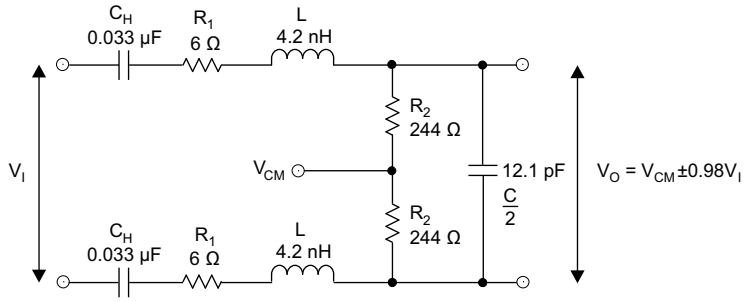

Figure 12. LC Filter With High-Pass and Common-Mode Reference

This circuit is very similar to Figure 8, with the addition of blocking capacitors and a common mode reference in place of ground at the midpoint of the R_2 resistors. Figure 13 shows the simulated small signal frequency response for Figure 12.

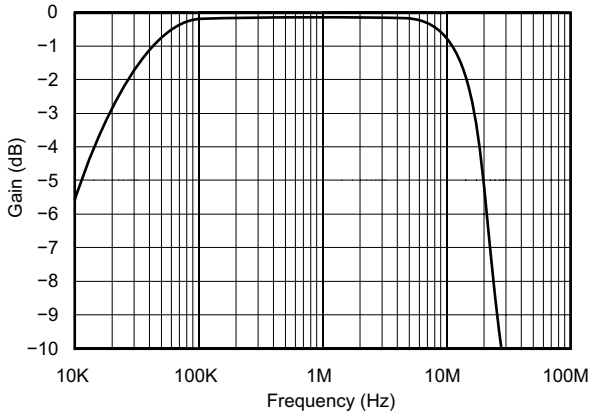

Figure 13. Simulated Frequency Response for the Circuit of Figure 12

6 Using 2nd-Order Transfer Functions to Infer Actual W_O and Q

The filter designs presented here provide an easy means to control noise power bandwidth and attenuate distortion when the harmonics fall beyond the cutoff frequency. It is not unusual that the actual filter characteristic deviates from the ideal analysis in implementation. Several sources can explain this deviation from ideal.

- Amplifier bandwidth rolling off in the passband region for the filter. If we assume the single-ended or differential V_I is coming from a prior amplifier stage, any slight rolloff prior to the filter cutoff frequency will appear as a lower f_{-3dB} than expected.
- Self-resonance in the inductors. The self-resonant frequency for the inductor needs to be far higher than the anticipated cutoff frequency to maintain the desired filter shape. It is for this reason that the lower inductor design point will often be the preferred design – if the higher capacitor value is acceptable to the converter's operation.
- Converter input capacitance adding in parallel with the filter C. Often, this may be an estimate in the device-specific ADC data sheet. Modern pipeline differential input converters do show an input capacitance that appears to be independent of both clock frequency and input voltage. Some earlier converters, and certain architectures, show an input capacitance dependent on either the clock frequency or the input signal voltages.

Bench testing for the filters shown here suggested an easy means to extract the ADC input capacitance from the measured filter response. If we apply amplifiers that are flat through the intended passband, and inductors that go self-resonant far beyond the desired cutoff frequency, any deviation in measured filter shape must be arising from the parasitic capacitance of either the converteror the probe capacitance used to measure the voltage at the filter output. The starting point for this extraction is to work backwards from the measured frequency response to what the W_O and Q must have been to get that frequency response. To do this, a short review of 2nd-order low pass filters is helpful.

The basic transfer function for a 2nd-order low-pass filter is shown in Equation 20.

$$\frac{V_O}{V_I} = \left[\frac{A W_O^2}{s^2 + s\frac{W_O}{Q} + W_O^2} \right] \tag{20}$$

The characteristic frequency (W_O) is the radial distance in the s-plane from the origin to the poles when they are complex-conjugate pairs. The units in Equation 20 are normally in radian frequency. This can be converted to hertz (Hz) by dividing W_O by 2π. The Q in this formulation indicates how complex the poles are.

The angle that the vector makes with the negative-real axis in the s-plane from the origin to the complex poles is given by $\cos^{-1}\left(\frac{1}{2Q}\right)$. Some key values for Q and the resulting pole locations are:

- When Q < 0.5, both poles are real
- When Q = 0.5, two repeated poles occur at – W_O
- When Q = 0.577, the resulting frequency response is a 2nd-order Bessel with the best phase linearity
- When Q = 0.707, the resulting frequency response is a 2nd-order Butterworth with the best gain flatness.

At Q = 0.707, the poles are at ±45° to the negative real axis in the s-plane.

Most of the filters chosen for frequency-domain-oriented ADC applications are at least Butterworth, or with slightly higher Q. As the Q exceeds 0.707, the frequency response starts to peak up, extending the –3dB bandwidth but increasing the integrated noise coming through the filters. Often, filters designed for a Q = 0.707 show a slight peaking in the measured response. This peaking is due to the added parasitic C in parallel with the desired filter C, increasing the Q for the physical filter. Going back to Equation 4, and with some manipulation to isolate on C, provides Equation 21 with where the filter Q is given:

$$Q = \left(R_T \sqrt{\frac{\alpha}{L}} \right) \frac{\sqrt{C}}{1 + C\frac{\alpha(1-\alpha)R_T^2}{L}} \tag{21}$$

This still rather involved expression for Q does not clearly show if the dependence on C is positive or negative. Taking the derivative of Q vs. C in Equation 21, and manipulating to solve for a positive derivative, gives the constraint of Equation 22. If this expression evaluates to be < 1, then the Q for the RLC filters discussed here will increase if C is higher than expected due to parasitics and ADC input capacitance.

$$\frac{(1-\alpha)R_T^2}{L^2 W_O^2} < 1 \tag{22}$$

Substituting into Equation 22 for L (using Equation 5 and Equation 6) gives the following condition for an increasing Q, for increasing C:

$$\frac{(1-\alpha)(2Q)^2}{\left(1 \pm \sqrt{1-(1-\alpha)\left(2Q^2\right)}\right)^2} < 1 \tag{23}$$

Recognizing that the same expression appears in both the numerator and the radical, this can be rewritten as a variable X = (1 - α) * (2Q)2, giving Equation 24:

$$\frac{X}{\left(1 \pm \sqrt{(1-X)}\right)^2} < 1 \tag{24}$$

X must be less than 1 in order to get a solution for L in Equation 5 and Equation 6. Solving Equation 24 for where the expression evaluates to equal 1 shows that this only occurs at X = 1 for either the positive or negative term in the denominator. Using the positive solution in the denominator (high L, Equation 5) always gives a solution < 1 in Equation 24. This indicates that a filter implemented using Equation 5 will always have an increasing Q, if C is increased from the design value. This solution is preferred in order to extract the converter parasitic C when an increased peaking is used to extract the actual W_O and Q. Interestingly, using the Equation 6 solution, and adding additional parasitic C in the implementation, will always reduce the Q. The converter parasitic C could also be extracted using this approach, but a more direct method is to identify the peak frequency and amount of peaking, rather than extracting W_O and Q for a more rolled off response.

Given a measured frequency response for the implementation of one of these RLC filters, it is possible to estimate the W_O and Q that would agree with the frequency response shape. A thorough approach would do a least-squares-error fit to the data vs. Equation 20 that would provide the best match over frequency to the actual data, finding the W_O and Q that minimizes the error.

A simpler approach is to measure a couple of key data points on the response, then use these two data points to solve for the two unknowns – W_O and Q. If the response is peaking, indicating that Q > 0.707, one easy approach is to measure the amount of peaking in the gain and then the –3dB bandwidth. This is the preferred approach and most applicable to the high L solution of Equation 5. Equation 25 gives the relationship on that peaking to Q, and Equation 26 gives the relationship between W_O and F_{-3dB} given a Q.

$$Peaking\ (dB) = 20 \log \frac{Q}{\sqrt{1 - \frac{1}{4Q^2}}} \tag{25}$$

$$F_{-3dB} = \frac{W_O}{2\pi} \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}} \tag{26}$$

This approach is simplified because the peaking only depends on the Q. Solving Equation 25 for Q, given the peaking as a ratio (β) of peak gain to the targeted gain (α in the filters discussed here), gives Equation 27.

$$Q = \frac{\beta}{\sqrt{2}} \sqrt{1 + \sqrt{1 - \frac{1}{\beta^2}}} \tag{27}$$

Evaluating this expression for β = 1 gives Q = 0.707, as expected. If there is no peaking, we should have the maximally flat Butterworth response that results from Q = 0.707.

With Q estimated from the peaking, putting that value into Equation 26 allows a quick solution for W_O, given the measured F_{-3dB}.

7 Using W_o and Q to Estimate Actual L and C

The final step in the filter implementation discussion is to work backwards from the estimated W_O and Q to resolve what L and C must have been to give that measured result. It is assumed here that R_1 and R_2 are known with some certainty. This gives the R_T and α necessary for this analysis.

Going back to Equation 5 and Equation 7, direct substitution of W_O and Q will give L (using Equation 5 or Equation 6) then going to Equation 7 will give the C value that would explain the measured frequency response. If the filter was implemented with a large L value, using Equation 5 will give an estimate of the actual value in the circuit; then, going on to Equation 7 will estimate the total C actually present in the circuit.

Similarly, if the small L value and a large C were used, then Equation 6 will estimate the L and Equation 7 will give the C.

The predicted L value should be within the tolerance of the inductors used, unless very long traces are present in the circuit implementation. Of more interest to us is the predicted C value. That predicted value, minus the probe capacitance and actual circuit value installed plus any estimate of layout parasitic [1], will give the apparent capacitance looking into the ADC input stage. Once this actual ADC plus layout value is determined, the filter capacitor may be reduced to more closely meet the filter design targets.

8 Conclusions

Modifying the typical RC last stage filter from the amplifier into the converter to an RLC filter with a series resistor and shunt resistor provides numerous design options for effectively driving into the converter. From the amplifier output side, it no longer sees a C load that has often led to stability or peaking problems with simple RC interfaces. From the converter side, it now principally sees a shunt C and R source at higher frequencies. The inductor acts to isolate both amplifier and converter from each other at higher, out-of-band frequencies.

Using a 2nd-order rolloff also improves SNR and SFDR for the system. Going from a simple RC filter (where the noise power bandwidth is 1.57*F_{-3dB}) to a 2nd-order Butterworth (where the noise power bandwidth is 1.11*F_{-3dB}) will give a $\sqrt{\frac{1.57}{1.11}} = 1.19$.

If the same white noise power is applied to the input of the two filters set up for the same F_{-3dB}, the 2nd-order filter will improve the SNR at the filter output by: 20 log(1.19) =1.5dB . Similarly, a 2nd-order rolloff in the filter will attenuate harmonics present at the input faster for the 2nd-order filter than for the 1st-order filter. For the differential implementations, only 3rd-order distortion terms are normally present. Once the input fundamental frequency exceeds F_{-3dB}/3, either filter will attenuate the 3rd-order harmonics present at the input. Typically, amplifier 3rd-order harmonics are increasing at a 20dB/dec rate due to loop gain rolloff. With a 40dB/dec 2nd-order filter following the amplifier, the worst-case output 3rd-order harmonic should occur at F_{-3dB}/3. If this is placed below the maximum desired frequency, an extended performance range for the (amplifier + filter) combination is achieved.

9 References

1. *Measuring Board Parasitics in High-Speed Analog Design* (SBOA094)

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